

DSP5680x Architecture Captures Best of DSP and MCU Worlds

David Zalac

1. Introduction

1.1 Overview

Motorola has introduced a new class of Digital Signal Controllers (DSC) devices addressing the needs associated with motor control and other system control applications. These devices are referred to as the 56F801, 56F803, 56F805 and 56F807, collectively referred to as the 56F800 series.

The objectives of this report are to present the architectural advantages offered by the 56F800 DSC series of devices with respect to conventional DSPs and MCUs, and to demonstrate the superiority of the 56F800 over other DSP-core based ICs having some controls-oriented capability.

The 56F800 DSC series of devices specifically addresses two main application requirement areas. First, computational requirements associated with complex control algorithms are met by a high-speed core, capable of executing up to 40 million multiply-accumulate operations per second. Second, control system interface requirements are met by a rich integrated peripheral set, including PWM capability, analog-to-digital conversion, bit I/O, and multiple serial interfaces.

In the following comparisons between the 56F800 series and conventional DSP and MCU devices, it is argued that both pure DSP and MCU devices fail to fully meet all the requirements of control system implementations. Further, among DSPs targeted for controls applications, the 56F800 devices combine *superior* processing power and a rich peripheral set.

Contents

1. Introduction	1
1.1 Overview	1
1.2 Control System Requirements	2
1.3 56F800 Architectural Overview.....	2
2. 56F800 DSC vs. Conventional DSP	2
2.1 Integrated Memory	3
2.2 Integrated Peripherals.....	3
2.3 Interrupt Support	4
3. 56F800 DSC vs. Conventional MCUs .	4
3.1 Mathematical Computation.....	4
4. 56F800 Controller vs. Other DSP/MCU Processors	6
4.1 DSP & MCU Architecture Requirements	6
4.2 Architecture Features Comparison.....	6
4.3 Interrupt Performance Comparison.....	8
4.4 Peripheral Details Comparisons.....	9
4.5 Architectural Advantages of the 56F800 DSC Series.....	11
5. Conclusions	12
5.1 Overall Performance and Cost Considerations	12
5.2 Summary	12
6. References	12

1.2 Control System Requirements

Medium-to-high end motor control and other control systems may require most or all of the following:

- High-speed Computational/Math Processing
- FLASH and SRAM memories
- Pulse-Width Modulation (PWM) Capability
- Analog-to Digital Conversion (ADC)
- Synchronous and/or Asynchronous Serial Comms
- CAN Interface
- Integrated Timers
- Single-bit I/O
- Quadrature Encoder Interfaces

1.3 56F800 Architectural Overview

The 56F800 devices possess a number of architectural features designed to meet digital signal processing needs and the control system requirements listed above. They are:

- 40-MIP core
- Harvard Architecture (separate program and data memory spaces)
- Fast bit-manipulation capability
- Integrated FLASH and SRAM memory modules
- Internal buses for Program & Data Memories and Integrated Peripherals
- External address and multiplexed data bus for program and data accesses
- Off-chip memory expansion up to 64K Program and Data memory
- Four-level pipelining
- Parallel instruction set with unique DSP addressing modes
- 19 addressing modes supporting DSP and MCU application software
- Integrated PWM modules
- 8-Channel ADC
- Quadrature encoder interfaces
- Up to 4 general-purpose quad timer modules
- CAN 2.0 A/B module
- Two asynchronous serial communications interfaces (SCI)
- High-speed synchronous serial interface (SPI)
- Dedicated pins for single-bit I/O (MPIO)

2. 56F800 DSC vs. Conventional DSP

Conventional DSP devices are well-suited to a wide range of applications requiring mathematical processing power. This arises from the high-speed DSP cores of the devices and a number of architectural features. DSPs typically support a single-cycle multiply-accumulate function, crucial to efficient DSP algorithm implementations. Additionally, DSPs share some of the architectural features of the 56F800 listed above. However, such DSPs lack a controls-oriented peripheral set and other features described on the next page.

The 56F800 has the same advantages as *pure* DSPs for meeting the computational needs of a given application. This conclusion follows the premise that 56F800 cores are true DSP cores. There are three crucial differences between *pure* DSP devices and the 56F800 DSC. First, the 56F800 devices possess a rich controls-oriented peripheral set shown [Table 1](#). Second, the 56F800 devices have extensive integrated FLASH and RAM memories. Third, the 56F800 has a sophisticated interrupt mechanism, supporting a large number of peripheral interrupt sources.

Table 1 contrasts the features of the 56F805 and a typical example of a *pure* DSP device with comparable CPU capability, namely the TI TMS320LC52.

Table 1. DSP56F805 vs. TMS320LC52 Feature Comparison

	DSP56F805	TMS320LC52
Processing bandwidth	40 MIPS	40 MIPS
Architecture style	Harvard	Harvard
Integrated FLASH	38K words	None
Integrated RAM	2.5K words	1K words
Integrated ROM	None	4K words
PWM channels	12	None
Integrated A/D channels	8	None
Asynchronous Serial channels	2	None
Synchronous Serial channels	1	2
Bit I/O	14 dedicated + 18 muxed	2
Quadrature Encoder I/Fs	2	None
CAN Interfaces	1	None
Timers	16	1
Interrupt sources	64	26

Two immediate conclusions can be drawn from **Table 1**: First, the 56F800 meets the computational requirements of DSP applications to the same extent as a conventional DSP. Second, the 56F800 has a much richer set of integrated memory and peripheral resources than the example standard DSP, making it well-suited to meet the needs of embedded control applications.

2.1 Integrated Memory

Memory requirements for any controls application can significantly affect system cost and design cycle time. Integrated FLASH and RAM memory modules of sufficient size may eliminate the need for external memory devices. This reduces dependence on the availability of such devices, decreasing schedule risk for a given hardware application. Address and data bus routing is completely eliminated, reducing PCB area and/or layer requirements. The on-chip memory requires no wait states, resulting in zero performance penalty for memory accesses. This may not be the case for systems requiring slower external memories. Further, both the lack of a need for external memory and the concomitant reduction in PCB area result in reduced system cost.

2.2 Integrated Peripherals

The 56F800 devices possess a number of integrated peripherals targeted for motor control and other control applications. Alternate solutions, such as off-chip substitutes, dramatically add to system cost as shown in **Table 2**. Additionally, external peripherals result in higher PCB chip counts and routing area requirements. As shown in **Table 1** and **Table 2**, the 56F800 integrated peripheral set greatly reduces system cost relative to a conventional DSP controls application solution. Further, since the on-chip peripherals have a predefined

interface to the core, as opposed to off-chip resources, system design, programming and control associated with the peripherals is simplified. Thus the software development cycle is shortened, resulting in development cost reduction.

Table 2. Examples of System Cost Impact of External Peripherals

Peripheral	Approximate Cost
ADC	\$5.05
Async Serial Interface	\$3.72
PWM	\$4.20
FPGA	\$10.00

The 56F800 peripheral set directly addresses the control system needs listed in the Control System Requirements list given above. Specifically, bit I/O, peripheral synchronous and asynchronous serial communications, PWM, ADC, Timer, and CAN modules are provided on-chip. Conventional DSP chips have peripherals occupying only, at most, a small subset of the 56F800 integrated peripheral offering.

2.3 Interrupt Support

Control systems typically make substantial use of interrupts from external devices and internal peripheral modules. Conventional DSPs handle only a small set of interrupts that are directly interfaced to the core. In contrast, the 56F800 supports a rather large number of interrupts as shown in [Table 1](#). Although the number of core interrupts addressed by the 56F800 is small compared to the total number of its interrupt sources, sophisticated internal interrupt multiplexing hardware provides for flexible and powerful support of 64 individually maskable and prioritizable interrupt sources.

The 56F800 is superior to conventional DSPs for controls-oriented applications. This conclusion follows from the demonstrated 56F800 advantages in integrated peripherals, integrated memories, and interrupt support.

3. 56F800 DSC vs. Conventional MCUs

Conventional MCUs may successfully fulfill the needs of low-to medium range embedded control applications. However, higher-end applications have computational processing power requirements that traditional MCUs fail to meet. This void is filled by the 56F800 DSC series of devices, delivering the computational and number-crunching power of traditional DSPs, as well as a peripheral set familiar to the controls system designer. The core and controls-oriented peripheral set of the 56F800 answer the needs of a medium-to-high level control system application. Mathematical processing requirements are met by a high-speed core supporting up to 40 million multiply-accumulates per second, while system interface requirements are met by a rich integrated peripheral set.

3.1 Mathematical Computation

The 56F800 has a true DSP core supporting a single-cycle multiply-accumulate function, and has a 16-bit bi-directional barrel shifter and an independent processing unit for fast bit manipulation. In contrast, typical MCUs lack the processing power required for implementation of high-complexity control algorithms.

[Table 3](#) contrasts architectural and other features of the 56F805 controller and the Infineon C164CI MCU.

Table 3. DSP56F805 vs. C164CI MCU Feature Comparison

	DSP56F805	C164CI
Processing bandwidth	40 MIPS	10 MIPS
Architecture style	Harvard	Von Neumann
Single-MAC cycles	1	5
Bit manipulation unit	Yes	Yes
Pipeline depth	4	4
Integrated FLASH	38K words	None
Integrated RAM	2.5K words	2K words
Integrated ROM	None	32K words
PWM channel pairs	6	3
Integrated A/D channels	8 (1.1 usec)	8 (9.7 usec)
Asynchronous Serial channels	2	1
Synchronous Serial channels	1	2
Bit I/O	32	59
Quadrature Encoder I/Fs	2	None
CAN Interfaces	1	1
Timers	16	3
Interrupt sources	64	32

A number of conclusions can be drawn from [Table 3](#).

First, the 56F800 wallops the MCU in terms of DSP processing capability by a factor of 20. The 56F800 requires 25ns for a multiply-accumulate operation, while the Infineon device requires 500ns, demonstrating the key advantage of the 56F800 versus general-purpose MCUs. This advantage follows not only from raw processor speed, but also on architectural features permitting the ability to perform a single-cycle dual-operand fetch and MAC operation. In general DSPs possess that operation while MCUs do not. This is a direct result of the Harvard architecture, which allows the core to address separate program and memory spaces. The Von Neumann architecture of the MCU fails to permit the parallel fetching of instruction words and data operands.

Second, while the MCU device above has a useful set of integrated controls-oriented peripherals, the 56F805 has a significantly richer set. This is particularly reflected by the number of interrupt sources of the 56F805 required to support all its peripheral modules.

Third, the on-chip memories are not strikingly dissimilar in size. However, the integrated FLASH of the 56F800 lends obvious advantages in terms of system flexibility.

Most MCUs simply fail to meet the processing requirements of controls applications requiring a significant amount of mathematical computation. This is primarily a result of architectural limitations and raw speed deficiency. The 56F800 competes well with an MCU in providing adequate controls peripherals, and also satisfies DSP processing needs.

We now further examine the architectural and other feature advantages of the DSP56800 devices compared with MCUs offered by four other device manufacturers.

4. 56F800 Controller vs. Other DSP/MCU Processors

There are a number of devices available offering both DSP and MCU capability. Here, we list the general architectural requirements often associated with each class of application.

4.1 DSP & MCU Architecture Requirements

DSP

- Hardware multiplier
- Ability to transport 2 data operands per cycle
- High-speed serial interfaces to analog conversion devices
- Hardware support for zero-overhead looping
- Circular buffers, including auto-buffering of input/output data streams to external devices
- High-speed clock

MCU

- Realtime interrupt processing
- Conditional jumps
- Bit manipulation capability
- Barrel shifter
- Controls peripherals

We have seen that the 56F805 better and more fully meets the requirements of control systems than conventional DSPs and MCUs. Now we examine architectural and other merits of the 56F805 with respect to other DSP-based devices having some controls-oriented capability. **Table 4** gives a comprehensive architectural feature comparison for four such devices.

4.2 Architecture Features Comparison

A number of conclusions can be drawn from **Table 4**:

- The 56F805 has substantially greater raw processing speed than its closest competitor
- The Infineon device doesn't possess the Harvard architecture essential to DSP
- The on-board 56F805 integrated FLASH benefit is equalled only by the TI device
- The 56F805 provides the greatest number of PWM channels
- The ADCM401 provides only limited bit-level I/O
- The 56F805 supplies the most abundant number of timers
- The large number of interrupts supported by the 56F805 enables lower interrupt latencies and greater ISR core density

Overall, the 56F805 clearly delivers the most valuable package of raw horsepower and on-chip memory and peripheral resources.

Table 4. DSP/MCU Device Architecture Comparison

	Motorola DSP56F805	TI '320LF2407	ADI ADMC401	Infineon C164
Processing Bandwidth	40 MIPS	30 MIPS	26 MIPS	12.5 MIPS
Architecture	Harvard	Harvard	Harvard	Von Neumann
1-cycle MAC	Yes	Yes	Yes	No
Barrel shifter	Yes	Yes	Yes	Yes
Bit-manip unit	Yes	No	Yes	Yes
Pipeline depth	4	?	?	4
FLASH	38K x 16	32K x 16	0	0
ROM	0	256 x 16	2K x 24	32K x 16
RAM	2K x 16	2592 x 16	3K x 24	2K x 16
PWM ch	12	16	8	6
ADC ch	8	16	8	8
SPI	1	1	2	2
SCI	2	1	1	1
Bit I/O	32	41	12	59
Quad encoder interfaces	2	0	1	0
CAN I/F	1	1	0	1
Timers	16	4	2	3
Interrupt sources	64	38	19	32
COP timer	Yes	Yes	Yes	Yes
JTAG path	Yes	Yes	No	No
PLL	Yes	Yes	No	Yes

The following subsections further detail interrupt performance and peripheral details for SPI, SCI, and PWM peripheral modules.

4.3 Interrupt Performance Comparison

Interrupt performance is typically measured in terms of latency, software overhead, flexibility in programming, total number of interrupts supported and other factors shown in [Table 5](#). A brief comparison of these criteria is given below.

Table 5. DSP/MCU Interrupt Performance

	56F800	TI 'C240x	ADIMC401	C164CI
# Core Ints	7	6	8	?
# Ext Ints	2	4	2	4
# Cfg. Pins	8	0	12	20
Total # Ints	64	38	19	32
Latency	6	9	6	6
Overhead	11	13	10	?
HW NMI?	No	No	Yes	Yes
Watchdog?	Yes	Yes	Yes	Yes
Fast Ints?	No	Yes	Yes	Yes

Application Impact

1. A larger number of interrupts support more complex systems
2. Shorter latency translates to faster controller response
3. Low overhead decreases MIPS requirement while supporting higher sample rates
4. NMI pin increases system robustness
5. Fast interrupts support higher sample rates and less overhead

4.4 Peripheral Details Comparisons

SPI

SPI modules of 56F800 DSC devices provide high-speed serial interfaces. Shown in [Table 6](#) is a brief comparison of key SPI features:

Table 6. SPI Feature Comparison

	DSP56F805	TMS320F2407	ADMC401	C164CI
Max bit rate	40e6 bps	7.5e6 bps	20e6 bps	5e6 bps
@Instr. Rate	40MHz	30MHz	26MHz	20MHz
# of SPIs	1	1	2	1
Bits/transfer	2-16	1-16	3-16	2-16
Full-duplex?	Yes	Yes	Yes	Yes
Master/Slave?	Yes	Yes	Yes	Yes
Double-Buffer?	Yes	Yes	Yes	?
Companding?	No	No	Yes	No

From [Table 6](#), we observe that the 56F803/05 support the highest serial throughput rate.

SCI

SCI modules of 56F800 DSC devices provide asynchronous serial interfaces. A brief comparison of key SCI features is shown in [Table 7](#).

Table 7. SCI Feature Comparison

	DSP56F805	TMS320F2407	ADMC401¹	C164CI
Max baud rate	2.5e6 bps	1.875e6 bps	0.3e6 bps	2.5e6/0.625e6
@Instr. Rate	40MHz	30MHz	26MHz	20MHz
Bits/transfer	8-9	1-8	8	8-9
# of rates	8192	65536	Autobaud	?
Sync also?	No	No	Yes	Yes

PWM

PWM modules of 56F800 DSC devices provide interfaces to motor drivers. [Table 8](#) shows a brief comparison of key PWM features.

Table 8. PWM Feature Comparison

	DSP56F803/5	TMS320F2407	ADMC401	C164CI
CH (Total)	6/12	16	6	0
CH (comp)	(0-3)/(0-6)	3	3	N/A
CH (indep)	6/12	2	3	N/A
Resolution	15	16	16	N/A
Edge/Center	Both	Both	Center	N/A
Programmable dead-time insertion?	Yes	Yes	Yes	N/A

As shown in [Table 8](#), the 56F805 supports the largest number of PWM channels.

Additionally, the 56F800 PWM module has a number of features that differentiate it from ordinary PWMs simply making use of timers to generate PWM signals. Additional features exist because the 56F800 PWM was specifically designed for motor control. Those unique features include:

- integrated fault protection
- multiple fault inputs
- fault programmability
- a PWM synchronization module
- high-current PWM outputs
- PWM commutation features
- programmable output polarity
- dead-time distortion correction
- half-cycle reload capability
- parameter update interlock
- write protection of critical system parameters

A detailed description of these features is given in the DSP56F80x User's Manual.

Quadrature Encoder Module

As shown in [Table 8](#), the 56F800 has two quadrature encoder modules. These modules enjoy particular architectural advantages with respect to other encoder modules.

Unique features include:

- an encoder watchdog timer
- a *delta* count register
- a *home* signal processing
- an *index* signal processing
- a pipelined velocity measurement technique

The measurement technique is based on the encoder waveform periods, independent of the encoder state width error. Further details are available in the DSP56F80x User's Manual.

4.5 Architectural Advantages of the 56F800 DSC Series

We have seen several key 56F800 architectural features that support the requirements of dual-purpose, digital signal processing and control applications. These are summarized below:

1. A hardware multiply-accumulate unit permits fast digital filtering and FFTs. The 56F800 supports up to 40 million multiply-accumulate operations per second.
2. A DSP's Harvard architecture allows simultaneous program instruction and data operand fetches. This feature is crucial in supporting typical DSP processing.
3. The 56F805 address-generation unit provides zero-overhead address updates for 2 operands to be used in a subsequent processor cycle. This unit also implements 19 addressing modes supporting efficient DSP and controls instruction execution and efficient compiler implementation.
4. Multiple internal buses provide connectivity and parallel operability of 4 separate execution units. This includes the ALU, AGU, program fetch and bit manipulation units. An external bus provides off-chip memory expansion capability.
5. A 4-deep pipeline allows for the parallel execution of various processor sub-tasks required to be performed in a given cycle, including instruction fetch, instruction decode, and data operand fetches.
6. On-chip memories provide zero-penalty accesses of program and data words, resulting in high throughput, reduced system cost, and increased flexibility.
7. Integrated SPI ports provide for glueless interfaces to codecs and other serial devices commonly found in DSP systems.
8. Integrated motor control peripherals, including PWM and timer modules, bit-level I/O, and quadrature encoder interfaces meet requirements typically encountered for control systems.
9. Other system requirements are addressed by on-chip peripherals, such as CAN, analog-to-digital converters, and asynchronous serial interface modules.
10. A programmable PLL simplifies and lends flexibility for providing clock signals internal and external to the 56F800.
11. The 56F800 core architecture includes a mechanism for zero-overhead, interruptible looping capability in software.
12. The 56F800 series supports embedded JTAG emulation and boundary scan hardware. This results in a headache-free realtime emulation environment.
13. The 56F800 core has features providing efficient C compiler code generation. These include a software stack, a register-based architecture and a large set of addressing modes.

5. Conclusions

5.1 Overall Performance and Cost Considerations

Performance in DSP/MCU is driven by a few simple factors. These include clock speed, integrated hardware multiplier, ability to quickly access peripherals, and interrupt response time. Performance is further enhanced by other device features as discussed at length in this report. In summary, the 56F800 has all the key architectural characteristics required to deliver high performance.

We have seen that integrated memories and peripherals can dramatically reduce system cost, as the requirement for external devices as well as board size is reduced. The full complement of such on-chip resources found on the 56F800 die is a strong asset in minimizing system cost.

5.2 Summary

The 56F800 provides a solid platform for motor control and other control applications. This is a result of architectural and other features of the device family. The 56F800 series is capable of supplying computational processing power comparable to that provided by pure DSPs, and also meets control system requirements via its rich integrated peripheral set.

The 56F800 is seen as a highly competitive solution for controls system implementations, in comparison with conventional DSPs, MCUs, and alternative combined DSP/MCU devices.

6. References

1. "DSP56800 Family Manual", Freescale Semiconductors, Inc
2. "DSP56F80x User's Manual", Freescale Semiconductors, Inc
3. "TMS320LC5x Digital Signal Processors", Texas Instruments, April 1996
4. "Microcomputer Components 16-Bit CMOS Single-Chip Microcontroller C164CI", Siemens AG 1998
5. "Single-Chip, DSP-Based High Performance Motor Controller ADMC401", Analog Devices, 1999



How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc. 2005. All rights reserved.

DSP56800WP2

Rev. 2
7/2005