Freescale Semiconductor, Inc.
User's Guide

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Hardware Development Guide for Vybrid Family of MCUs

1 About This Document

1.1 Overview

The purpose of this document is to help hardware engineers design and test their boards based on the Vybrid series of processors. It provides information on design checklists and board layout recommendations to ensure first-pass success and pave ways to avoid board bring-up problems. It also provides information on board-level testing and simulation such as properly configuring the JTAG tools, using BSDL for board-level testing, using the IBIS model for electrical integrity simulation, and more.

Engineers are expected to have a working understanding of board-layout principles and terminology, IBIS modeling, BSDL testing, and common board-hardware terminology.

1.2 Devices supported

This Hardware Development Guide currently supports the VF3xx, VF5xx, VF6xx, VF3xxR, and VF5xxR families of processors.

Contents

1.3 Essential reference

This guide is intended as a companion to the Vybrid-family chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see the *AN3298 "Solder Joint Temperature and Package Peak Temperature"* application note, which is available on www.freescale.com.

1.4 Suggested reading

This section lists additional reading that provides background for the information in this guide as well as general information about the architecture.

1.4.1 General information

The following documentation provides useful information about the ARM® processor architecture and computer architecture in general:

For information about the ARM® Cortex® A5 processor see:

- http://www.arm.com/products/processors/cortex-a/cortex-a5.phpo

For information about the ARM Cortex M4 processor see:

- http://www.arm.com/products/processors/cortex-m/cortex-m4-processor.php
- *Computer Architecture: A Quantitative Approach (Fourth Edition) – by John L. Hennessy and David A. Patterson*
- *Computer Organization and Design: The Hardware/Software Interface (Second Edition) – by David A. Patterson and John L. Hennessy*

The following documentation provides useful information about high-speed board design:

- *Right the First Time – A Practical Handbook on High Speed PCB and System Design – Volumes I & II - Lee W. Ritchey (Speeding Edge) – ISBN 0-9741936-0-72*
- *Signal and Power Integrity Simplified (2nd Edition) – Eric Bogatin (Prentice Hall) – ISBN 0-13-703502-0*
- *High Speed Digital Design – A Handbook of Black Magic – Howard W. Johnson & Martin Graham (Prentice Hall) – ISBN 0-13-395724-1*
- *High Speed Signal Propagation – Advanced Black Magic – Howard W. Johnson & Martin Graham – (Prentice Hall) – ISBN 0-13-084408-X*
- *High Speed Digital System Design – A handbook of Interconnect Theory and Practice – Hall, Hall and McCall (Wiley Interscience 2000) – ISBN 0-36090-2*
- *Signal Integrity Issues and Printed Circuit Design – Doug Brooks (Prentice Hall) – ISBN 0-13-141884-X*
- *PCB Design for Real-World EMI Control – Bruce R. Archambeault (Kluwer Academic Publishers Group) – ISBN 1-4020-7130-2*
- *Digital Design for Interference Specifications – A Practical Handbook for EMI Suppression – David L. Terrell & R. Kenneth Keenan (Newnes Publishing) – ISBN 0-7506-7282-X*

- *Electromagnetic Compatibility Engineering – Henry Ott (1st Edition – John Wiley and Sons) – ISBN 0-471-85068-3*
- *Introduction to Electromagnetic Compatibility – Clayton R. Paul (John Wiley and Sons) – ISBN 978-0-470-18930-6*
- *Grounding & Shielding Techniques – Ralph Morrison (5th Edition - John Wiley & Sons) – ISBN 0-471-24518-6*
- *EMC for Product Engineers – Tim Williams (Newnes Publishing) – ISBN 0-7506- 2466-3*

1.5 Related documentation

For related Freescale documentation, see www.freescale.com. Additional literature is published as new Freescale products become available.

1.6 Conventions

This document uses the following notational conventions:

- `Courier` – used to indicate commands, command parameters, code examples, and file and directory names
- *Italics* – italics indicates command or function parameters
- **Bold** – function names are written in bold
- cleared / set – when a bit takes the value zero, it is said to be cleared; when it takes a value of one, it is said to be set
- **mnemonics** – instruction mnemonics are shown in lowercase bold; book titles in text are set in italics
- sig_name – internal signals are written in all lowercase
- *nnnn nnnn*h – denotes hexadecimal number
- 0x – alternate notation denoting hexadecimal number
- 0b – denotes binary number
- **r**A, **r**B – instruction syntax used to identify a source GPR
- **r**D – instruction syntax used to identify a destination GPR
- REG[FIELD] – abbreviations for registers are shown in uppercase text; specific bits, fields, or ranges appear in brackets; for example, MSR[LE] refers to the little-endian mode enable bit in the machine state register
- x – in some contexts, such as signal encodings, an unitalicized x indicates a "Don't Care"
- *x* – an italicized x indicates an alphanumeric variable
- *n, m* – an italicized n indicates a numeric variable

NOTE

In this guide, notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

1.7 Signal conventions

- $\overline{\text{RESET}}$ – an overbar indicates that a signal is active when low
- _b, _B – alternate notation indicating an active-low signal
- *signal_name* – lowercase italics is used to indicate internal signals

1.8 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Definitions and acronyms

Term	Definition
AC	Alternating Current
AFE	Analog Front End
ARM	Advanced RISC Machines (processor architecture)
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array (package)
BOM	Bill Of Materials
BSDL	Boundary-Scan Description Language
BSP	Board Support Package
CAN	Controller Area Network (bus)
CCM	Clock Controller Module
DC	Direct Current
DCU	Display Control Unit
DDR	Double Data Rate (DRAM type)
DDR2	DDR type 2
DDR3	DDR type 3
DRAM	Dynamic Random-Access Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ENET	Ethernet
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
FIRC	Fast Internal RC Oscillator
FSL	Freescale
GND	Ground
GPIO	General-Purpose Input / Output
HDMI	High-Definition Multimedia Interface

Table 1. Definitions and acronyms (continued)

Term	Definition
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit (interface)
IBIS	Input / Output Buffer Information Specification
I/O	Input / Output
IOMUX	Input / Output MUltipleXing (chip level)
ISBN	International Standard Book Number
JTAG	Joint Test Action Group
LDO	Low Drop-Out (voltage regulator)
LIN	Local Interconnect Network
LPCG	Low-Power Clock Gating
LPDDR2	Low-Power DDR2
LQFP	Low-Profile Quad Flat Package
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
MAPBGA	Molded Array Process Ball Grid Array (package)
MII	Media Independent Interface
MLB	MediaLB (Media Local Bus)
ODT	On-Die Termination
PC	Personal Computer
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
ppm	Parts per Million
RAM	Random-Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RMII	Reduced MII
ROM	Read-Only Memory
RX	Receive
SIRC	Slow Internal RC Oscillator
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
TX	Transmit
TVS	Transient Voltage Suppressor

Table 1. Definitions and acronyms (continued)

Term	Definition
UART	Universal Asynchronous Receiver / Transmitter
USB	Universal Serial Bus
USB OTG	USB On-The-Go
USB 2.0	USB version 2.0

2 Design Checklist

2.1 Design checklist overview

This chapter provides a design checklist for the following Vybrid series families of processors:

- VF3xx
- VF5xx
- VF6xx
- VF3xxR
- VF5xxR

The design checklist tables (see Section 2.2, “Design checklist tables”) contain recommendations for optimal design. Where appropriate, the checklist tables also provide an explanation of the recommendation so that users have a better understanding of why certain techniques are recommended. All supplemental information referenced by the checklist appear in sections following the design checklist tables.

2.2 Design checklist tables

Table 2. DDR recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Connect ZQ pad to an external 240 Ω 1% resistor, whose other side is connected to GND.	This is a reference used during calibration of the DRAM output buffer driver.
	Connect VREF to a source equal to 50% of the DDR power voltage value. Shunt the lower resistor with a closely-mounted small-size minimum 0.1 to 0.22 μF capacitor.	A precision external resistor divider may be used (see Section 2.6, “DDR reference circuit” for value selection). Using resistors with recommended tolerances ensures the ± 2% VREF tolerance per the LPDDR2 and DDR3 specifications. Using a tracking voltage regulator is optional; it is recommended for memory configurations of more than four devices, which is not the case.

Table 2. DDR recommendations (continued)

Checkbox	Recommendation	Explanation / supplemental recommendation
	Connect $\overline{\text{RESET}}$ to a 10 to 100 kΩ pull-up resistor to the DDR power rail.	Only applicable if DDR self-refresh mode is used when Vybrid is in the LPStop modes, in which its I/Os are in the high-impedance state. Any Vybrid's terminations (such as 50 Ω) should not be present; simulation should be performed to ensure signal integrity.
	Connect CKE to a 10 to 100 kΩ pull-down resistor to GND.	
	When LPDDR2 is used, make sure it is connected to correct Vybrid I/Os.	The DRAM Controller's I/O names are for the DDR3 default and not necessarily match the LPDDR2 functionality.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply can be left floating.

Table 3. Boot-mode (BOOTMOD and RCON) recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	If peripherals are connected to the Vybrid I/Os also used for the boot-mode function, use peripherals with three-state outputs, otherwise connect them through three-state buffers.	It should be ensured that the peripherals' (or their three-state buffers') outputs are in the high-impedance state during the boot-mode selection interval, for example, by utilizing the Vybrid $\overline{\text{RESET}}$ signal.
	RCON31 must be tied low during reset. When this pin is left floating, it may be registered as logic 1. In this case the BOOT ROM will enter an endless loop and not boot from any interface.	Entering the endless loop allows for testing watchdog behavior during development. This pin will have no effect when booting from fuses.
	For the Vybrid I/Os used for both boot-mode function and high-speed peripherals, isolate the boot-mode circuits by inserting either series resistors or three-state buffers.	Depending on design specifics, the Vybrid I/Os bearing DCU signals might be a good example. To keep the trace stubs short and prevent signal integrity issues, place the isolation components as close to the Vybrid I/Os as possible. See schematic examples in Figure 2 and Figure 3.
	Depending on the design specifics, feel free to mark either part of the boot-mode related circuits or all of them as “optional.”	Depending on the development stages, these circuits become quite often fully or partially unnecessary, on the production stage, where the Vybrid processor boot details may be defined by its pre-programmed fuses.

NOTE

When not using HAB, RCON16 must be tied low during RESET. If this bit is registered as '1', the device will always boot from the boot device, even when exiting LPSTOP modes.

Table 4. I²C recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Verify the target I²C interface clock rates.	The bus can only operate as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I²C port.
	Verify that the target I²C address range is supported and does not conflict with other peripherals. If there is an unavoidable address conflict, move the offending device to another I²C port.	The Vybrid processors support up to: • three I²C ports for the VF3xx and VF3xxR families • four I²C ports for the VF5xx, VF6xx, and VF5xxR families If moving a conflicting device to another I²C port is undesirable, check if re-mapping of its address is possible. See example in Table 13.
	Do not place more than one set of pull-up resistors on the I²C lines.	Placing one pair of pull-up resistors only to prevent excessive output loading is a good design practice.

Table 5. JTAG recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Do not use external pull-up or pull-down resistors on TDO.	TDO is configured in a way that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on TDO is detrimental. See Table 15 for a summary of the JTAG interface.
	Keep I²C traces aways from signals with fast edges, eventually use BLM chokes to filter out glitches on the clock I/O.	The I²C CLK input does not have a glitch filter. Due to the nature of I2C, clock edges are relatively slow and traces can be traversing the PCB, which makes them sensitive to EMC noise; that means glitches may be imposed upon a slow edge and this glitch can be seen as an additional clock. When that happens, the receiver and transmitter get out of sync and the transfer will stall.
	If external pull resistors are used with JTAG signals, except for TDO, ensure that the on-chip pull-up / pull-down configuration is matched. For example, no external pull-down on an input with an on-chip pull-up.	External resistors may be used with all JTAG signals, except for TDO, but are not required. See Table 15 for a summary of the JTAG interface.
	Use a 10 kΩ pull-up resistor on the active-low JTAG connector reset pin ($\overline{\text{TRST}}$).	A debugger uses this bi-directional open-drain pin to either reset the processor or to detect if it is in the reset state.
	Tie the VTREF JTAG connector pin to 3.3 V.	"Voltage Reference" is used by the debugger to create its logic-level reference (VTREF/2) for the input comparators and auto-adjust the output voltage levels.
	When using the JTAG system reset (SRST) signal is required, make it control the Vybrid system reset ($\overline{\text{RESET}}$) pin.	Since Vybrid has no separate JTAG system reset pin, its $\overline{\text{RESET}}$ pin should be used. In this case, the JTAG SRST signal should be connected either directly to it or combined with the external power-on reset circuitry.

Table 6. Power and decouple recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Comply with the power-up sequence guidelines as described in the data sheet to guarantee reliable operation of the device.	Any deviation from these sequences may result in the following situations: • excessive current during power-up phase • prevention of the device from booting • irreversible damage (worst-case scenario)
	Do not power any external loads from the built-in LDOs.	These LDOs are for the internal loads only. For example, DECAP_V11_LDO_OUT is the on-chip LDO output used, among other blocks, to power the on-chip crystal oscillators; using it for external loads is not recommended because of its limited output capability and clock quality degradation due to noise generated by external loads.
	Handle unused power inputs in one of the following ways: • Connect to power sources with relevant voltage values; to save power, disable the relevant blocks and / or gate their clocks. • Keep floating.	Due to the internal structure of the pin multiplexer, proper care should be taken if a pin is shared by several Vybrid blocks; for example, if it can act as either a GPIO or an ADC input, it still has to be powered to keep the GPIO functionality, even if the ADC functionality is not required. For details on handling unused analog pins, including the power inputs, see Table 17 (based on the processor data sheet information).
	Keep the unused built-in LDOs' pins floating.	If a built-in LDO is not powered, it needs no decoupling capacitors on its input and output.
	Provide each capacitor with a path to its power pin / via with impedance as low as possible. Use a via size appropriate for the expected current draw.	Placing a capacitor no farther than 50 mils from its power pin / via is recommended as well as using as much copper as possible, for example, solid copper or a wide trace.
	Only one 10 μF bulk capacitor should be connected to each of these on-chip LDO regulator outputs: • DECAP_V25_LDO_OUT • DECAP_V11_LDO_OUT • USB_DCAP (if USB interface is used)	If the nominal capacitance value is larger than recommended, power-up ramp time is excessive and proper operation is not guaranteed. Select a low-ESR capacitor type.
	In addition to a bulk capacitor, provide each power rail with small-value capacitors, for example, 0.1 μF or 0.22 μF.	With proper layout quality, there is no need for one capacitor per pin / via; one per each pair of adjacent pins / vias is sufficient.
	Meet the maximum voltage-ripple requirements on the power inputs.	Common peak-to-peak requirement is less than 5% of the average supply voltage value.
	Select and connect the backup battery properly.	The target battery is a 3 V coin cell. If a rechargeable type is used, the appropriate series resistor value must be used (see the data sheet for details).

Table 7. Oscillator and clock recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Precision 32.768 kHz on-chip crystal oscillator: • Connect a crystal between XTAL32 and EXTAL32. • Select a crystal with the ESR value specified in the data sheet. • Follow the manufacturer's load-capacitance recommendation. • Use short traces between the crystal and Vybrid, with a GND plane under the crystal, load capacitors, and associated traces. • Do not use any external resistors in the oscillator circuit.	The capacitors implemented on either side of the crystal are about twice the crystal load capacitance. To hit the target oscillation frequency, board capacitors need to be reduced to compensate for the board and oscillator I/Os parasitic capacitance; typically 12-18 pF is employed. The integrated oscillator has an on-chip self-biasing scheme but has high impedance (is relatively weak) to minimize power consumption. Care must be taken to limit parasitic leakage from XTAL32 to either power or GND (> 100 MΩ) as this negatively affects the oscillator bias (~0.5 V for XTAL32 and EXTAL32) and causes the start-up margin reduction. If there is no oscillator signal at any time, the chip will automatically use the SIRC/4 clock as a 32 KHz source, provided the SIRC is not disabled by software.
	External kHz source: • Drive XTAL32 directly (DC-coupled) within the swing and frequency range specified in the data sheet, with EXTAL32 being floating or driven with a complimentary signal.	To prevent damage / malfunction, the input signal should not be driven if the DECAP_V11_LDO_OUT supply is off. If there is no external signal at any time, the chip will automatically use the SIRC/4 clock as a 32 KHz source, provided the SIRC is not disabled by software.
	Loose-tolerance 128 kHz on-chip ring oscillator (SIRC): • Use it only for applications not requiring precise clock.	The system uses 32 kHz, that is, 128 kHz divided by four by default, the frequency tolerance being specified in the data sheet. The ring oscillator starts faster than the external-crystal oscillator and is used until the latter reaches stable oscillation. It also starts automatically if no clock is detected at XTAL32 at any time, including the case when there is no crystal and XTAL32 is tied to GND (EXTAL32 floating).

Table 7. Oscillator and clock recommendations (continued)

Checkbox	Recommendation	Explanation / supplemental recommendation
	Precision 24 MHz on-chip crystal oscillator: • Connect a fundamental-mode crystal between XTAL and EXTAL. • Select a crystal with: – ESR and maximum drive level specified in the data sheet – load capacitance of 20 pF or lower • Follow the manufacturer's load-capacitance recommendation. • Bias the XTAL ball with a 2.2 MΩ resistor to GND placed as close to the ball as possible.	The Freescale BSP software expects this frequency to be 24 MHz. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. See Table 16 for guidelines and the “Crystal oscillator” chapter of the reference manual and the USB interface specification for details. The crystal drive level depends on the ESR value; the lower it is, the lower the maximum drive-level rating may be. For details, see Section 2.3, “24 MHz crystal drive level calculation.” The XTAL bias must be adjusted externally to ensure reasonable start-up time. Without the resistor, start-up time may be 200 ms or more.
	External MHz source: • Drive XTAL directly (DC-coupled) within the swing and frequency range specified in the data sheet, EXTAL being floating.	The Freescale BSP software expects this frequency to be 24 MHz. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. See Table 16 for guidelines, the “Crystal Oscillator” chapter of the reference manual, and the USB interface specification for details. To prevent damage / malfunction, the input signal should not be driven if the DECAP_V11_LDO_OUT supply is off. Low-voltage clock sources are quite uncommon; connection example of a 3.3 V powered clock is shown in Figure 1.

Table 7. Oscillator and clock recommendations (continued)

Checkbox	Recommendation	Explanation / supplemental recommendation
	Loose-tolerance 24 MHz on-chip ring oscillator (FIRC): • Use it only for applications not requiring precise clock.	For frequency tolerance, refer to the data sheet. The ring oscillator starts faster than the external-crystal oscillator and is used until the latter reaches stable oscillation. Then, depending on the ANADIG setting, the clocking scheme either switches to the external-crystal source (default) or keeps using FIRC (see the "Clock Generation and Distribution" block diagram from the processor reference manual for details). Thus, if the external-crystal 24 MHz source is selected but not physically provided, the processor operation fails. Selecting loose-tolerance FIRC is not recommended if Vybrid PLLs are used.
	Use high-speed LVDS0P / LVDS0N for clock input / output in the range from zero to the Vybrid A5 core frequency. Alternatively, a single-ended signal can be used to drive the LVDS0P input. In this case, LVDS0N should be tied to a constant voltage level equal to 50% of its power domain value. Provide termination for high-frequency signals taking the internal I/O impedance into account. Leave floating if unused.	This differential pair is only used for clock, not data. The electrical parameters are compatible with the TIA / EIA-644 standard. Although designed to operate up to the Vybrid A5 core frequency, the block has only been tested up to 400 MHz at the date of publication. Signals above a few tens of MHz may be impractical due to board attenuation. Board simulation is strongly encouraged. The LVDS I/Os belong to the DECAP_V25_LDO_OUT power group. It may be configured: • as input to feed external reference clocks to the on-chip PLLs and / or modules • as output (without drive-strength or slew control) to be used as a reference or functional clock for peripherals • disabled after initialization (if unused)

Table 8. Reset recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	For system reset, assert the Vybrid $\overline{\text{RESET}}$ pin low at power-up and keep it asserted until initialization process of the memory IC used for booting is completed (for details, see Section 8.6.1, "Verifying boot-source readiness"). If required, wire a reset switch, for example, push-button, to $\overline{\text{RESET}}$.	If an external system reset signal is used, $\overline{\text{RESET}}$ acts as a cold-reset, active-low input, which resets all Vybrid modules and logic. $\overline{\text{RESET}}$ is recommended to be used in addition to the internally-generated power-on reset signal (logical and both internal and external signals are considered active-low). See Section 8.5, "Avoiding power-on reset pitfalls" for details.
	If using a reset IC is required, use one with an open-drain / collector type and a pull-up resistor to Vybrid's VDD33 power rail.	$\overline{\text{RESET}}$ in some occasions acts as an active-low output (see details in Figure 33).
	If applicable, use the $\overline{\text{RESET}}$ pin for the JTAG interface operation.	See Table 5 for details.

Table 9. MAC (Ethernet) recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	If Vybrid generates and delivers the RMII reference clock, apply the *e8052* Erratum workaround.	Without the workaround, the TX direction does not operate. See Section 12.3.0.2, "Internal RMII reference clock" for details.
	For proper IEEE-1588 operation, provide sufficient wait time in the software code as described in the Reference Manual.	Without sufficient wait time, the time-stamp read operation returns incorrect data.

Table 10. USB recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	If monitoring of the port's ID pin is required, for example, for "true USB OTG device" operation, use an additional processor's GPIO for that.	The ID function is not built into Vybrid's USB PHYs' hardware, so it should be covered by its software.
	Turn VBUS on only when the port is operating as host.	• It is recommended to use a VBUS power switch, which is explicitly turned on by software and is by default turned off during the processor power-on and boot. • For host-only operation, VBUS on the connector may be connected to a 5 V supply directly, provided its current is limited to 5 A and it recovers automatically after the overload is over.
	Connect the VBUS pin of the connector to the Vybrid USBn_VBUS and USBn_VBUS_DETECT pins.	Monitoring the VBUS level on the USB connector is a part of OTG signaling.
	To comply with the USB host specification, connect VBUS directly to a 5 V supply. Connect the VBUS supply on the connector to the Vybrid USBn_VBUS pin and, optionally, USBn_VBUS_DETECT pin.	In typical USB host cases, VBUS stays on permanently.

Table 10. USB recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	In case of the USB peripheral use, USB VBUS power from the connector may or may not be used.	As per the USB peripheral specification, two power options exist: • bus-powered (power from USB) • self-powered (its own power supply)
	For USB versions 2.0 and later, use a high-frequency board material.	Such low-attenuation materials are rated for frequencies in GHz range (examples provided in Section 3.2, “Stackup recommendations”).

Table 11. Miscellaneous recommendations

Checkbox	Recommendation	Explanation / supplemental recommendation
	Tie the Ext_POR pin to GND.	This pin is for factory use only. Despite its name, do not use this pin for the "power-on reset" purposes, but use RESET instead.
	Tie the TEST pin to GND.	These pins are for factory use only.
	Tie the FA_VDD pin to VDD.	
	For termination of unused analog interfaces, see Table 17.	–
	As per *e7955*, add external pull-up resistors to 3.3 V on the LPStop modes' wakeup pins.	These pull-up resistors should have values between 10 and 100 kΩ.
	Leave DDR_ODT1 pin floating.	This pin is unused.

2.3 24 MHz crystal drive level calculation

As mentioned in Table 7 for the “Precision 24 MHz on-chip crystal oscillator,” this chapter discusses the approach guaranteeing that the maximum drive level requirement for a 24 MHz crystal selected for use with Vybrid is met. If the crystal is overdriven, the potential failure effect is not immediately obvious. The crystal may either fail over time or its operating frequency may be affected.

An approached based on several parameters provided by the crystal supplier is offered. Without it, a crystal with a 250 µW maximum drive level rating shall be used. At the same time, careful crystal selection allows lowering it down to 100 µW.

The crystal described in Table 12 is chosen as an example because it is used in numerous Freescale development platforms.

Table 12. Crystal example[1]

Manufacturer	Part Number	Package	Maximum Drive
Epson Toyocom	TSX-3225 24.0000MF 15X-AC3	3.2 × 2.5 mm	200 µW

1 Freescale cannot recommend one supplier over another and does not suggest that this is the only crystal supplier

To minimize crystal drive level, the balance of load capacitance (CL1, CL2), motional resistance (Rs), and package capacitance (C0) must be kept low.

The C0 value of 5 pF is used for example only; the actual value depends on the package type and may be verified with the crystal supplier.

2.4 Connection of 3.3 V powered external 24 MHz clock source

As referred to in Table 7 for the “External MHz source”, Figure 1 shows how to connect a 3.3 V powered external 24 MHz clock source to the Vybrid XTAL pin. The board stray and the XTAL pin capacitances shall be taken into account while tuning the voltage-divider capacitors.

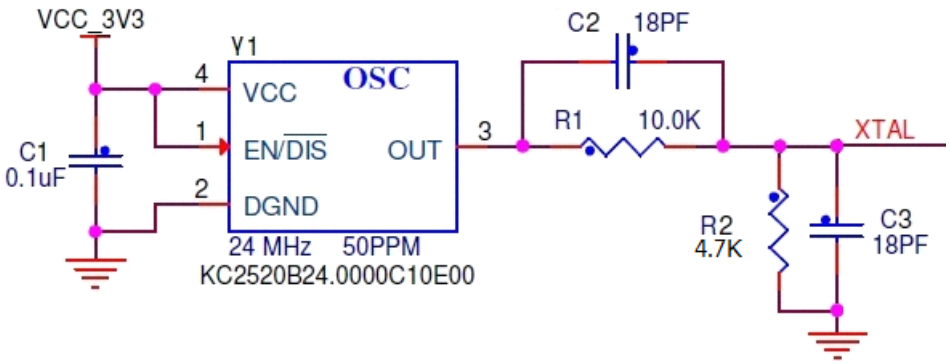


Figure 1. Connection of 3.3 V powered external 24 MHz clock source

2.5 Boot-mode circuit isolation

Provided below are two boot-mode circuit isolation options:

- based on series resistors (see Figure 2) – inexpensive but with somewhat compromised performance due to non-zero conductivity of the series resistors
- based on three-state buffers (see Figure 3) – more expensive classic approach with best performance:
  - high drive-strength logic levels on the processor’s I/Os while sampling the boot-mode configuration
  - ideal isolation of the above-mentioned I/Os from the boot-mode circuit during normal operation

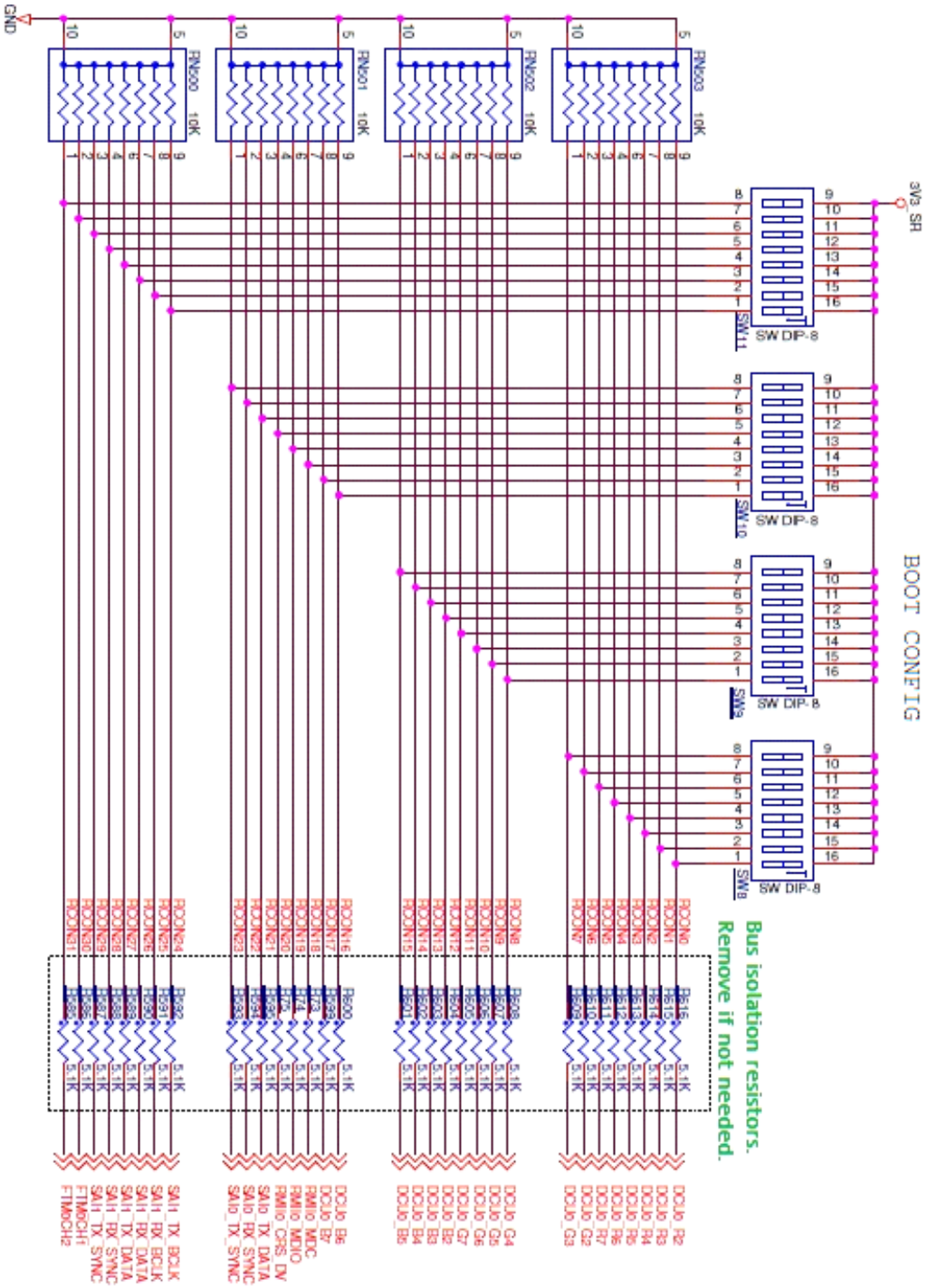


Figure 2. Isolation with series resistors

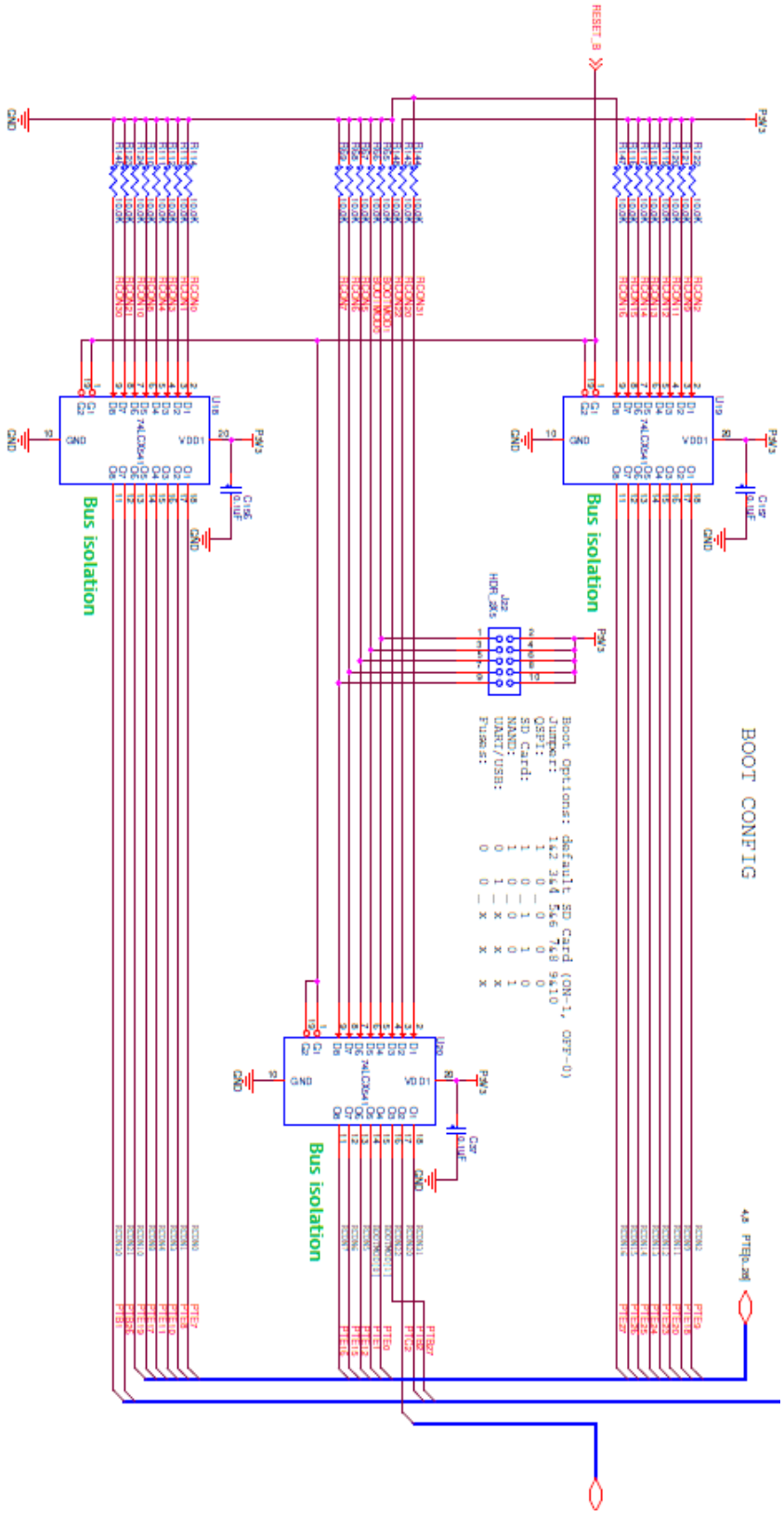


Figure 3. Isolation with three-state buffers

NOTE

These examples only illustrate the circuit isolation options; what processor's I/Os are involved in the boot-mode circuit is design-specific.

2.6 DDR reference circuit

A simple voltage divider based on two equal-value inexpensive 1% resistors is good enough to generate the DDR reference; see the DDR3 0.75 V reference example in Figure 4.

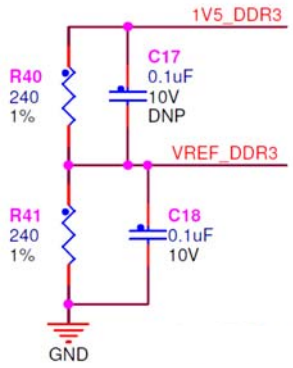


Figure 4. DDR3 0.75 V VREF supply

If a DDR memory device with 2 µA VREF input current is used, the maximum recommended value is 2.42 kΩ 1%. For the BOM consolidation, a 1% resistor type already used somewhere else in the design might be utilized, for example, the one used for the ZQ pad (see Table 2 and Figure 4).

See the layout recommendations for this signal in Section 3.6.4, “VREF recommendations.”

2.7 I^2C ports usage

2.7.1 I^2C address and speed

Table 13 shows a spreadsheet approach to avoid I^2C conflicts as referenced in Table 4.

NOTE

The example in this section applies to a hypothetical Vybrid-based reference design.

Notice that the cells outlined in black in Table 13 highlight two different issue types:

- a potential bus-speed problem (of the RF Tuner)
- a potential slave-address conflict (between the MLB Card and the Analog-to-Digital Converter)

Table 13. I²C bus example spreadsheet

Peripheral	Bus activity level	Speed (kbit/s)	Slave addresses supported on peripheral (hex)	Selected system address (hex)
MLB Card	Low	400	40	40
Port Expander	Low	400	30, 32, 34	30
RF Tuner	Med	250	C0, C2, C4, C6	C0
Analog-to-Digital Converter	Med	400	40, 42	42
Audio codec	Low	400	90, 92, 94, 96	90

2.7.1.1 Bus-speed issue resolution

The RF tuner is rated for up to 250 kbit/s, whereas all other peripherals are rated for up to 400 kbit/s. If all of them are placed on the same I²C bus, it forces to lower its speed, since it cannot exceed that of the slowest one.

If the I²C bus rate exceeded the RF tuner module's maximum bus rate, the I²C bus operation might fail or become unpredictable. The slow peripheral may unpredictably take over the bus or malfunction in some other way.

If utilizing the other peripherals' higher speed is preferred, the RF tuner must be isolated on a separate I²C port (see Table 14).

2.7.1.2 Slave-address conflict resolution

As mentioned in Table 4, this conflict may be easily avoided by remapping the address of one of the conflicting devices, in this specific case, the Analog-to-Digital Converter's address (see the "Selected system address" column in Table 13 and Table 14).

2.7.1.3 I²C port usage scenario

Assuming that the system can function properly with a reduced bus rate of 250 kbit/s, Table 14 provides a possible optimized I²C port usage.

Table 14. I²C port usage scenario

Vybrid I²C Ports	Peripheral	Selected system address (hex)	Bus speed (kbit/s)
Port 1	MLB Card	40	400
Port 1	Port Expander	30	400
Port 1	Analog-to-Digital Converter	42	400
Port 1	Audio codec	90	400
Port 2	RF Tuner	C0	250

2.7.2 I²C interface timing settings

Refer to the “Clock rate and IBFD Settings” chapter of the processor reference manual for details.

2.7.3 I²C interface operation in presence of noise

Complex boards quite often have high-frequency noise induced into their I²C lines:

- Power-hungry digital components may contaminate power and ground planes with significant amount of high-frequency ripple.
- Due to limited space, electromagnetic coupling of the I²C lines to the numerous high-speed traces is not unlikely, especially fast simultaneous switching of outputs like data buses can introduce noise.

The nature of the I2C bus with its relatively slow edges makes it susceptible to glitches forming on the clock edges. When these glitches are close to the threshold level of the input buffer, there is a fair chance that the glitch is considered an additional clock cycle. Due to this, the receiver and transmitter get out of sync. Some Freescale development platforms have series ferrite beads on the I²C data and clock lines; in this case, a low-pass LC filter on each line is formed by the bead inductance and the parasitic capacitance to ground, which consists of two parts – the board stray capacitance and the processor’s I/O pin one.

2.8 JTAG signal termination

Table 15 is a JTAG termination chart.

Table 15. JTAG interface summary

Signal	Vybrid I/O direction	Vybrid on-chip termination	External termination
TCK	Input	Pull-down	Not required; 10 kΩ pull-down resistor may be used.
TMS	Input / Output	Pull-up	Not required; 10 kΩ pull-up resistor may be used.
TDI	Input	Pull-up	Not required; 10 kΩ pull-up resistor may be used.
TDO	Output	None	Do not use pull-up or pull-down resistors.

2.9 24 MHz oscillator tolerance

The following table provides 24 MHz oscillator tolerance guidelines (see Table 16). Since these are guidelines, the designer must verify all tolerances are within the official specifications.

Table 16. 24 MHz crystal tolerance guidelines

Interface	Tolerance (± ppm)
MAC (Ethernet)	50
USB2.0	500

2.10 Unused analog interfaces

Table 17 shows the recommended connections for unused analog interfaces (see Table 11).

Some I/O pins are shared by both the digital and analog Vybrid modules (for details, see the "Recommended Connections for Unused Analog Interfaces" section of the Vybrid data sheet). When shared pins are used as digital pins, their associated analog supply must also be powered. This also applies to boundary scan, if shared pins are used in boundary scan tests. If shared pins are not used in BSDL tests, the analog supplies can remain off during BSDL.

Table 17. Recommended connections for unused analog interfaces

Module	Pin name	Recommendations
ADC / DAC	VDDA33_ADC, VREFH_ADC	Both at the same time tied to 3.3 V or floating.
	VREFL_ADC	Grounded if VREFH_ADC is tied to 3.3 V. Floating if VREFH_ADC is floating.
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Grounded or floating.
CCM	LVDS0P, LVDS0N	Floating.
DAC	DACO0, DACO1	Floating.
USB	USB_DCAP, USB0_VBUS, USB1_VBUS	Never ground directly due to latch-up risk. If only one USBx_VBUS remains unused, connect it to ground through a 10 kΩ resistor. If both USBx_VBUS remain unused, tie all three pins together and connect this common net to ground through a 10 kΩ resistor.
	USB0_GND, USB1_GND	Grounded.
	USB0_VBUS_DETECT, USB1_VBUS_DETECT	Floating.
	USB0_DM, USB0_DP, USB1_DM,USB1_DP	Floating.
Video ADC	VDDA33_AFE	Tied to 3.3 V or floating.
	VDD12_AFE	Tied to 1.2 V or floating.
	VADC_AFE_BANDGAP	Floating.
	VADCSE0, VADCSE1, VADCSE2, VADCSE3	Grounded or floating.

3 Layout Recommendations

This chapter provides recommendations to assist design engineers with the correct layout of their Vybrid family-based system. The majority of this chapter discusses the implementation of the DDR interface, but it also provides recommendation for power, LVDS, USB, reference resistors and ESD, as well as related electromagnetic emission.

This chapter uses the Vybrid Tower module and the Vybrid Automotive platform to illustrate the key design concepts. See the relevant layout files as an addition to this chapter.

3.1 Basic design recommendations

The Vybrid processor comes either in the 364-ball MAPBGA (VF5xx, VF6xx, and VF5xxR) or the 176-lead LQFP (VF3xx and VF3xxR) package.

For detailed information about the packages, see the Vybrid Consumer and Automotive data sheets.

3.1.1 Mechanical data

3.1.1.1 MAPBGA package

The VF5xx, VF6xx, and VF5xxR processors come in a 17 × 17 mm MAPBGA package with 0.8 mm ball-pitch. The ball-grid array contains 20 rows and 20 columns; 36 empty pins in the rows F and R and columns 6 and 15 form a square-shaped gap around the center cluster, making it a 364-ball BGA package.

Figure 5 shows the ball-grid array. Figure 6 shows additional package information.

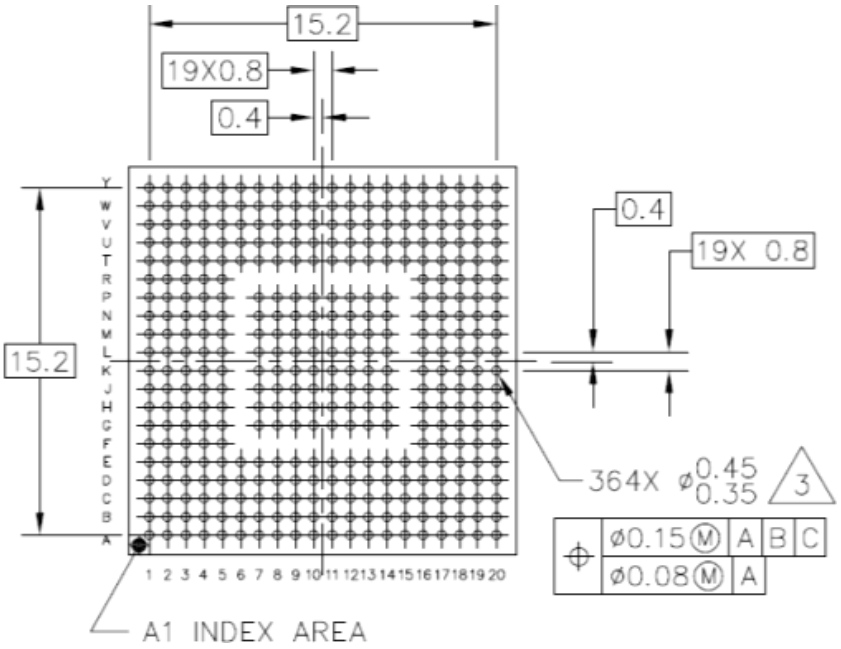


Figure 5. Vybrid MAPBGA ball-grid array

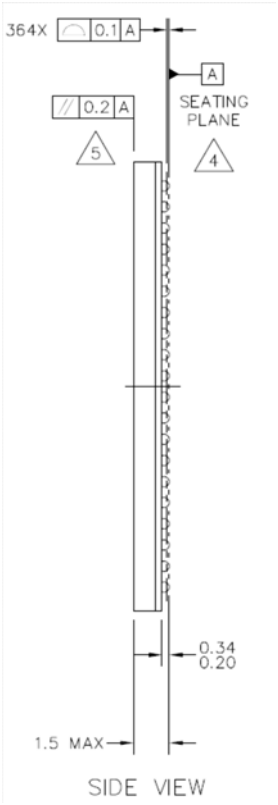


Figure 6. Vybrid 364 MAPBGA package information

It is critical to maintain the recommended footprint of a 13-mil pad with a 17-mil open solder mask for ease of fanout. In this case, the solder paste is the same as the pad with 13 mil, which allows an air gap of 18.49 mils between pads.

When using the Allegro tool, optimal practice is to use the footprint as created by Freescale. When not using the Allegro tool, use the Allegro footprint export feature (supported by numerous tools). If export is not possible, create the footprint as per the package mechanical dimensions outlined in the product data sheet.

3.1.2 LQFP package

The VF3xx and VF3xxR processors come in a plastic 24 × 24 × 1.40 mm body with 0.5 mm lead-pitch. The "gull-wing" leads extend from each of the four sides, making it a 176-lead LQFP package.

Figure 7 and Figure 8 show the "gull-wing" array and additional package information, respectively.

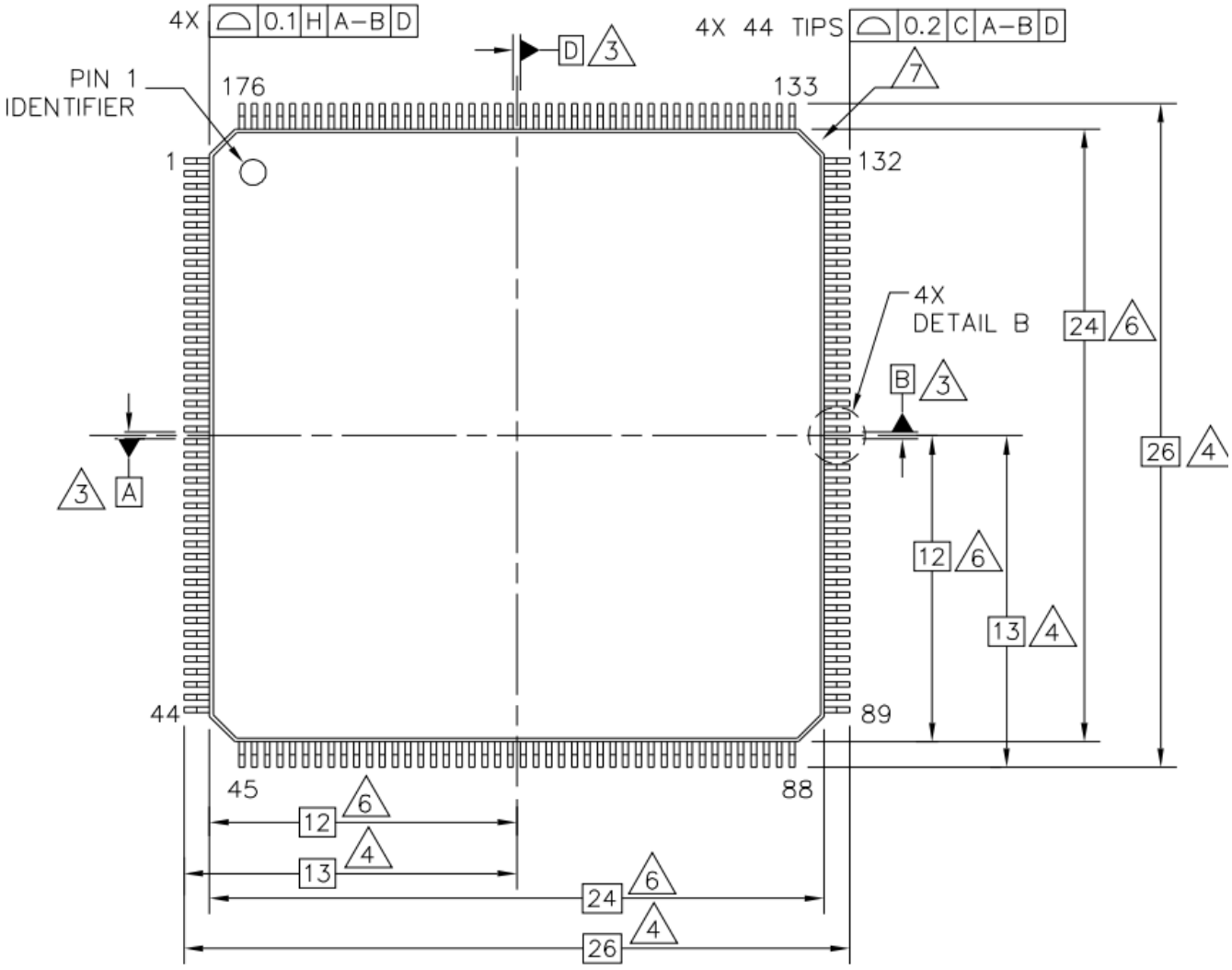


Figure 7. Vybrid LQFP "gull-wing" lead array

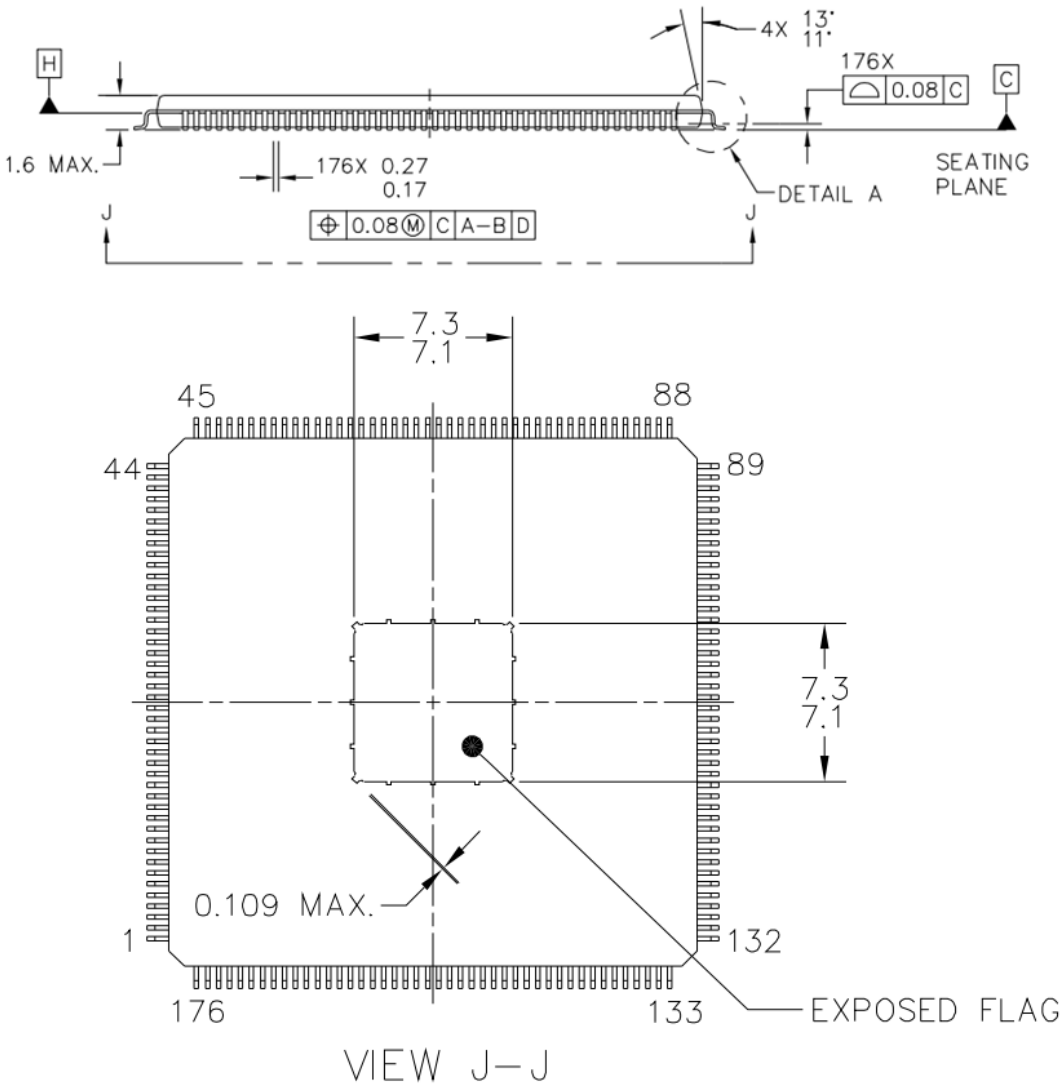


Figure 8. Vybrid LQFP package information

NOTE

The bottom exposed pad (flag) is connected to VSS (GND) internally for both electrical and thermal purposes.

NOTE

Although the VF3xx and VF3xxR processors come in the same 176-lead LQFP package type, they are not hardware-compatible due to different pinouts.

3.1.3 Fanout illustrations for Vybrid

LQFP-based layout approaches are quite straightforward, including the bottom-exposed pad's connection to the internal GND plane with numerous vias; therefore, only recommendations for the much more complex MAPBGA-based layout are provided.

Figure 9 and Figure Figure 10 show the top and bottom layer fanouts for a Vybrid chip in the MAPBGA package.

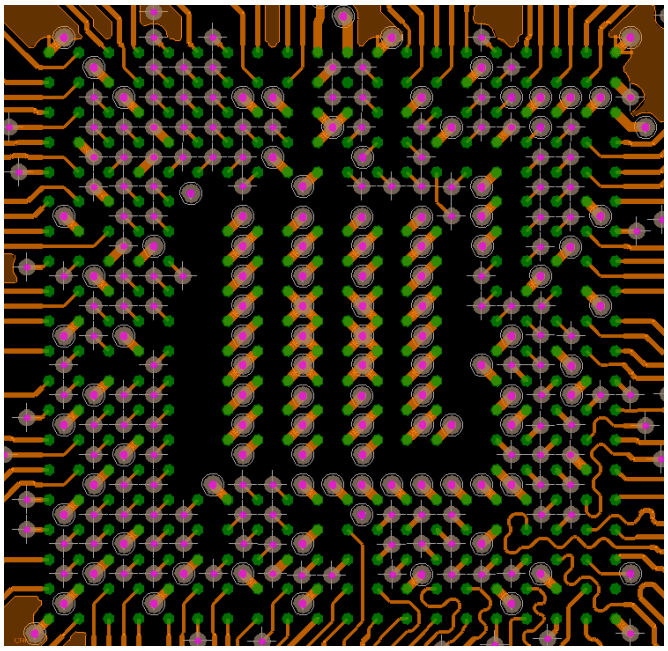


Figure 9. Vybrid MAPBGA fanout example, top layer view

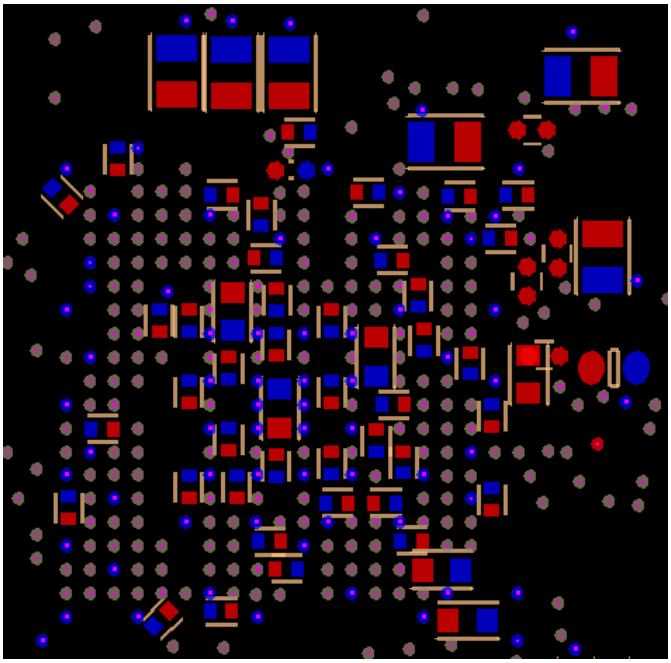


Figure 10. Vybrid MAPBGA fanout example, bottom layer view

The colors signify the following:

- top layer
  - brown = etch
  - green = pad
  - pink = vias
- bottom layer
  - blue = GND net
  - red = power rails

3.1.4 Placing decoupling capacitors

All the power-related balls used by the Vybrid core are located in the center ball-cluster, and the fanout scheme utilizes the square-shaped gap around it (see Section 3.1.1, “Mechanical data”) that facilitates placement of the bulk decoupling capacitors on the bottom side of the PCB.

The capacitors’ connections to their relevant power balls should have minimal inductance to ensure high-speed transient current demand by the processor. To meet this requirement, the small-size (for example, 0402) and bulk (for example, 0603) decoupling capacitors should be mounted as close as possible to the power vias, the recommended distance being less than 50 mils. Additional bulk capacitors may be placed near the edge of the BGA via array.

A correct via size is critical for preserving adequate routing space, the recommended via geometry being 18 and 8 mils for the pad and drill sizes, respectively.

The following list provides main recommendations for choosing the correct decoupling scheme for the boards using Vybrid in the BGA package:

- For efficient high-speed bypassing, select the smallest capacitor package size that budget and manufacturing can support for a specific application, for example, automotive.
- Use the largest capacitance value available in the package size selected, for example, 0.22 µF (at the date of publication) for the 0402 automotive-grade package.
- For each small-size capacitor, make the overall path (a sum of the “capacitor-to-via” and “via-to-Vybrid power pad” segments) as short as possible (series inductance cancels out capacitance!).
- Tie capacitors to GND plane directly with vias placed as close to their pads as possible.

The Vybrid Tower and Automotive platforms use the preferred BGA power-decoupling design. The layout data are available through www.freescale.com. Customers should use the reference design strategy for power and decoupling.

3.2 Stackup recommendations

High-speed design requires a good stackup in order to have the right impedance for the critical traces. The constraints for the trace width may depend on a number of factors, such as the board stackup and associated dielectric and copper thickness, required impedance, and required current rating (for power

traces). The Freescale reference platforms use a minimum trace width of three mils, specifically for the DDR section routing.

The stackup also determines the routing and spacing constraints.

Consider the following when designing the stackup and selecting the board material:

- Board stack-up is critical for high-speed signal quality.
- Impedance of critical traces must be pre-planned.
- High-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- Freescale development platforms use Isola 370HR.
- Freescale validation boards use Isola FR408.

3.2.1 Stackup examples

Figure 11 and Table 18 show the Freescale Vybrid Tower module documentation data provided in the 8-layer fabrication Gerber file.

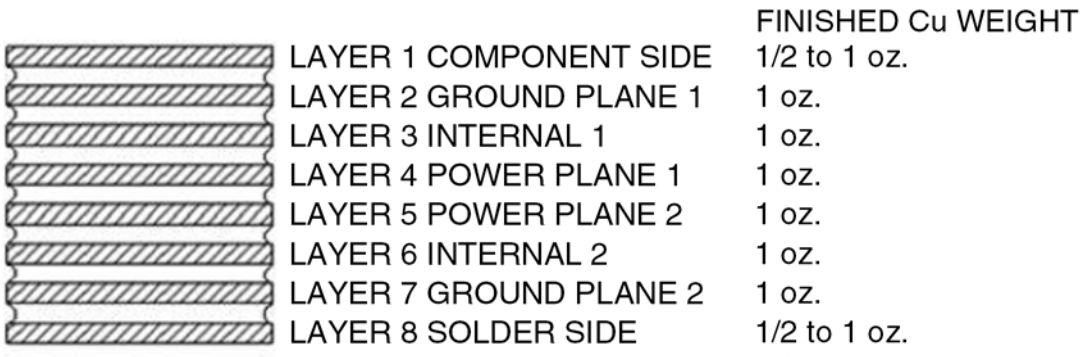
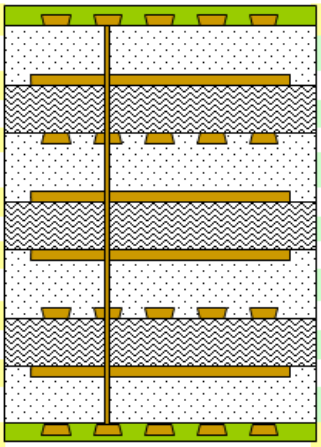


Figure 11. Vybrid Tower module stackup drawing from Freescale documentation

Table 18. Vybrid Tower module stackup table from Freescale documentation

Layer No. /Name	Single-ended		Differential 1			Differential 2		
	Trace width (mils)	Impedance	Trace width (mils)	Trace spacing (mils)	Impedance	Trace width (mils)	Trace spacing (mils)	Impedance
1/TOP	6.4	50	6.5	14.3	90	5.0	12.8	100
3/INT1	6.5	50	6.4	14.3	90	5.0	12.8	100
6/INT2	6.5	50						
8/BOT	6.4	50	6.5	14.3	90	5.0	12.8	100

Figure 12 and Table 19 show the Vybrid Tower module data provided by the PCB-fabrication company.



Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	1.9	0.333			Foil, 0.5 oz reduce to 0.333 oz
			4.15	3.62	Prepreg 370HR 3313
2	1.2	1			
			4.25	5.00	Core 370HR 5mils 0.5 oz / 1 oz
3	0.6	0.5			
			4.00	5.04	Prepreg 370HR 1080/1080
4	1.2	1			
			4.40	24.00	Core 370HR 24mils 1 oz / 1 oz
5	1.2	1			
			4.00	5.04	Prepreg 370HR 1080/1080
6	0.6	0.5			
			4.25	5.00	Core 370HR 5mils 0.5 oz / 1 oz
7	1.2	1			
			4.15	3.62	Prepreg 370HR 3313
8	1.9	0.333			Foil, 0.5 oz reduce to 0.333 oz

Layers	Drill Type		
1 - 8	PTH	61.12	Thickness over Copper
		62.52	Thickness over Soldermask

Figure 12. Vybrid Tower module stackup drawing from PCB-fabrication company

Table 19. Vybrid Tower module stackup table from PCB-fabrication company

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (± ohms)	Target Linewidth (mils)	Edge-Coupled Pitch [1] (mils)	Reference Layers	Modeled Linewidth (mils)	Modeled Impedance (ohms)
1	Single-Ended	Yes	50.00	5	0.00		(2)	5.50	49.89
1	Edge-Coupled Differential	Yes	90.00	9	5.10	10.30	(2)	4.70	90.50
3	Single-Ended	---	50.00	5	5.00		(2, 4)	4.20	50.18
3	Edge-Coupled Differential	---	90.00	9	5.20	12.20	(2, 4)	4.80	90.17
3	Edge-Coupled Differential	---	100.00	10	4.30	13.30	(2, 4)	4.00	100.16
6	Single-Ended	---	50.00	5	5.00		(5, 7)	4.20	50.28
6	Edge-Coupled Differential	---	90.00	9	5.20	12.20	(5, 7)	4.80	90.17
6	Edge Coupled Differential	---	100.00	10	4.30	13.30	(5, 7)	4.00	100.16
8	Single-Ended	Yes	50.00	5	0.00		(7)	5.50	49.89
8	Edge-Coupled Differential	Yes	90.00	9	5.10	10.30	(7)	4.70	90.50

[1] Edge-Coupled Pitch is measured between centerlines of the two differential-pair traces.

3.3 Routing recommendations

3.3.1 Crystal circuitry recommendations

A solid ground plane must be directly under the crystal circuitry, including the associated components and traces.

3.3.2 High-speed routing recommendations

Provided in this section are routing recommendations for high-speed signals, for example the DDR, USB, MAC, or graphic display ones.

3.3.2.1 Generic requirements

Apply the below good-practice rules to all high-speed signals:

- Route them with higher priority than low-speed signals.
- Control impedance of the involved traces.
- Do not cross-split reference planes during the routing.
- Avoid creating slots, voids, and splits in reference planes; verify that via voids do not create such splits (space-out vias).
- Avoid having layer transitions.
- If layer transition is inevitable:
  - Try staying within the same reference plane (just referenced to the opposite side thereof).
  - Make sure the trace impedance does not change after the layer transition.

3.3.2.2 Synchronous-interface routing requirements

Additional requirements are applied to synchronous interfaces:

- Control the bus propagation delay by verifying the length matching, including that with respect to the clock trace.
- To reduce crosstalk, provide at least 2.5 × spacing (2.5 × height from the reference plane) from any adjacent trace for all the clock or strobe signals that are on the same layer.

3.3.2.3 SD card interface requirements

Follow the below rules for the SD card connection:

- Match Data and Command trace lengths (length delta depends on the specific bus rate).
- The Clock trace should be longer than the longest trace in the Data / Command group (+ 5 mils).
- SD card interface layout requirements are very similar to those for the DDR one (see Section 3.5, “DDR routing rules”).

3.3.3 Ground plane recommendations

This section provides examples of good practices and explains how to avoid common mistakes when creating ground planes.

The following two figures show common examples of poor ground planes. The copper plane is represented by the gray color in Figure 13 and by the horizontal green lines in Figure 14.

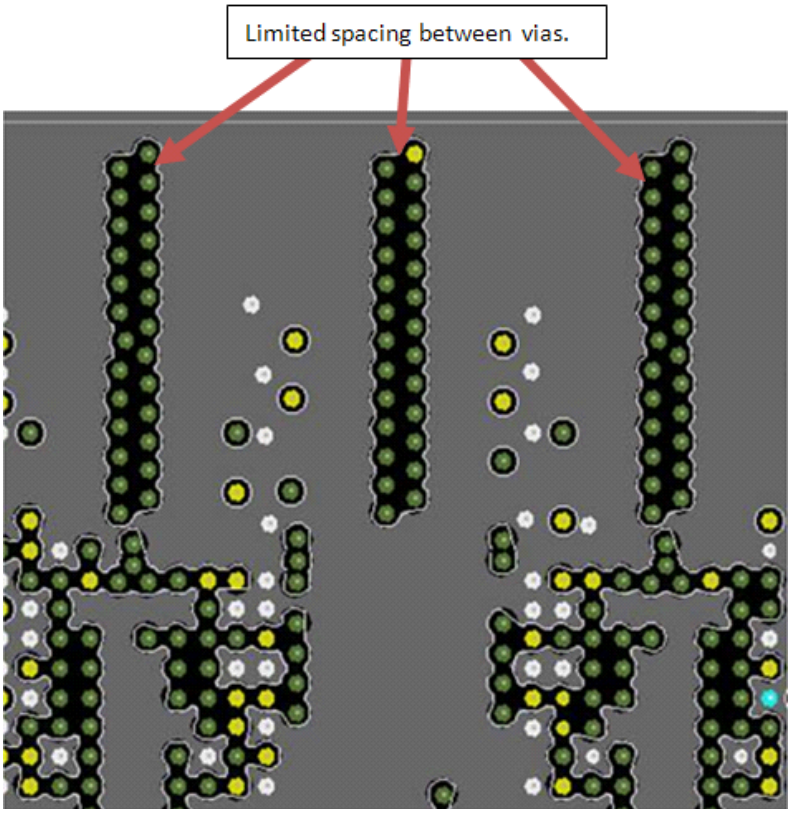


Figure 13. Poor GND plane, example 1

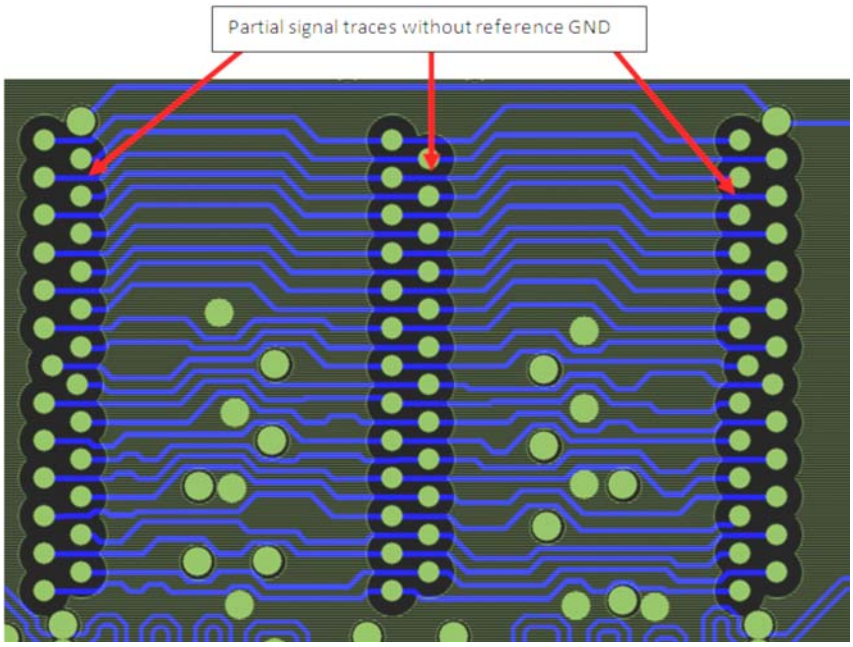


Figure 14. Poor GND plane, example 2

Spacing the vias some mils apart facilitates the ground copper flowing in the plane. The following figures show good practices of ground planes.

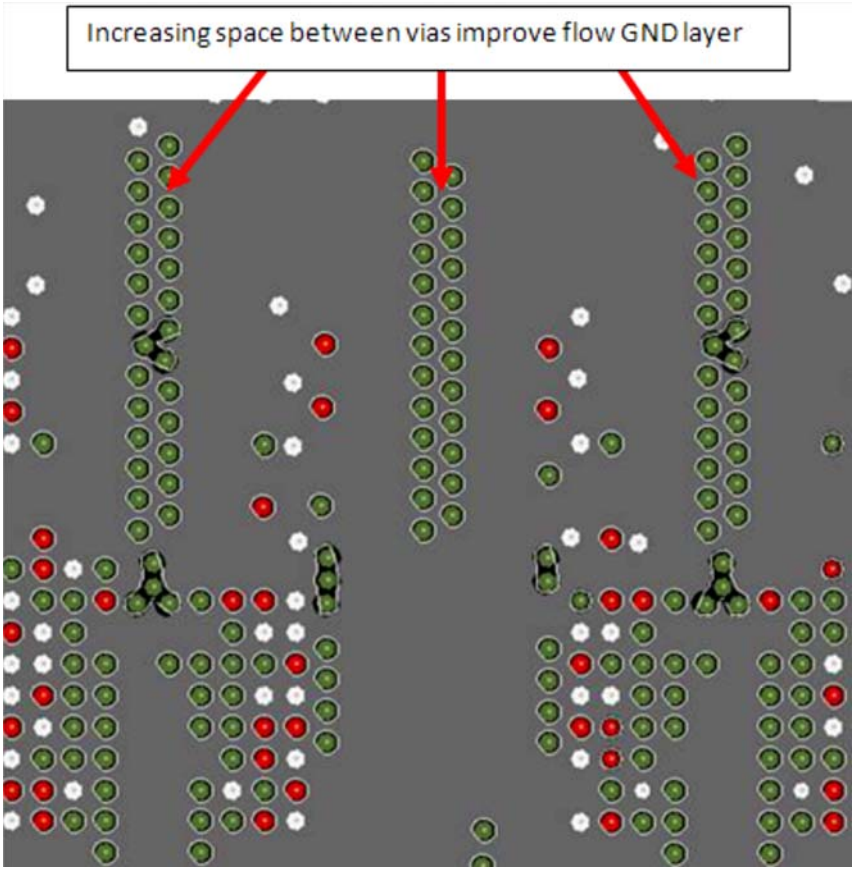


Figure 15. Good layout GND plane detail, example 1

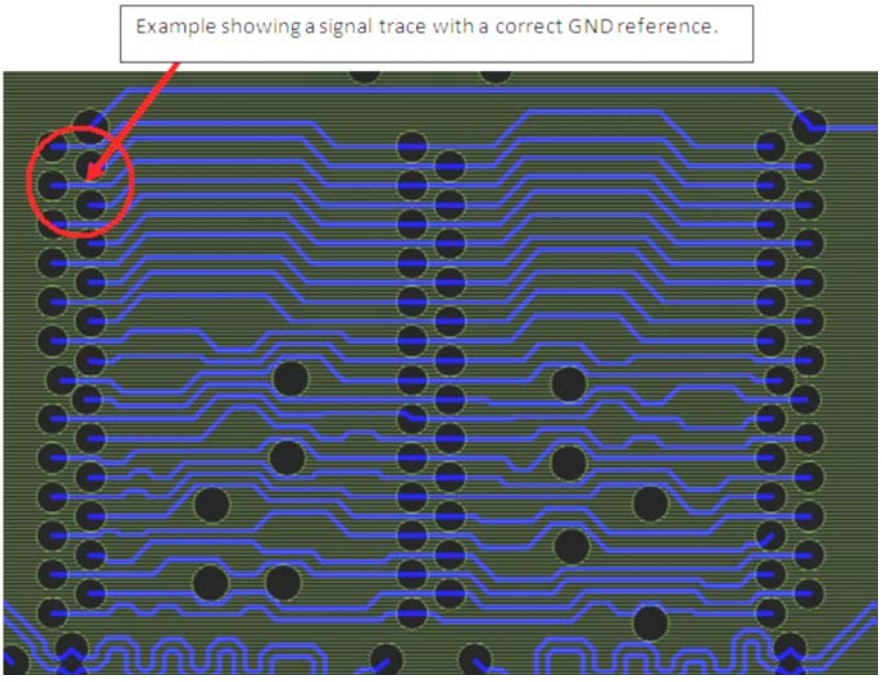


Figure 16. Good layout GND plane detail, example 2

3.4 DDR connection information

Only Vybrid versions in the MAPBGA package have a DDR interface, the block diagrams are shown in Figure 17 and Figure 18 for the DDR3 and the LPDDR2 cases, respectively.

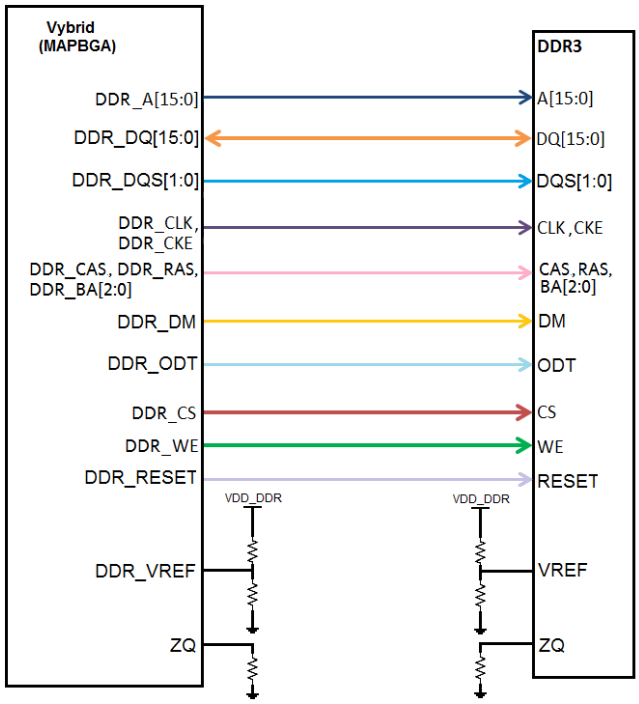


Figure 17. Vybrid DDR3 connections

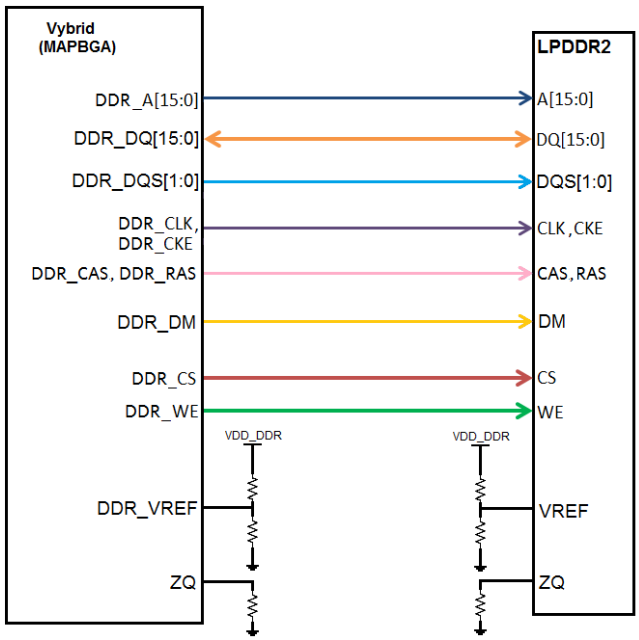


Figure 18. Vybrid LPDDR2 connections

The traces must have controlled impedance; 50 Ω for the single-ended ones and 100 Ω for the differential pairs.

Figure 19 shows the physical DDR placement scheme – the DDR3 memory IC itself and its decoupling capacitors. The green and red figures show the top and the bottom layer, respectively.

It is very important to place the memory as close to the processor as possible to reduce trace capacitance and keep the propagation delay to the minimum. Follow the reference board layout as a guideline for memory placement and routing.

Since the DDR interface is one of the most critical ones for chip routing, it is strongly recommended to verify its robustness with the DDRv design aid (see Section 6.2, “DDRv design aid”).

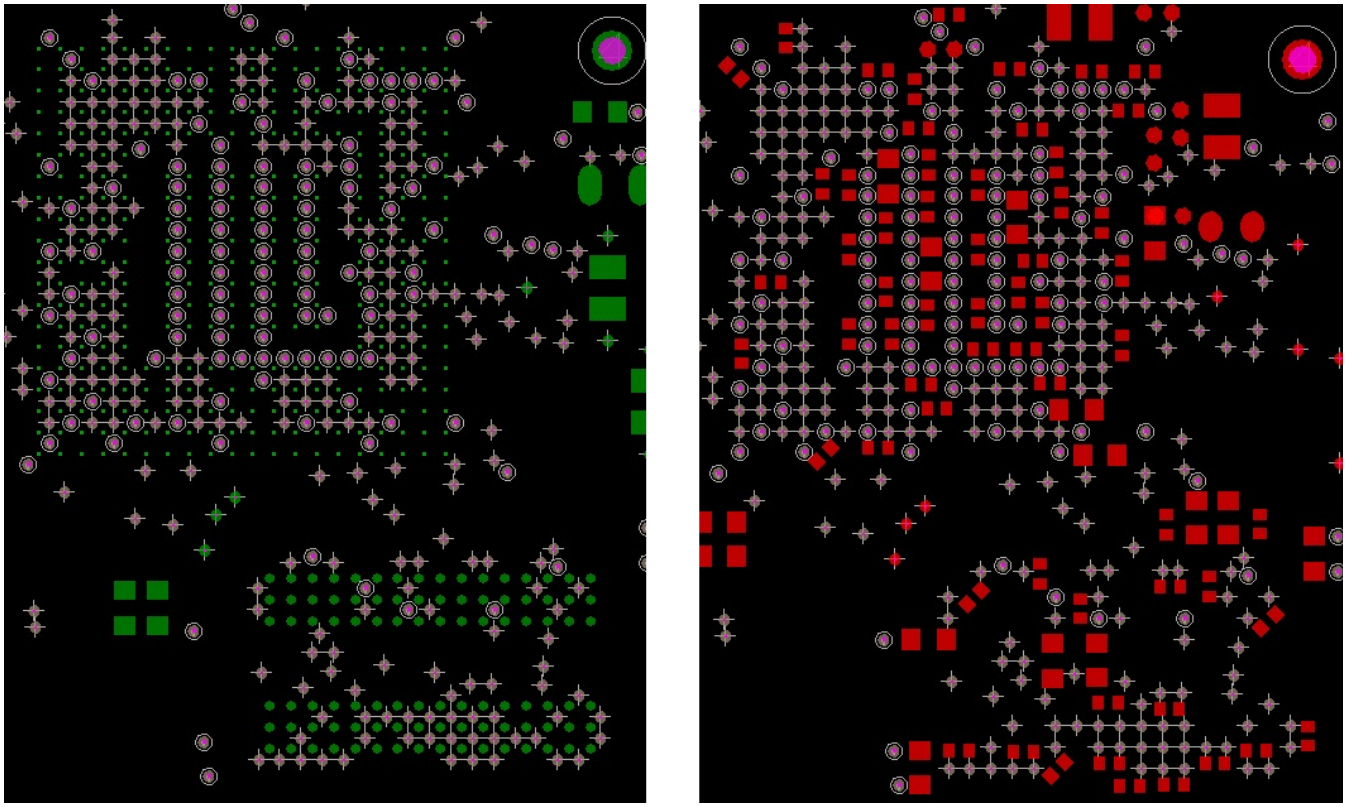


Figure 19. Placement of DDR3 memory IC and its decoupling capacitors

3.5 DDR routing rules

Although demonstrated on the DDR3 example, the approach is applicable in the LPDDR2 case as well.

DDR3 routing can be accomplished in two different ways; either routing all signals at the same length or routing by byte group.

3.5.1 Same-length routing

Routing all signals at the same length can be more difficult at first because of the tight space between the DDR and the processor and the large number of required interconnections. However, it is a better way because it makes signal-timing analysis straightforward. Ideally, one could route all the signals at the same length; however, it could be difficult because of the large number of connections in the tight space between the DDR IC and the processor.

Table 20 explains the rules for routing the signals by the same trace length.

Table 20. DDR3 routing by the same length

Signals	Reference length	Recommendations
Clock DDR_CLK (differential pair)	3 inches	---
Address and Bank	Clock trace length	Match ± 25 mils of the value specified in the reference length column.
Data		
Control signals		
DDR _DQS (each differential pair)		Match ± 10 mils of the value specified in the reference length column.

3.5.2 By-byte group routing

Routing by byte group requires better control of the signals of each group. It is also more difficult for analysis and constraint settings. However, its advantage is that the constraint to match lengths can be applied to a smaller group of signals. This is often more achievable once the constraints are properly set.

Table 21 explains the rules for routing the signals by byte group.

Table 21. DDR3 routing by byte group

Signals	Group	Reference length		Recommendations
		Min.	Max.	
Clock DDR_CLK (differential pair)	Clock	As short as possible	2.25 inches	---
Address, Bank, CAS, RAS, WE	Address and Command	Clock (min) – 200 mils	Clock (min) [1]	Match the signals ± 25 mils.
Lower Data Byte, DQS0 (differential pair), DQM0	Byte Group 0	---		Match the signals of each byte group ± 25 mils. Match the differential signals of DQS ± 10 mils.
Upper Data Byte, DQS1 (differential pair), DQM1	Byte Group 1	---		
CS, CKE, ODT	Control signals			Match the signals ± 50 mils.

[1] Clock (min) – the shortest length of the clock-group signals (because this group has a ± 5 mil matching tolerance)

3.6 DDR routing considerations

Vybrid can handle up to 1 GB of DRAM memory. The DDR routing needs to be separated into three groups: data, address, and control; each of them having its own method of routing.

When applicable, the Vybrid DDR controller provides address mirroring, which aids address line routing for the memory IC placed on any side of the board.

3.6.1 Termination-less topology considerations

Be sure to take into account the following when designing this topology:

- the routing rules described in Table 21 need to be followed
- termination resistors are not required
- the traces need to be as short as the board layout permits and no longer than one inch, ideally within 800 mills and 600 mills for the data and clock traces, respectively (for example see Table 22)
- on-chip drive-strength control

3.6.2 Fly-by topology considerations

The classic fly-by topology, thanks to its bus-termination resistors, is recommended for use in cases where distance between the processor and the DDR memory cannot be minimized. Since the memory controller balls are placed on the Vybrid package corner for easy connection to a memory chip, it is hard to imagine the case when the termination-less topology is impossible to implement, and the fly-by topology is not detailed in this document.

3.6.3 Routing examples

The figures in this section show examples for the DDR3 interface routing. Figure 20 and Figure 21 are guidelines for the termination-less configuration routing on an 8-layer PCB.

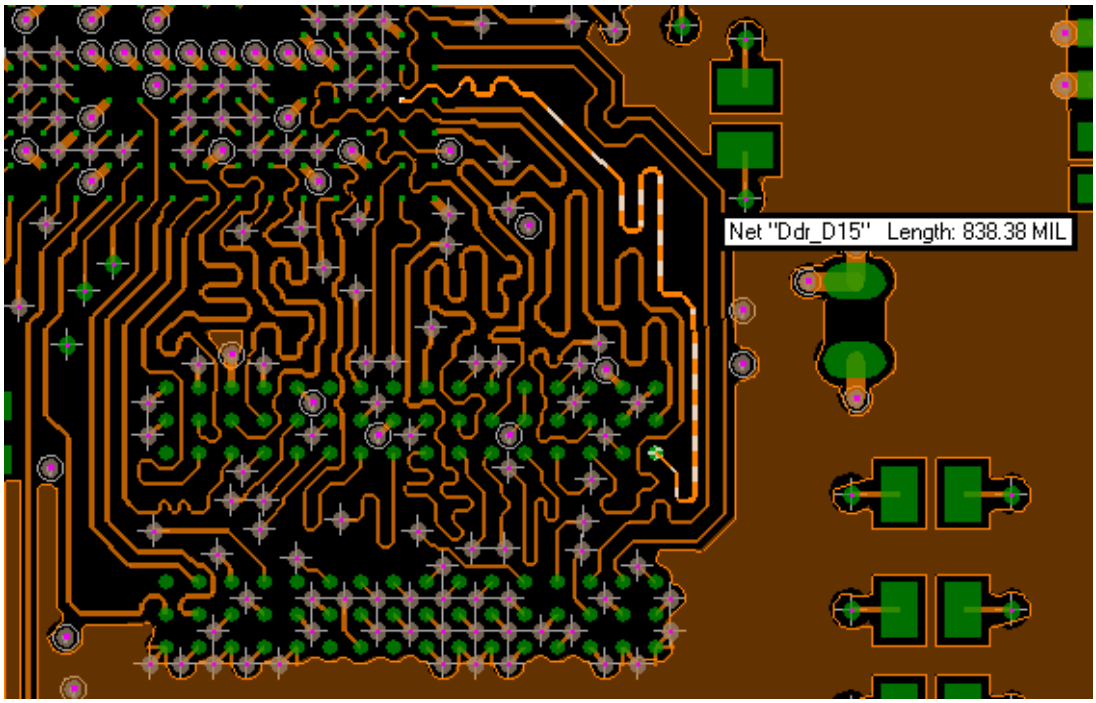


Figure 20. Top layer DDR3 routing

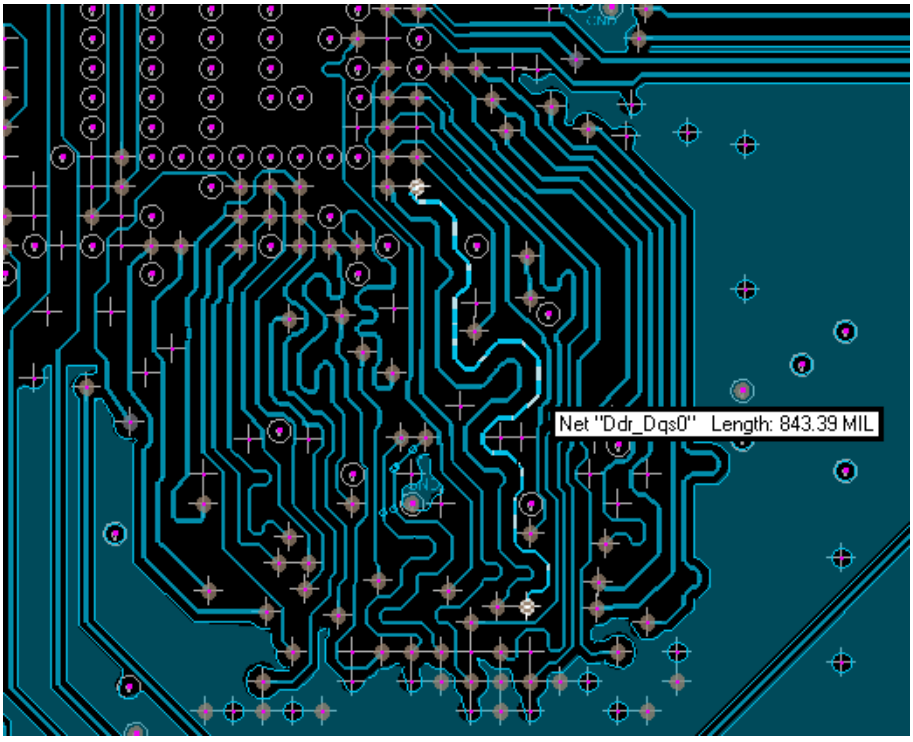


Figure 21. Internal L3 (INT1) layer DDR3 routing

Table 22 shows the total etch of the signals for the byte zero and byte one groups. The layout is an example of applying the Table 21 recommendations:

- Approximately 845-mil length for the data-related traces
- Approximately 640-mil length for the clock

Table 22. Total signal etch (DDR3) of Vybrid Tower module

DDR_D0	841.1
DDR_D1	840.1
DDR_D2	841.9
DDR_D3	847.0
DDR_D4	839.2
DDR_D5	843.9
DDR_D6	840.2
DDR_D7	844.0
DDR_D8	838.5
DDR_D9	841.7
DDR_D10	841.5
DDR_D11	842.7
DDR_D12	842.2
DDR_D13	841.2
DDR_D14	840.1
DDR_D15	838.4
DDR_DQM0	843.4
DDR_DQM1	841.9
DDR_DQS0	843.4
DDR_DQS1	845.2
DDR_DQS0_B	847.1
DDR_DQS1_B	845.8
DDR_CLK	640.3
DDR_CLKB	639.9

3.6.4 VREF recommendations

Apply the following rules to the DDR voltage reference net (see Figure 22):

- Use a minimum of 30-mil trace between the VREF source and the destinations.
- Maintain a 25-mil clearance from the adjacent nets.
- Isolate VREF and / or shield with GND.
- Have one 0.1 to 0.22 µF capacitor atached to GND in each of the three locations – on the VREF source, the Vybrid controller, and the DDR memory device.

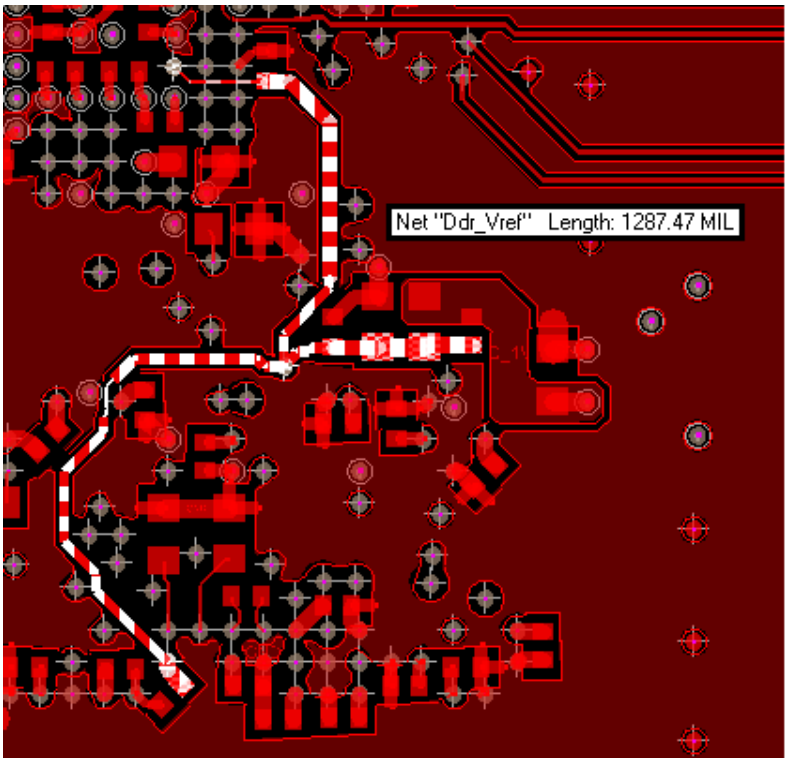


Figure 22. Bottom layer DDR3 routing (VREF only)

3.6.5 ZQ recommendations

The ZQ pad resistor and its connection (as short as possible), should be placed away from noisy regions. Noise induced into it may impact the internal circuit and degrade the interface signals.

3.7 USB differential-signal recommendations

Use below recommendations for the high-speed DP / DM (a.k.a. D+ / D–) pair:

- Assign it higher routing priority than the USB power.
- Rate it for differential impedance of 90 Ω .
- For lower signal attenuation, minimize its length.
- For lower signal attenuation, route it on top or bottom layer, over a homogeneous ground plane.
- Length-match the DP / DM traces to ± 5 mils.
- Do not use ferrite beads on this high-speed pair but a common-mode choke (ideally, approved for USB use) and place it as close to the USB connector as possible. All this prevents excessive radiated emission of a plugged-in USB cable; however, with good PCB layout, filtering should not be required.
- Apply standard high-speed differential-routing rules for signal integrity:
  - Route it with a minimum number of corners; if inevitable, round them or at least use 45-degree, not 90-degree turns.
  - Avoid running it over any reference plane interruptions like slots, anti-etch, or clearouts around the USB connector pins.
  - Avoid running it under oscillator circuits.
  - Minimize running in parallel to Clock and / or Data-bus traces.
  - Avoid having impedance disturbances like layer changes (that means vias), stubs, or branches.

3.8 LVDS recommendations

Use below recommendations for the LVDS lines:

- Rate it for differential impedance of 100 Ω .
- Apply the same rules as for a differential USB signal listed in Section 3.7, “USB differential-signal recommendations”, except for radiated-emission filtering not needed for a signal not leaving the board.

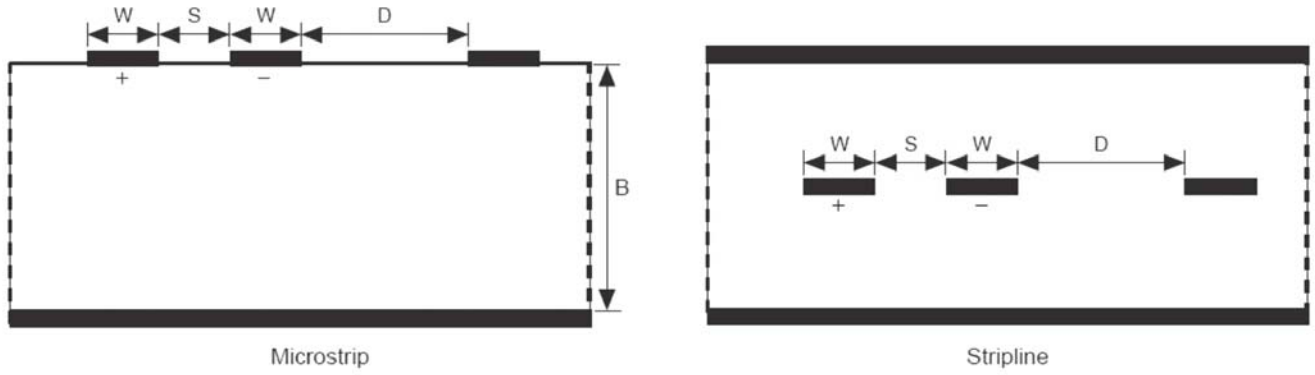
3.9 Impedance signal recommendations

Use the Table 23 data to define PCB constraints on the layout design stage.

Table 23. Impedance signal recommendations

Signal Group	Style	Impedance Value, (ohms)	Impedance Value tolerance (± %)
All signals, unless specified	Single-ended	50	10
USB	Differential	90	
Other than CAN and USB: LVDS, MLB, Ethernet, and so on	Differential	100	
CAN	Differential	120	

Figure 23 shows two differential pair topologies – microstrip and stripline.



For better coupling within a differential pair, make S < 2W, S < B, and D = 2S where:

W = width of a single trace in a differential pair
S = space between two traces of a differential pair
D = space between two adjacent differential pairs
B = thickness of the board

Figure 23. Microstrip and stripline differential pair dimensions

Routing of multiple differential pairs is shown in Figure 24. To avoid crosstalk, the space between the two adjacent differential pairs should be at least twice the space between individual conductors of the pair.

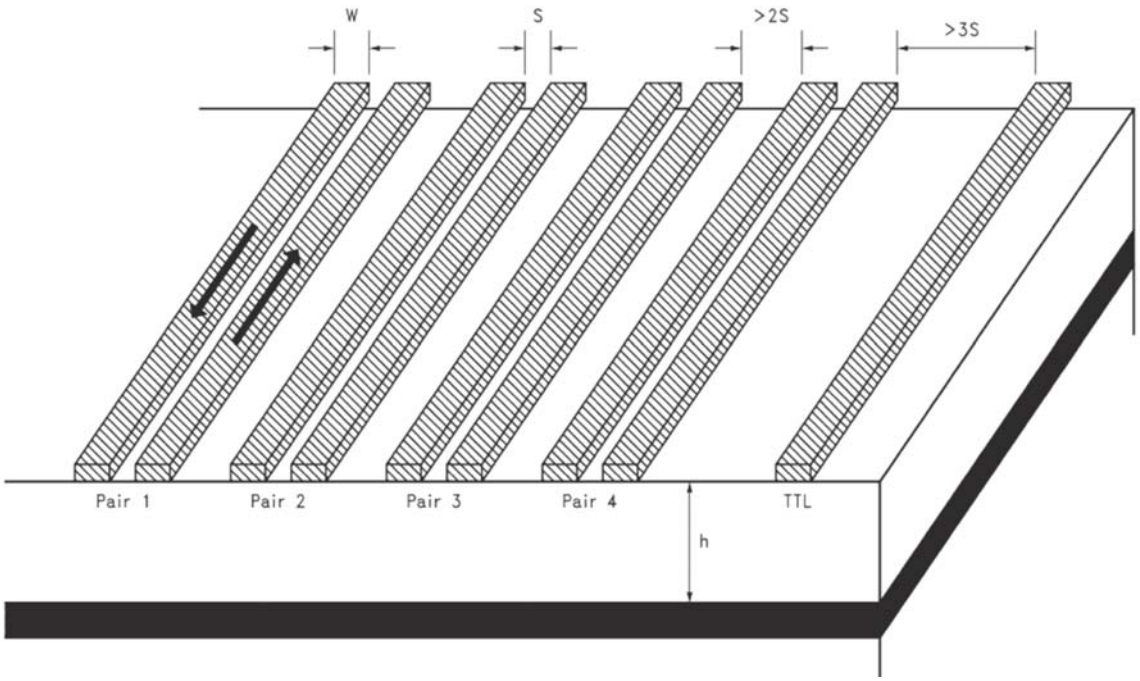


Figure 24. Differential pair routing

3.10 EMI / EMC recommendations

3.10.1 General recommendations

Where a device has a metal chassis (usually connected to Earth ground), to prevent both ESD and emission problems, components with metal shields (connectors, push buttons, and so on) should have their shields connected to the device chassis, either directly or via the PCB.

Even with all the measures taken, EMI / EMC test results are not easy to predict; therefore, it is recommended to start with the worst-case EMI / EMC protection scheme and simplify it later if the test results allow for that.

3.10.2 Radiated emission reduction

Sufficient number of layers (minimum of six, more realistically eight) is recommended to provide all the high-speed signals with solid reference planes.

Each net connecting to an external cable, including power and GND, should have series ferrite beads placed as close to the PCB connector as possible.

NOTE

Types with a minimum impedance of 500 Ω at 100 MHz are recommended, compromise being possible for a USB 5 V rail due to the high DC current rating.

Details on treating the differential USB signal are provided in Section 3.7, “USB differential-signal recommendations.”

Ethernet ports do not need additional emission reduction – all standard Ethernet magnetic modules already have built-in common-mode chokes.

3.10.3 Connection between USB connector shield and signal GND

Special attention must be paid to the connection between the board signal GND and the USB connector shield. It is recommended to not connect them directly but through an RC filter instead (see Figure 25), which prevents turning the USB cable shield into a radiating antenna. The resistor provides a DC path, whereas the capacitor provides a high-frequency one.

To minimize the USB signal noise while providing EMI / EMC compatibility, the resistance and capacitance values in a specific design have to be selected. Their range may be quite wide – from 100 Ω to 1 MΩ and from 27 pF to 4700 pF, respectively (as per discussions on the Internet engineering forums).

The Freescale designs use the 100 Ω and the 1000 pF to 2200 pF values. The lower the resistance value is, the lower the voltage drop caused by the ESD current is, which allows for using a capacitor rated for a relatively low voltage (and definitely not higher than a few hundreds of volts the USB cable itself can withstand).

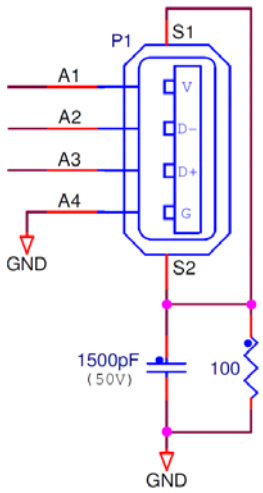


Figure 25. Connection between USB connector shield and signal GND

3.11 ESD damage prevention

3.11.1 Protecting board

To prevent the PCB damage while dealing with it (production, repair, and so on), it is recommended to have an “ESD Guard Ring” – about 100-mil wide exposed (that is no solder mask) copper along the board edge with numerous vias to GND at least 400 mils apart.

3.11.2 Protecting ports

The most optimal protection scheme is that in which a signal comes from the connector through the series ferrite beads to a voltage-clamping device. Having a non-zero ferrite bead impedance limits the ESD peak current flowing through the voltage-clamping device, which in turn lowers the clamped voltage value (beneficial for the protected net) and extends the clamping device's life.

3.11.2.1 Protecting USB ports

Even though Vybrid embeds on-chip ESD protection on the DP, DM, and VBUS lines, it is recommended to enforce it by using external transient-suppressing components and place them as close to the USB connector as possible to reduce the potential discharge path and discharge propagation on the PCB. These protection components may either be integrated special-purpose devices or independent, discrete devices.

The integrated devices, like that in Figure 26, are very common. Unfortunately, although using the right topology, quite many of them are based on built-in 5 V TVSs, and it is unclear how such devices might be recommended for protecting the DP and DM inputs of a 3.3 V powered device usually tolerating levels up to 3.8 V (5.25 V for VBUS).

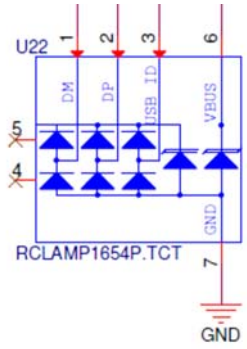


Figure 26. Integrated ESD protection device example

The optimized solution shown in Figure 27 uses the same topology but differs in that there are two TVS voltage ratings – 3.3 V for the signal lines (DP, DM, and ID) and 5 V for VBUS. The solution might be implemented either as a single integrated device or using discrete complements.

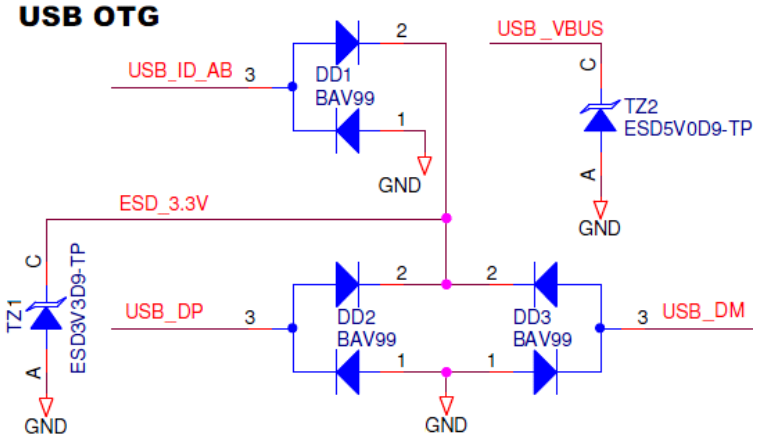


Figure 27. Optimized ESD protection topology

3.12 Component placement recommendations

Adhere to the following recommendations when placing components:

- Place components in a way that short and / or critical routes can be easily laid out:
  - critical routes determine component location
  - orient devices to facilitate routes (minimize length and crossovers)
- Consider placing the following pairings adjacent:
  - processor and DDR
  - ethernet PHY and associated connector
  - connector and codec input
  - RF block (for example, Bluetooth™) and antenna

3.13 Reducing skew and phase problems in differential-pair traces

Differential-pair technology has evolved to require more stringent checking in the area of phase control. This is evident on the higher data rates associated with parallel buses such as DDR, LVDS, or Ethernet. In the simplest terms, differential-pair technology sends equal-level and opposite-phase signals down a pair of traces. Reducing skew to keep these two opposite signals in phase is essential to assure that they function as intended.

The upper differential pair in Figure 28 shows an example of static routing where a match is achieved without needing to tune one side of the differential pair, whereas the lower one in it as well as the differential pair in Figure 29 both have the delay addition to the shorter pair side (in the green boxes) to avoid length mismatch.

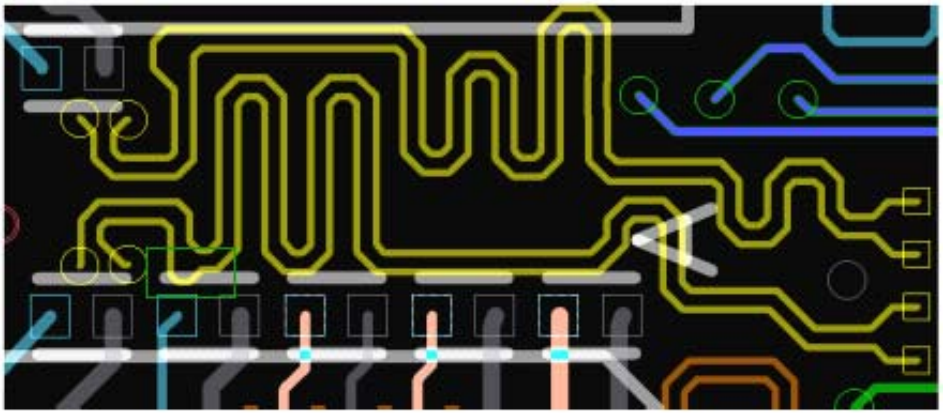


Figure 28. Two differential pairs – with and without delay added to shorter side

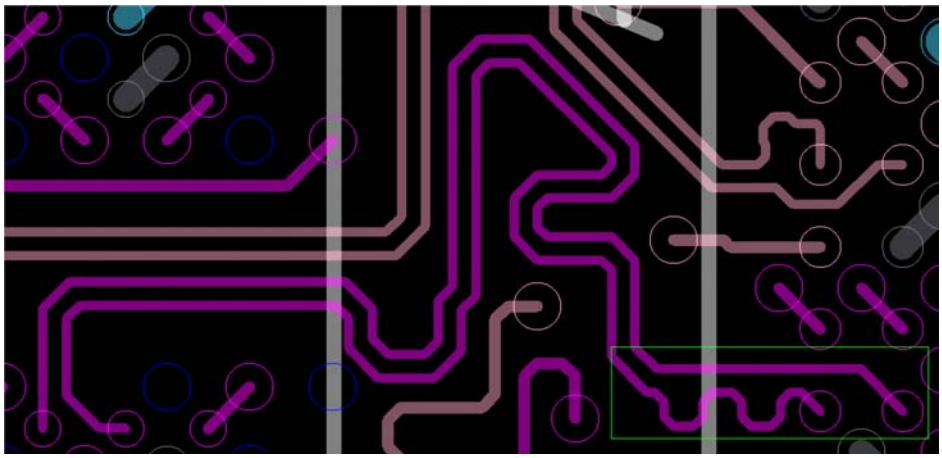


Figure 29. Differential pair with delay added to shorter side

4 Requirements for Power Management

4.1 Voltage domains

The Vybrid device has multiple voltage domains that must be supplied with different and properly sequenced voltages. Table 24 provides this information for the 364-ball BGA case; in the 176-lead LQFP case, the irrelevant domains should be ignored.

Table 24. Power sequencing

Vybrid power domain	Board-level power source	Power-up order
VDD33_LDOIN	VDD33	1
VDDREG		
VDD33		
VDDA33_ADC	VDDA33_ADC	
VREFH_ADC	VREFH_ADC	
VDDA33_AFE	VDDA33_AFE	
VDD12_AFE	VDD12_AFE	2
VDD	VDD	
USB0_VBUS	USB0_VBUS	Don't care
USB1_VBUS	USB1_VBUS	
VBAT	VBAT	
SDRAMC_VDD1P5	SDRAMC_VDD1P5[1]	

[1] If used for the processor core power, see additional board-level timing requirement in Section 4.2, “Processor core power.”

NOTE

There are no sequencing restrictions among supply pins with the same power-up order number.

NOTE

If no DDR is used, the SDRAMC_VDD1P5 pins may be left floating.

NOTE

The power-down order is opposite to the power-up order.

It is advantageous that Vybrid has been designed to use a single 3.3 V power source (VDD33 from Table 24), the rest of the device domains being powered from its fully controlled built-in linear regulators.

4.2 Processor core power

The flipside of the purely linear approach is quite low voltage-conversion efficiency. For example, it causes significant heat dissipation on the linear regulator serving the power-hungriest processor core (VDD) domain, especially at high current values. Due to that, an external ballast NPN transistor is used in this regulator, whose simplified topology is shown in Figure 30.

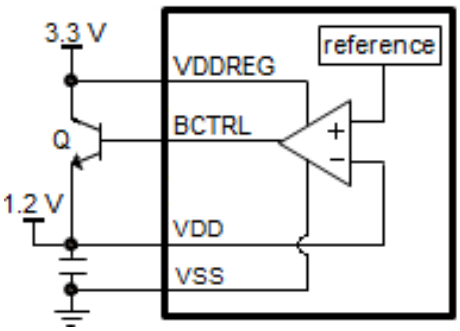


Figure 30. Simplified topology of VDD voltage regulator

To decrease heat dissipation (thus improving the voltage-conversion efficiency), the transistor collector may be powered from a source lower than 3.3 V, for example 1.5 V available in the system configuration using a DDR3 memory device. The only timing requirement in this core-powering scheme is that the transistor collector voltage shall appear no later than signal on its base connected to Vybrid BCTRL (base-control) pin, otherwise its output current exceeds the maximum value of 20 mA. The most reliable way to meet this new requirement is to turn on 1.5 V on the board prior to 3.3 V, which alters the single-rail Vybrid power sequencing shown in Table 24.

Refer to the *AN4807 – "Vybrid Power Consumption and Options"* application note for details.

The Vybrid reference designs offer both 1.5 V and 3.3 V options (see Figure 31).

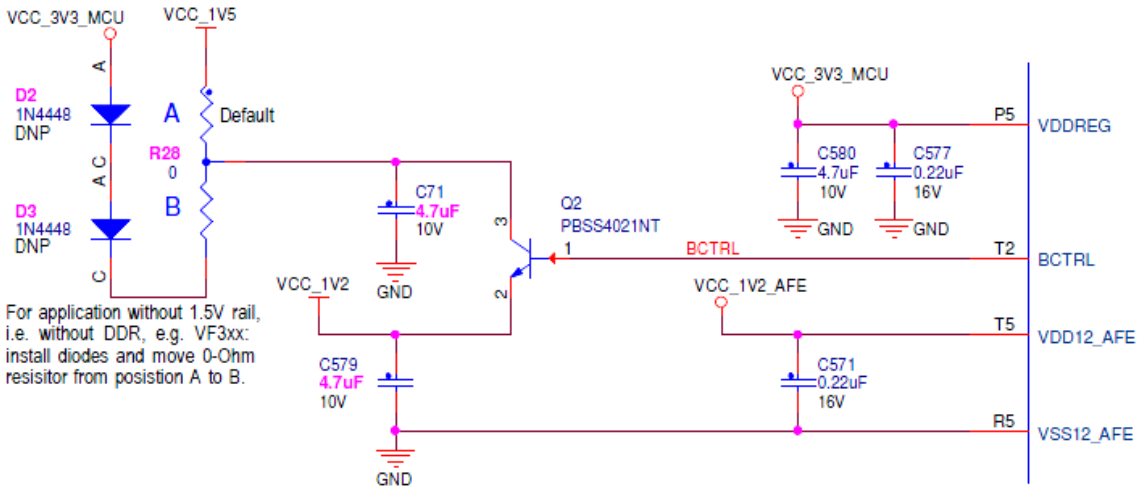


Figure 31. VDD voltage regulator in reference design

4.2.1 Transistor type selection

The Vybrid data sheet requirements for proper ballast NPN transistor type selection are applicable to the collector voltage down to 1.8 V.

If lower value is used, for example 1.5 V, the following method, based on the transistor operation theory (and using its terminology), shall be applied while selecting the transistor type:

- For the application of interest, with its known operating temperature range and highest I_c, select a transistor candidate with a linear-region Hfe of 100 to 150 (quite common for inexpensive NPN transistors nowadays) or higher.
- With high I_c, I_b is usually quite high and drives V_{be} up to 1 V or even higher; with V_{ce} of 0.3 V (that is V_c of 1.5 V), the transistor operates in the saturation region, that is the base-collector junction is forward-biased and "steals" part of I_b, so that Hfe degrades (this is why a relatively high linear-region Hfe is required).
- Based on I_c and Hfe (from the transistor data sheet for this I_c value), I_b is calculated.
- Based on I_b and the transistor data sheet, V_{be} is defined.
- Based on V_{be} and the transistor data sheet, the lowest possible V_{ce} is defined, which in turn defines the lowest possible V_c.
- Based on I_c and V_{ce}, the heat dissipation is calculated and checked against the transistor data sheet.

Applying this method is easier with a higher linear-region Hfe for the following reasons:

- It guarantees lower I_b ==> lower V_{be} ==> less deep saturation ==> lower Hfe degradation.
- Even with degraded Hfe, I_b does not exceed 20 mA (the maximum Vybrid BCTRL output current).

If a specific transistor candidate appears to have a sufficient V_{ce} margin, it is possible to:

- Keep V_c and try a transistor candidate with lower linear-region Hfe, usually less expensive.
- Keep Hfe and lower V_c, which in turn:

— decreases heat dissipation
— saves power
— improves voltage-conversion efficiency
— allows switching to a smaller transistor case, less expensive and occupying less space on the board

NOTE

Even for the above-mentioned V_c of 1.8 V, the collector-base junction is already somewhat forward-biased, but the "I_b-stealing" effect is still negligible.

4.3 Analog power rails

Each of the four analog rails, VDD12_AFE, VCC_3V3_AFE, VCC_3V3_ADC, and VREF_3V3, has two powering options (see Figure 32):

- The cost-efficient option (default in our reference designs) – through a filtering ferrite bead from the relevant main power rail.
- The more expensive option when high-quality AFE, ADC, and DAC performance is required – from a dedicated linear voltage regulator.

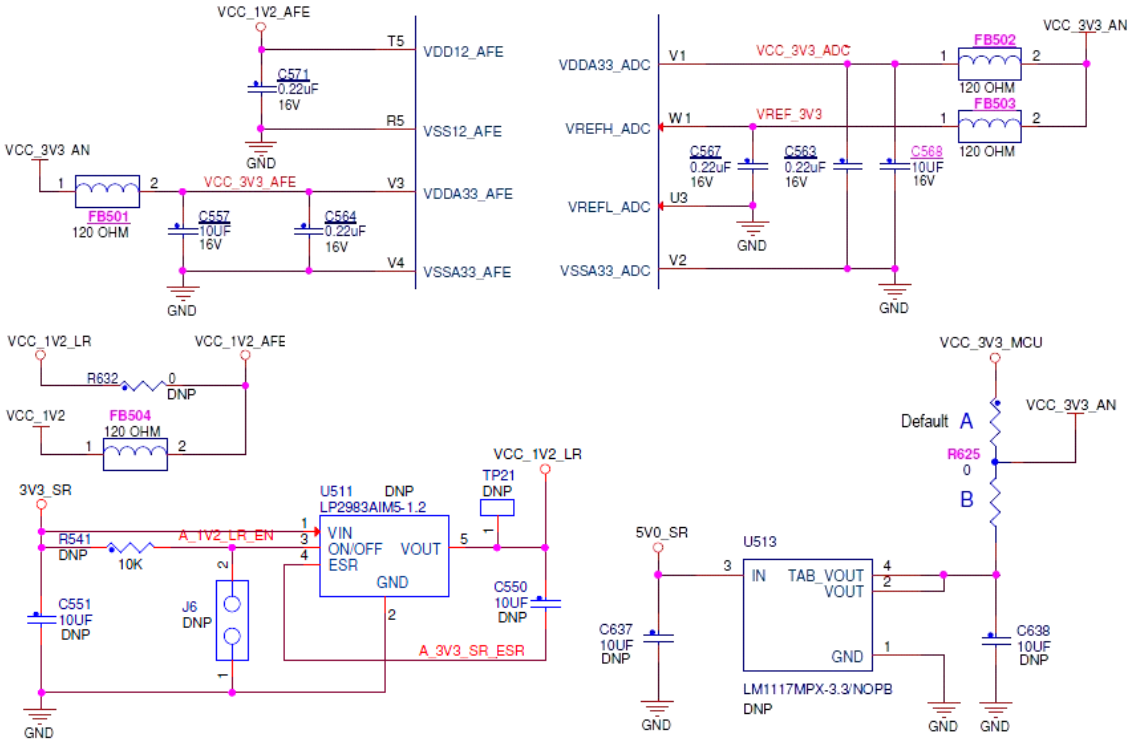


Figure 32. Powering options for analog power rails

4.3.1 AFE block power consumption

While selecting linear voltage regulator types for the scheme shown in Figure 32, the worst-case data (fast silicon and maximum voltage values) shall be used:

- VCC_3V3_AFE at 3.6 V – 41 mA
- VDD12_AFE at 1.3 V – 14 mA

Based on the above, the overall worst-case power consumption of the entire AFE block equals approximately 150 mW (compared to 110 mW typical at nominal '3.3 V' and '1.2 V' rails' values).

5 Root Clocks

Clock connectivity is described in the “High Level Clocking Diagram” section in the “Clocking Overview” chapter of the processor reference manual. This section contains a series of tables that describe the clock inputs of each module and which clock is connected to it.

NOTE

In some cases, a clock is associated with an external interface and is sourced from a pad (mainly through the IOMUX block) and not from the CCM. Such clocks do not appear in the clock connectivity table but are described in the relevant interface sections.

Clock gating is done with the LPCG module based on a combination of the clock enable signals. For information on how the clock-gating signals are logically combined, see the “LPCG” section in the “CCM” chapter of the chip reference manual.

In some cases, a user needs to divide the clock inside the module when the maximum frequency is used in order to meet the protocol requirements. CCM generates and drives the clock sources.

For information on how the root clocks are generated, see the “Clocking Overview” and “Clock Controller Module (CCM)” chapters of the chip reference manual.

The root clocks, with the relevant CCM signal names and default (that is at boot time) speeds, are detailed in the “Clocks at Boot Time” chapter of the chip reference manual.

6 Processor Expert Tool

Processor Expert is a software tool for design, implementation, verification, and optimization of the embedded microcontroller applications available on the Freescale web site. This high-productivity development platform allows efficient use of microcontrollers and their peripherals and saves development time and cost. It has built-in internal definitions of the entire microcontrollers spectrum with all their integrated peripherals. An intuitive and powerful graphical user interface allows users to define the desired behavior of the system by using components with their settings and selections. Based on the users’ feedback, its functions and Freescale processors’ coverage are being constantly developed and new features added.

Out of the Processor Expert components available at the time of publication, there are two hardware-design aids of interest, IOMUX and DDRv.

6.1 IOMUX design aid

The IOMUX design aid facilitates the assignment of internal signals to external device pins by helping users to:

- Record signal assignments for the supported processor
- Identify conflicts, allowing them to be resolved in real time
- Add notes or comments for each signal to the list of recorded assignments
- Generate C code to configure the IOMUXC registers according to the specific design
- Move signals to different modules to order configuration code into logical functions

6.2 DDRv design aid

The DDR Validation (DDRv) design aid is a software application that helps to optimize the DDR settings, which otherwise might appear to be quite marginal. It helps user to find all the settings that work for a specific application, display them on a visual map allowing to select a setting that provides the maximum margin.

This process can be extremely difficult and generally requires specialized software running large exhaustive tests on very large memories. While running such tests, user needs to vary each setting against other varying ones – basically setting up a geometric progression that is very time-consuming, complex, and fraught with problems. Furthermore, user must track what worked, what didn't work, and then have some way to make sense from all that data. The DDRv application does all of this automatically.

7 Debug Interfaces

7.1 Using OpenSDA debug interface

OpenSDA is a low-cost open-standard serial and debug interface embedded in certain Freescale platforms, for example the Vybrid Tower module (see Table 33). It bridges serial and debug communications between a USB host, for example a computer, and a target processor.

OpenSDA features a mass-storage device bootloader, which provides a quick and easy mechanism for loading different OpenSDA applications such as flash programmers, run-control debug interfaces, serial-to-USB converters, and more.

Refer to the OpenSDA documentation for details.

7.2 Using JTAG debug interface

The JTAG module is a standard JEDEC debug peripheral. It provides debug access to important hardware blocks, such as the ARM processor and the system bus, which can give users access and control over the entire chip.

7.2.1 Vybrid JTAG tool requirements

To use JTAG tools, the user's system must have a standard ARM JTAG port, for example a 20-pin header. Freescale recommends making it accessible during initial validation, bring-up, and software debugging. It is accessible in all development kits from Freescale.

Multiple tools are available for accessing the JTAG port for tests and software debugging. Freescale recommends use of the ARM JTAG tools for compatibility with the ARM core. However, the JTAG chain should also work with non-ARM JTAG tools as described in the following sections. For more information about configuring non-ARM tools, contact the third-party tool vendor for support.

7.2.2 Extra JTAG functionality

Additional debug components, such as trace machines may be used for extra JTAG functionality, for example the ARM DSTREAM hardware connected to the target processor via the ARM ETM interface implemented on the 38-pin Mictor connector and running the ARM DS-5 debug software.

Such an option, however, is not mandatory for a basic configuration and beyond the scope of this document, although some Freescale kits, for example the Vybrid Tower module, feature the ETM™ connector, with the regular JTAG connection being a subset thereof.

7.2.3 JTAG security

To prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the Vybrid series processors incorporate a secure controller for regulating JTAG access. It provides four different JTAG security levels, which are selected by the e-Fuse configuration.

For more information about the security levels, see the "Secure JTAG control" section in the Vybrid chip reference manual.

8 Avoiding Board Bring-up Problems

This chapter provides recommendations for avoiding typical mistakes when bringing up a board for the first time. These recommendations consist of basic techniques that have proven useful in the past for detecting board issues and addressing the three most typical bring-up pitfalls: power, clocks, and reset. A sample bring-up checklist is provided at the end of the chapter.

8.1 Monitoring current to avoid power pitfalls

Excessive current can cause damage to the board. The problem is avoided by using a current-limiting laboratory supply set to the expected typical main current draw (at most) and monitoring the main supply current when powering-up the board for the first time. In this case, any excessive current can usually be detected before permanent damage occurs.

8.2 Verifying power sequencing

It is recommended to verify that the power sequencing (especially the power-up) requirements mentioned earlier in Table 24 are met.

8.3 Using Voltage Report to avoid power pitfalls

Using incorrect voltage rails is a common power pitfall. To help avoiding this mistake, it is recommended to create a basic table called Voltage Report prior to bringing-up the board. It helps to validate that all the supplies are reaching the expected levels.

The Voltage Report lists the following:

- The board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

The best measurement location on the board for each power rail should be carefully determined, taking into account the parasitic voltage drop (called IR drop). The following guidelines help to produce the best current measurements:

- Measuring closest to the load (the processor in this case)
- Making two measurements – the first after initial board power-up and the second while running a heavy use-case that stresses the processor

Ensure that the supplies powering the Vybrid device meet the data sheet DC electrical specifications.

Table 25 is an example based on the Vybrid Tower module data; it shows that the measured values are well within the required range and close to those expected.

Table 25. Voltage Report on Vybrid Tower module example

Source	Board net name	Required Vybrid voltage range (volts)	Expected value (volts)	Measured value (volts)	Point of measurement (across)
Built-in Vybrid LDO	VCC_1V1	0.9 to 1.2	1.10	1.11	C59
Built-in Vybrid LDO with external ballast transistor	VCC_1V2	1.1 to 1.26	1.23	1.232	C43
On-board regulator	VCC_1V5_SDRAM		1.50	1.509	C10
Built-in Vybrid LDO	VCC_2V5_SDRAM	2.3 to 2.6	2.50	2.497	C141
On-board regulator	VCC_3V3_MCU	3.0 to 3.6	3.30	3.303	C47
On-board regulator	VCC_3V3_ADC	3.0 to 3.6	3.30	3.303	C171
On-board regulator	VCC_3V3_AFE	3.0 to 3.6	3.30	3.303	C56

8.4 Checking for processor clock pitfalls

Problems with the clocks are another common source of board bring-up issues; it has to be ensured that all the clock sources are running as expected.

8.4.1 Checking reference clocks

8.4.1.1 Checking built-in reference clocks

The built-in 24 MHz and 32 kHz crystal-based oscillators (using the XTAL / EXTAL and XTAL32 / EXTAL32 pin pairs, respectively) are two main reference clock sources.

It must be verified that:

- They have no external feedback resistors (have high-resistance built-in ones)
- The XTAL ball is biased with a 2.2 MΩ resistor to GND placed as close as possible to it (see Table 7)

When checking crystal frequencies, the following guidelines need to be followed:

- Using an active probe is recommended to avoid excessive loading
- Probing the output less likely inhibits the oscillator from starting-up than probing its input

The best practice is to monitor the 32 kHz oscillator signal when it is internally routed to Vybrid output. This provides required buffering and avoids probing the crystal directly, which may stop the oscillation.

If a 32.768 kHz crystal is not connected to the processor, the loose-tolerance on-chip ring oscillator (SIRC) is automatically used for the low-frequency clock source (see Table 7).

8.4.1.2 Checking external reference clocks

If an application requires a high-quality 24 MHz clock, it uses an external oscillator. If a solution described in Section 2.4, “Connection of 3.3 V powered external 24 MHz clock source” is applied, the parasitic capacitances act as “hidden components,” whose values are only estimated at the early design stages. It has to be verified that the XTAL voltage swing meets the Vybrid data sheet requirements, otherwise the voltage divider tuning is required.

8.4.2 Checking auxiliary external clocks

Although not mandatory, usage of low-jitter external oscillators to feed LVDS0P/N on the processor can be an advantage if low-jitter or special-frequency clock sources are required by modules driven by LVDS0P/N. See the reference manual for details.

8.4.3 Checking clock frequencies indirectly

While being probed directly, a built-in oscillator inevitably somewhat changes its oscillation frequency. As an alternative, it is possible to measure the specific clock frequency on the CKO1 or CKO2 outputs.

Due to the maximum frequency limitation of a GPIO pad, the initial clock frequency has to be divided to have a value of a few tens of megahertz. Higher frequencies may be output via the LVDS0P/N differential port (see Table 7 for details).

See the processor reference manual for details about which clock sources can be output to these outputs and how their frequencies can be divided. A JTAG tool (see 7, “Debug Interfaces”) can be used to configure the necessary registers to do this.

8.5 Avoiding power-on reset pitfalls

Although the processor generates an internal power-on reset signal (see Table 8 and Figure 33), using an external $\overline{\text{RESET}}$ signal is strongly recommended.

As per Table 8, a power-on reset IC should have:

- An open-drain / collector output type
- An active-low output signal
- An active timeout period long enough to guarantee that when the output signal goes high:
  - all the voltage rails associated with boot-up stabilize at their nominal levels
  - the selected boot-source is ready to communicate with the processor (see Section 8.6.1, “Verifying boot-source readiness”)

Figure 33 shows the Vybrid power-up sequence, including the $\overline{\text{RESET}}$ and the 24 MHz crystal-based oscillator behavior.

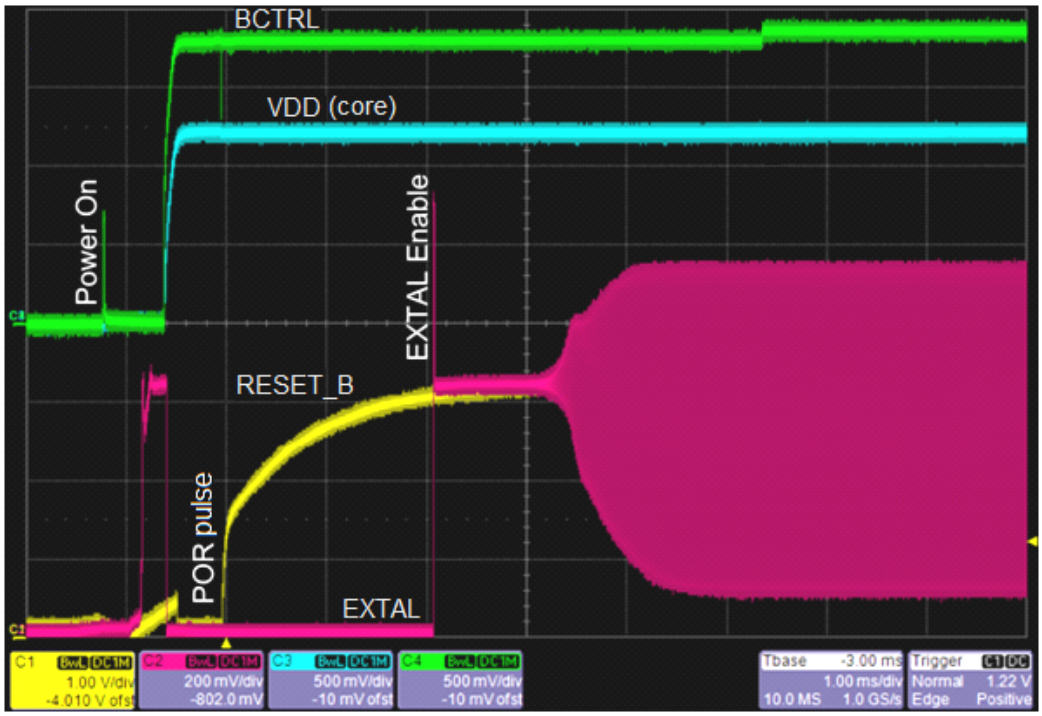


Figure 33. Vybrid power-up sequence example

8.6 Booting using correct boot mode

The following aspects must be verified:

- The boot-mode pins (BOOTMOD[0..1] and, if applicable, RCON) are configured properly
- The processor is booting from the expected boot source, that is as the boot-mode pins dictate

If, despite the correct boot-mode pins' settings, the processor is not booting as expected, it might be due to the following reasons:

- Incorrect internal fuses' configuration – if the boot configuration reads from the internal fuses
- Incorrect sampling of boot-mode pins due to improper boot-mode circuit isolation – if external boot configuration is used (refer to Section 2.5, "Boot-mode circuit isolation")

For a more detailed description about the different boot modes and how the GPIOs and internal fuses control the processor boot behavior, refer to the "System Boot" chapter of the processor reference manual.

8.6.1 Verifying boot-source readiness

As mentioned earlier (see Table 8), it has to be guaranteed that, by the time the processor is supposed to boot from the selected memory type, its power-up initialization process is already completed. The amount of time required varies for different memory types, for example, it may be as long as hundreds of milliseconds for some SD cards.

To prevent such problems, the Freescale designs use power-on reset ICs with an active timeout period of at least 200 milliseconds (see Section 8.5, "Avoiding power-on reset pitfalls").

8.7 Sample board bring-up checklist

Table 26 incorporates the recommendations described in the previous sections. Blank cells should be filled in during bring-up as appropriate.

Table 26. Board bring-up checklist

Checklist Item	Details	Owner	Finding and status
Note: The following items must be completed serially.			
Perform a visual inspection.	Check major components to make sure nothing has been misplaced or rotated before applying power.		
Verify all Vybrid voltage rails.	Confirm that the voltages match the data sheet requirements. Be sure to check voltages not only at the voltage source, but also as close to the Vybrid as possible (like on a bypass capacitor). This reveals any IR drops on the board that will cause issues later. Ideally all of the Vybrid voltage rails should be checked, but VDD is particularly important. This is the core logic voltage and must fall within the parameters provided in the Vybrid data sheet. SDRAMC_VDD1P5 is also critical to the Vybrid boot-up. It is used as the DDR I/O pads' power source.		
Verify power-up sequence.	Verify that power-on-reset (POR_B) is de-asserted (high) after all power rails have come up and are stable. See the Vybrid data sheet for details about power-up sequencing.		
Measure / probe input clocks (32 kHz, 24 MHz, others).	Without a properly running clock, the Vybrid will not function properly.		
Check JTAG connectivity.	This is one of the most fundamental and basic access points to the Vybrid to allow the debug and execution of low-level code.		
Note: The following items may be worked on in parallel with other bring-up tasks.			
Access on-chip RAM.	Perform a basic "write-read-verify" test. No software initialization is necessary.		
Verify CKO outputs (measure and verify default clock frequencies for desired clock output options) if the board design supports probing of the CKO pins. Test points must be provided in order to monitor signals assigned to these pins.	This ensures that the corresponding clock as well as the involved PLLs are working. This step requires chip initialization, for example via the JTAG debugger, to properly set up the IOMUX to output CKO and to set up the clock control module to output the desired clock. Refer to the reference manual for details. Unlike the LVDS0P/LVDS0N balls, regular I/Os cannot handle high frequencies of some of the internal clocks. These clocks must be monitored by a divided version of the clock.		

Table 26. Board bring-up checklist (continued)

Checklist Item	Details	Owner	Finding and status
Using boot-mode settings, select different boot sources (that is memory types), then check signals on their buses, for example chip-select ones, clocks (including their frequencies), and so on.	This verifies the specified signals' connectivity between the Vybrid and boot device and that the boot-mode signals are properly set. See the "System Boot" chapter in the processor reference manual for details about configuring the various boot modes.		
Run basic DDR initialization, and then test its operation.	Assuming a JTAG debugger is used, run the DDR initialization and open a debugger memory window pointing to the DDR memory-map starting address. Check if a basic "write-read-verify" test passes, otherwise recheck: • the DDR initialization sequence • connections between the processor and the DDR device on the board It is also recommended that users re-check the schematic to ensure that the DDR memory has been connected to the processor correctly.		

9 Understanding the IBIS Model

This chapter explains how to use the IBIS model, which is an Electronic Industries Alliance standard for the electronic behavioral specifications of integrated circuit input / output analog characteristics. The model is generated in the ASCII text format and consists of multiple tables that capture “current vs. voltage” (IV) and “voltage vs. time” (VT) characteristics of each buffer. IBIS models are generally used to perform PCB-board-level signal integrity (SI) simulations and timing analyses.

The IBIS model:

- Supports fast chip-package-board simulation, with SPICE-level accuracy and faster than any transistor-level model
- Provides the following for portable model data:
  - I/O buffers, series elements, terminators
  - package RLC (resistance/inductance/capacitance) parasitics
  - electrical board description

9.1 IBIS structure and content

The IBIS file contains the data required to model a component’s input, output, and I/O buffers behaviorally in ASCII format.

The basic IBIS file contains the following data:

- Header information regarding the model file

- Information about the component, the package's electrical characteristics, and the pin-to-buffer model mapping (in other words, which pins are connected to which buffer models)
- The data required to model each unique input, output, and I/O buffer design on the component

IBIS models are component-centric, meaning they allow users to model an entire component rather than only a particular buffer. Therefore, in addition to the electrical characteristics of a component's buffers, an IBIS file includes the component's pin-to-buffer mapping and the electrical parameters of the component's package.

9.2 Header information

The first section of an IBIS file provides the basic information about the file and its data. Table 27 explains the header information notation, and the following example shows what header information look like in an IBIS file.

Table 27. Header information

Keyword	Required	Description
[IBIS Ver]	Yes	Version of IBIS Specification this file uses.
[Comment char]	No	Change the comment character. Defaults to the pipe (|) character.
[File Name]	Yes	Name of this file. All file names must be lower-case. The file name extension for an IBIS file is ".ibs".
[File Rev]	Yes	The revision level of this file. The specification contains guidelines for assigning revision levels.
[Date]	No	Date this file was created.
[Source]	No	The source of the data in this file. Data is taken from a simulation and validated on the board.
[Notes]	No	Component or file-specific notes.
[Disclaimer]	No	May be legally required.
[Copyright]	No	The file's copyright notice.

Example 1. Header information

```
[IBIS Ver]       4.2
[Comment Char]   |_char
[File Name]      vybrid_364_f.ibs
[File Rev]       1
[Date]           Fri Dec 14 11:49:57 2012
[Source]         FSL Viper 2012.06.28
[Notes]
```

9.3 Component and pin information

The second section of an IBIS file is where the data book information regarding the component's pinout, pin-to-buffer mapping, and the package and pin electrical parameters are placed. Table 28 explains the component and pin information notation, and the following example shows what it looks like in an IBIS file.

Table 28. Component and pin information

Keyword	Required	Comment
[Component]	Yes	The name of the component being modeled. Standard practice has been to use the industry-standard part designation. Note that IBIS files may contain multiple [Component] descriptions.
[Manufacturer]	Yes	The name of the component manufacturer.
[Package]	Yes	This keyword contains the range (minimum, typical, and maximum values) over which the packages' lead resistance, inductance, and capacitance vary (the R_pkg, L_pkg, and C_pkg parameters).
[Pin]	Yes	This keyword contains the pin-to-buffer mapping information. In addition, the model creator can use this keyword to list the package information: R, L, and C data for each individual pin (R_pin, L_pin, and C_pin parameters).
[Package Model]	No	If the component model includes an external package model (or uses the [Define Package Model] keyword within the IBIS file itself), this keyword indicates the name of that package model.
[Pin Mapping]	No	This keyword is used if the model creator wishes to include information on buffer power and ground connections. This information may be used for simulations involving multiple outputs switching.
[Diff Pin]	No	This keyword is used to associate buffers that should be driven in a complementary fashion as a differential pair.
[Model Selector]		This keyword provides a simple means by which several buffers can be made optionally available for simulation at the same physical pin of the component.

Example 2. Component and pin information

```
[Component]        BGA364
[Manufacturer]     FREESCALE
[Package]
| variable      typ                 min                 max
R_pkg           0.3036154           0.0040188           0.508762
L_pkg           3.45535nH           0.05120nH           6.31992nH
C_pkg           12.0998pF           0.70019pF           132.372pF
|
[Pin] signal_name model_name    R_pin      L_pin C_pin
A2    DDR_CLK[0]  ddr3          0.363171 4.85829nH 1.48037pf
A3    DDR_ZQ      POWER      0.322073 4.93118nH 1.28946pf
...

|
[Pin Mapping]   pulldown_ref    pullup_ref
A1               VSS             NC
A2               VSS             SDRAMC_VDD1P5
A3               VSS             SDRAMC_VDD1P5
...

|
[Diff Pin]  inv_pin  vdiff  tdelay_typ tdelay_min tdelay_max
A2          B2       NA        NA        NA        NA
D3          E3       NA        NA        NA        NA
E1          F1       NA        NA        NA        NA
Y14         W14      NA        NA        NA        NA
...
|
[Model Selector] ddr3
ddr3_sel11_ds111_mio                    DDR, 1.5V, ddr3 mode, 34 Ohm driver impedance
|
[Model Selector] gpiohv
gpiohv_ds111_sr111_mio                  GPIO, 3.3V,extra drive,fast sr,max fsel
```

9.4 Model information

The [Model] keyword starts the description of the data for a particular buffer. Table 29 shows the main sets of parameters and keywords, composing the model definition.

Table 29. Model information

Keyword	Comment
[Model Spec]	General set of parameters for the model simulation.
[Receiver Thresholds]	Threshold information for the different simulation cases.
[Temperature Range]	The temperature range over which the min, typ and max IV and switching data have been gathered.
[Voltage Range]	The range over which VCC is varied to obtain the min, typ and max pullup and power clamp data.
[Pulldown] [Pullup] [GND_clamp] [POWER_clamp]	IV information. For more details, see Section 9.4.1, “IV information.”
[Ramp] [Rising Waveform] [Falling Waveform]	VT information. For more details, see Section 9.4.2, “VT information.”
[Test Data] [Rising Waveform Near] [Rising Waveform Far] [Falling Waveform Near] [Falling Waveform Far] [Test Load]	VT golden model information. For more details, see Section 9.4.3, “Golden Model VT information.”

9.4.1 IV information

IV information is composed of four Current-over-Voltage tables: [Pullup], [Pulldown], [GND_clamp], and [Power_clamp]. Each look-up table describes a different part of the I/O cell model as shown in Figure 34.

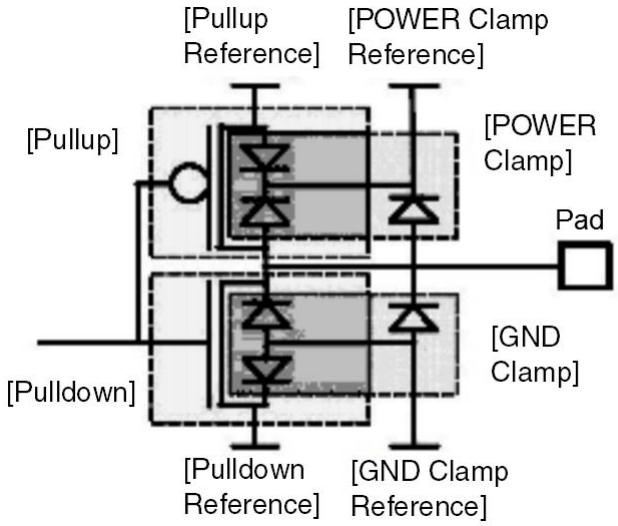


Figure 34. Structure of IV parameters

9.4.2 VT information

Table 30 defines the keywords that provide the information about an output or I/O buffer, and the following example shows what they look like in an IBIS file.

Table 30. Ramp and waveform keywords

Keyword	Required	Comment
[Ramp]	Yes	Basic ramp rate information, given as a dV / dt_r for rising edges and dV / dt_f for falling edges, see the following equation: $\frac{dV}{dt} = \frac{20\ \%\ \text{to}\ 80\%\ \text{voltage swing}}{\text{time taken to swing above voltage}}$ The dV value is the 20% to 80% voltage swing of the buffer when driving into the specified load, R_load (for [Ramp], this load defaults to 50). For CMOS drivers or I/O buffers, this load is assumed to be connected to the voltages defined by the [Voltage Range] keyword for falling edges and to ground for rising edges.
[Rising Waveform]	No	The actual rising (low to high transition) waveform, provided as a VT table.
[Falling Waveform]	No	The actual falling (high to low transition) waveform, provided as a VT table.

Example 3. Ramp and waveform keywords example

```
[Ramp]
| variable       typ                 min                 max
dV/dt_r  0.4596/0.3646n      0.4347/0.4508n      0.4825/0.3394n
dV/dt_f  0.4571/0.3648n      0.4353/0.3965n      0.4688/0.3872n
R_load = 0.2400k
|
[Rising Waveform]
R_fixture= 0.2400k
V_fixture= 0.0
V_fixture_min= 0.0
V_fixture_max= 0.0
|time     V(typ)              V(min)              V(max)
|
|0.0S              0.3514uV          5.6662uV            0.1188uV
|24.9696fS         0.5201uV          5.8401uV            0.2827uV
|26.1827fS         0.5283uV          5.8456uV            0.2907uV
|27.3500fS         0.5333uV          5.8509uV            0.2983uV
...
[Falling Waveform]
R_fixture= 0.2400k
V_fixture= 0.0
V_fixture_min= 0.0
V_fixture_max= 0.0
|time     V(typ)              V(min)              V(max)
|
|0.0S              0.7661V           0.7245V             0.8042V
|0.1197nS          0.7661V           0.7245V             0.8042V
|0.1648nS          0.7661V           0.7245V             0.8041V
|0.3327nS          0.7660V           0.7245V             0.8041V
...
```

The [Ramp] keyword is always required, even if the [Rising Waveform] and [Falling Waveform] keywords are used. However, the VT tables under [Rising Waveform] and [Falling Waveform] are generally preferred to [Ramp] for the following reasons:

- VT data may be provided under a variety of loads and termination voltages
- VT tables may be used to describe transition data for devices as they turn on and turn off
- [Ramp] effectively averages the transitions of the device, without providing any details on the shapes of the transitions themselves; all details of the transition ledges would be lost

The VT data should be included under two [Rising Waveform] and two [Falling Waveform] sections, each containing data tables for a VCC-connected load and a Ground-connected load (although other loading combinations are permitted).

The most appropriate load is a resistive value corresponding to the impedance of the system transmission lines the buffer will drive (own impedance). For example, a buffer intended for use in a 60 Ω system is best modeled using a 60 Ω load (R_fixture).

Figure 35 shows how to interpret the model data:

- I_down [GND clamp] + [Power clamp] + [Pulldown]
- I_up [GND clamp] + [Power clamp] + [Pullup]
- I_recvr [GND clamp] + [Power clamp]

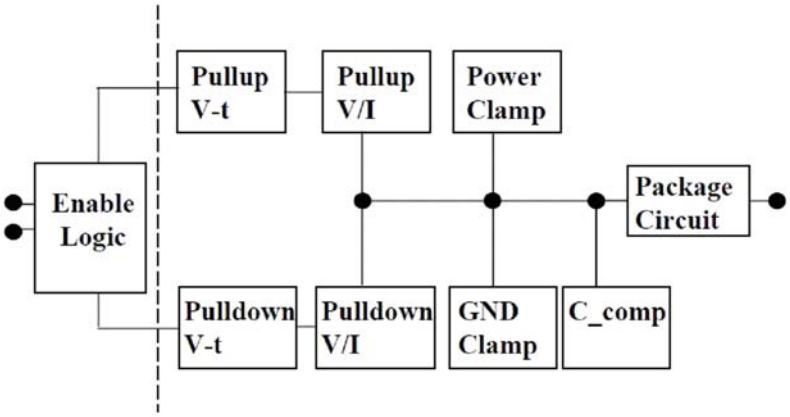


Figure 35. Model data interpretation

9.4.3 Golden Model VT information

Golden waveforms are a set of waveforms simulated using known ideal test loads. They are useful for verifying the accuracy of behavioral simulation results against the transistor-level circuit model from which the IBIS model parameters originated.

Figure 36 shows a generic test load network.

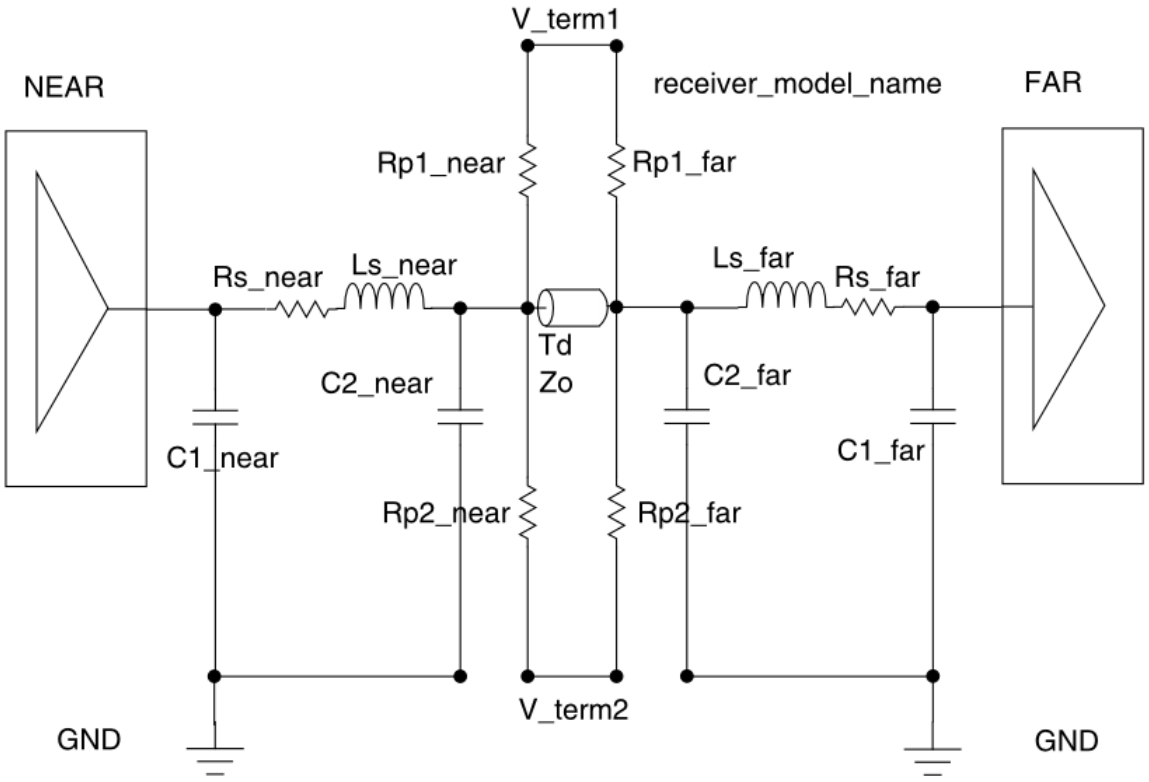


Figure 36. Generic test load network

Table 31. Golden waveform keywords

Keyword	Required	Comment
[Test Data]	No	Provides a set of golden waveforms and references the conditions under which they were derived. Useful for verifying the accuracy of behavioral simulation results against the transistor-level circuit model from which the IBIS model parameters originated.
[Rising Waveform Near] [Rising Waveform Far] [Falling Waveform Near] [Falling Waveform Far]	Yes	Current-Over-Voltage tables, for far and near portions of the golden model as described in Figure 36.
[Test Load]	Yes	• Defines a test load network and its associated electrical parameters for reference by golden waveforms under the [Test Data] keyword. • If Test_load_type is Differential, the test load is a pair of the circuits shown in Figure 36. If the R_diff_near or R_diff_far subparameter is used, a resistor is connected between the near or far nodes of the two circuits. • If Test_load_type is Single_ended, R_diff_near and R_diff_far are ignored.

9.5 Naming conventions for model names and usage in Vybrid IBIS file

The model names are defined per each [Model selector]. The models may differ from each other by having different parameters – such as voltage, drive strength, mode of operation, and slew rate. The mode of operation, drive strength, and slew rate parameters are programmable by software.

9.5.1 [Model Selector] ddr

The “ddr” model type supports the DDR protocol signals.

9.5.1.1 DDR [Model Selector]

The “ddr” models exist for all the DDR protocols.

This model type has the following parameters:

- DDR protocol
- DDR I/O type
- drive strength
- ODT enable / disable

The IBIS model name is composed from the parameters’ values in two ways, as follows:

- Without active ODT circuit:

  ```
  <ddr protocol>_sel<ddr_type>_ds<drive_strength>_mio
  ```

- With active ODT circuit:

  ```
  <ddr protocol>odt_t<ODT_value>_sel<ddr_type>_mi
  ```

DDR write models ("_mio" suffix) have no simulated ODT, as ODT is disabled during write.
Write models' DS parameter is meaningful and changes to describe the different levels of drive strength.

DDR read models ("_mi" suffix) have no meaningful DS parameter, as no driving happens during read.
Read models’ ODT parameter is meaningful and changes to describe different levels of ODT impedance.

DDR protocol is selected according to the DDR used. DDR I/O voltage level is selected accordingly.

DDR I/O Type is selected between DDR3 & LPDDR2 using the DDRMC_CR154 register.

Drive strength is Defined by the DSE settings in the IOMUX registers controlling the I/Os involved in the DDR operation.

ODT value is Defined by the ODT settings in the IOMUX registers controlling the ODT behavior of the I/Os involved in the DDR operation.

Example 4. [Model Selector] DDR in IBIS file

```
[Model Selector] ddr3
ddr3_sel11_ds111_mio                    DDR, 1.5V, ddr3 mode, 34 Ohm driver impedance
...
|
[Model Selector] ddr3odt
ddr3odt_t17_sel11_mi                    DDR, 1.5V, ddr3 mode, 17 Ohm ODT
...
|
[Model Selector] lpddr2
lpddr2_sel10_ds111_mio                  LPDDR, 1.2V, lpddr2 mode, 34 Ohm driver impedance
lpddr2_sel10_ds110_mio                  LPDDR, 1.2V, lpddr2 mode, 40 Ohm driver impedance
...
```

See the register description in the “IOMUXC” chapter in the chip reference manual for further details about this model.

9.5.2 [Model Selector] gpio

This model has the following parameters:

- voltage level
- drive strength
- slew rate
- speed

The IBIS model name is composed from parameters’ values as follows:

```
gpio<voltage_level>_ds<drive_strength>_sr<slew_rate(1 bit)><speed(2 bits)>_mio
```

- Voltage level for Vybrid chips is rated for 3.3 V
- Drive strength is defined by the DSE settings in the IOMUX registers controlling the relevant I/Os
- Slew rate is Defined by the SRE settings in the IOMUX registers controlling the relevant I/Os
- Speed is defined by the SPEED settings in the IOMUX registers controlling the relevant I/Os

9.5.3 [Model Selector] lvds

A single model is available for LVDS, as no configurable parameters exist for this I/O model.

Example 5. [Model Selector] lvds in IBIS file

```
[Model Selector] lvds
lvds_mio                              LVDS, Vos = 1.2V, Voh = 1.375, Vol = 1.025, Vovdd = 2.5
...
```

9.6 Quality assurance for IBIS models

The IBIS models are validated against the IBIS specification, which provides a way to objectively measure the correlation of model simulation results with reference transistor-level spice simulation or measurements.

Correlation is the process of making a quantitative comparison between two sets of I/O buffer characterization data, such as lab measurement vs. structural simulation or behavioral simulation vs. structural simulation.

Correlation level is a means for categorizing I/O buffer characterization data based on how much the modeling engineer knows about the processing conditions of a sample component and which correlation metric he or she used.

All models have passed the following checks:

- IBISCHK without errors or unexplained warnings
- Data for basic simulation checked
- Data for timing analysis checked
- Data for power analysis checked
- Correlated against Spice simulations

Validation reports can be provided upon demand.

9.7 IBIS usage

Freescale board designers used the Vybrid IBIS model with the HyperLynx tool by Mentor Graphics.

Effective board design results achieved after loading:

- Vybrid IBIS model
- Companion IC IBIS models
- Board model in HyperLynx format

Board simulations for various signals were then run.

9.8 References

Consult the following references for more information about the IBIS model:

- IBIS Open Forum (www.eda.org/ibis)
  - The IBIS Open Forum consists of EDA vendors, computer manufacturers, semiconductor vendors, universities, and end-users. It proposes updates and reviews, revises standards, and organizes summits. It promotes IBIS models and provides useful documentation and tools.
- IBIS specification (eda.org/pub/ibis/ver5.0)

10 Using Manufacturing Tool

10.1 Overview

The tool is designed to program firmware onto storage devices such as NAND or an SD card and to pre-load the data area with media files in an efficient and convenient manner. It is intended for Freescale Semiconductor customers or their OEMs who plan to mass-manufacture processor-based products.

The tool version available at the date of publication:

- Only supports parts with a primary A5 core
- Only uses the on-chip RAM

The application is not designed to test the devices or to diagnose manufacturing problems. Devices initialized with this application still need to be functionally verified.

10.2 Feature summary

The tool includes the following features:

- Continuous operation – operations automatically begin with the connection of a new device, and multiple operations such as update and copy can be linked together seamlessly
- Enumeration – static-ID firmware loaded into RAM in recovery-mode prevents the computer operating system from enumerating every device
- AutoPlay – various “pop-up” applications and status messages, such as Explorer in Windows® XP and Windows® 7

In addition, the following characteristics improve the tool’s ease of use:

- An independent process bar is set up for each physical USB port
- The tool begins processing with the connection of the first device detected and allows users to replace each device after completion instead of needing to wait for all devices to complete
- The tool uses color-based indicators to indicate the work status on each of the ports:
  - blue indicates the device is being processed
  - green indicates the device was successfully processed and that the programmed device can be replaced with a new one, independent of the device’s progress
  - red indicates the device failed to process

10.3 Other references

For more detailed information about the manufacturing tool, see the following documents included in the manufacturing tool release package. Contact the local Freescale sales office for assistance in obtaining documents if needed:

- For detailed information about how to use the manufacturing tool, see *"Manufacturing Tool V2 Quick Start Guide"*
- For detailed information about how to script the processing operations of the manufacturing tool, see the *"Manufacturing Tool V2 UCL User Manual"*
- For information about how to generate the manufacturing tool firmware for Linux and Android, see *"Manufacturing Tool V2 Linux or Android Firmware Development Guide"*
- For the change list and known issues, see *"Manufacturing Tool V2 Release Notes"*

11 Using BSDL for Board-level Testing

11.1 BSDL overview

Boundary Scan Description Language (BSDL) is used for board-level testing after components have been assembled. The interface for this test uses the JTAG interface pins. The definition is contained within IEEE Std 1149.1.

11.2 How BSDL works

The BSDL file defines the internal scan chain, which is the serial linkage of the I/O cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, a test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, to test an external ROM interface, the tool would do the following:

- Output a specific set of addresses and controls to pins connected to the ROM
- Perform a read command and scan out the values of the ROM data pins
- Compare the values read with the known golden values

Based on this procedure, the tool can determine whether the interface between the two parts is connected properly and contains no shorts or opens.

Boundary-scan specifics of configuring and using Vybrid's I/Os as outputs, for example for the above-mentioned external ROM interface test, are described in the *"e8379"* erratum.

11.3 Downloading BSDL file

The BSDL file for each Vybrid processor is stored on the Freescale website upon product release. Contact the local sales office or field applications engineer to check the information availability prior to product releases.

11.4 Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. User can open the file with a text editor (like Wordpad) to review how each pin will function. The BSDL file defines these functions as shown:

```
-- PORT DESCRIPTION TERMS
-- in      = input only
-- out     = three-state output (0, Z, 1)
-- buffer  = two-state output (0, 1)
-- inout   = bidirectional
-- linkage = OTHER (vdd, vss, analog)
```

The appearance of “linkage” in a pin’s file implies that the pin cannot be used with boundary scan. These are usually power or analog pins that cannot be defined with a digital logic state.

11.5 I/O pin power considerations

The boundary scan operation uses each of the available device pins to drive or read values within a given system. Therefore, the power supply pin for each specific module must be powered in order for the I/O buffers to operate.

This requirement is straightforward for the purely digital Vybrid pins. However, some I/O pins are shared by the digital and analog Vybrid modules. As per Section 2.10, “Unused analog interfaces,” used pins that have a shared analog and digital function must have the associated analog module powered; also during BSDL, when shared pins are part of the test. Analog power supplies have no effect on the BSDL scan chain itself but they do affect the I/O drivers.

12 Using MAC (Ethernet) Interface

12.1 Overview

Due to limited number of dedicated I/Os, the Vybrid MAC (Ethernet) block may provide either one MII or two RMII connections. Although some of the Vybrid reference designs provide an optional MII connection (see Table 33), all of them feature at least one RMII connection, therefore this chapter focuses on this option.

NOTE

This chapter only covers the required hardware and register settings. Modifications to the MAC (Ethernet) driver or its initialization code are beyond its scope. For this information, see the BSP documentation.

12.2 RMII signal connections

Figure 37 shows the signal connections required to use the RMII interface. Although they are generally self-explanatory or explained in the chip reference manual, some additional information is required.

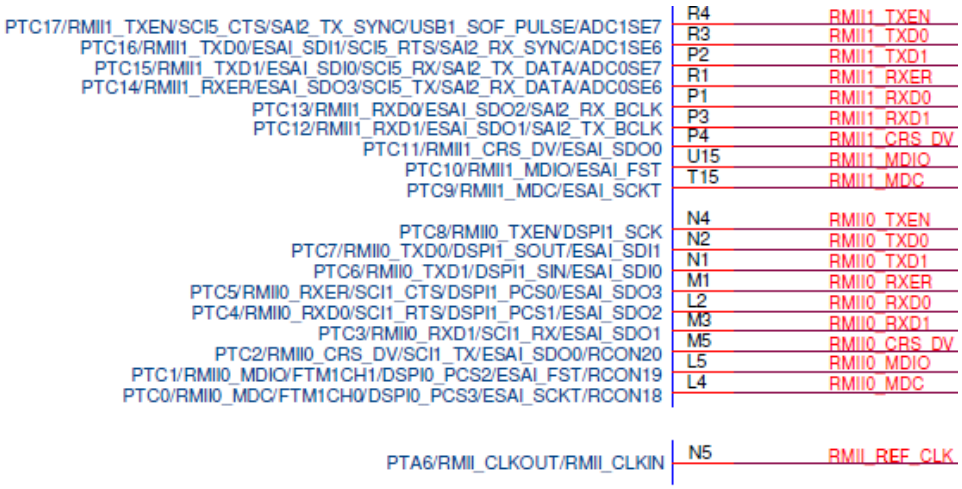


Figure 37. RMII interface signals

12.3 Generating RMII reference clock

Being one of the RMII interface signals, a free-running 50 MHz reference clock may be generated either externally or internally to Vybrid.

12.3.0.1 External RMII reference clock

Two options exist for generating the RMII reference clock externally to Vybrid:

- By an external oscillator providing it to both Vybrid and the PHY (see Figure 38)
- By an Ethernet PHY providing it to Vybrid (see Figure 39)

With the RMII reference clock pin configured as an input, both are supported.

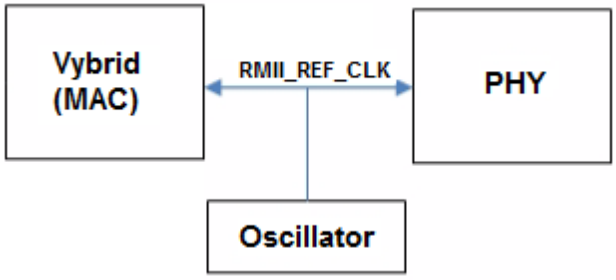


Figure 38. Reference clock from external oscillator to Vybrid and PHY

Figure 39. Reference clock from PHY to Vybrid

12.3.0.2 Internal RMII reference clock

The clock can be generated by Vybrid and delivered via its RMII reference clock pin configured as an output (see Figure 40).

Figure 40. Reference clock from Vybrid to PHY

As mentioned in Table 9, the erratum *e8052* – "*RMII TX hold time too small when processor provides RMII reference clock*" is applicable in this case.

Two alternative workarounds are available while using this scheme:

- For each TX data line, add an external capacitor to ground (see Figure 41) and decrease pad drive-strength (that is increasing internal impedance). Reduction of the pulse edge slope is equivalent to delaying the TX data with respect to the reference clock. To meet the RMII specification hold-time requirements reliably, tune the pad drive-strength and / or the external capacitance.

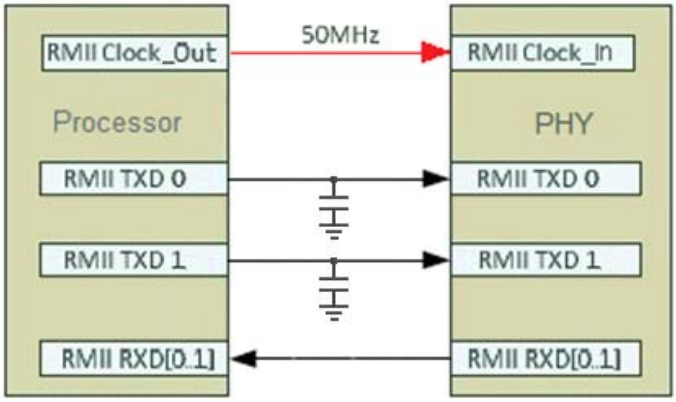


Figure 41. Workaround based on TX data delay

- Configure Vybrid to deliver a free-running 50 MHz clock via a pin not involved in the RMII functionality. Bring this clock externally back to the processor pin used as an RMII reference clock input (see Figure 42). Because this clock is not related to the RMII functionality, the processor's MAC (Ethernet) block treats it the same way as if it came from an external source, that is, like in Section 12.3.0.1, “External RMII reference clock.”

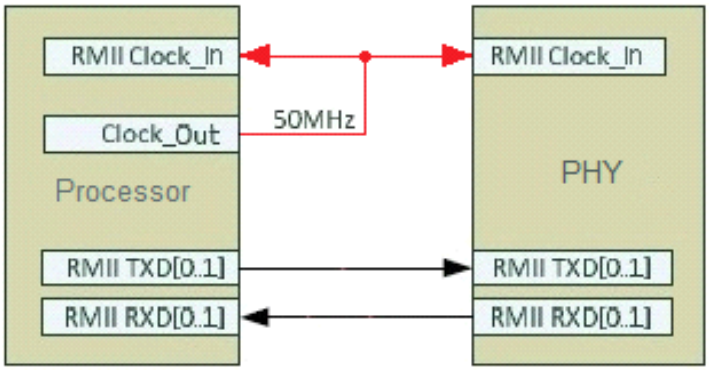


Figure 42. Workaround based on "external clock source" scheme

Since the workaround impacts the design hardware, it shall be applied as early as on the schematic drawing stage.

13 Revision history

Table 32. Revision history

Rev. No.	Date	Change description
0	11/2014	Initial release
1	05/2015	Added Crystal Power Calculator and DDR_ODT1 pin description

Appendix A Development Platforms

This appendix provides a list of the Freescale Vybrid-based development platforms that are available at the date of publication. This information may be used as a quick guide for finding the best match for the specific user's needs.

Table 33. Vybrid Tower module

Vybrid version used	MVF61NS151CMK50
Marketing Part Number	TWR-VF65GS10
Schematic Part Number and Rev.	170-27442, Rev.H
Features	• USB-powered • battery-based power supply for Vybrid Real-Time Clock and Tamper Detection modules • OpenSDA (USB) port • 1-Gb (64Mx16) DDR3 IC • 2-Gb (128MX16) NAND Flash IC • two 128-Mb (16 MB) QuadSPI Flash ICs • micro SD Card slot • jumpers for boot-device selection (QuadSPI, NAND, SD card, or USB Flash drive) • three mechanical push buttons for user inputs, and one for reset • potentiometer connected to Vybrid ADC • three-axis digital accelerometer • general-purpose TWRPI socket • 20-pin JTAG debug header • ARM® 38-pin Mictor ETM / Trace debug connector • dual USB interface with Vybrid on-chip PHYs (full 500 mA support per connector) • UART interface via Elevator • graphical interface via Elevator to TWR-LCD-RGB module • 10 / 100 Mbit/s MAC (Ethernet) interface (two RMII or one optional MII) via Elevator
Schematic	Available at http://www.freescale.com/TWR-VF65GS10
Layout	
Quick Start Guide	
User Guide	

Table 34. Vybrid Automotive Evaluation Board

Vybrid version used	SVF522R3K1CMK4
Marketing Part Number	EVB-VF522R3
Schematic Part Number and Rev.	170-28141, Rev.A
Features	• powered from single 12 ± 2 V DC supply • 1-Gb (64Mx16) DDR3 IC • three 256-Mb (32 MB) QuadSPI Flash ICs • SD Card slot • boot configuration jumpers and full 32-bit RCON switches • two incremental encoders • four dedicated station preset buttons • potentiometer connected to Vybrid ADC • unified 24-bit DCU connector (matches Freescale LCD and HDMI daughtercards) with analog and I^2C support for basic touchscreen operation • four analog video inputs with direct connection to Vybrid video ADC • 0.1 headers for all GPIO and analog signals not used elsewhere on the board • Aux In connector (3.5mm) with filter and dedicated audio ADC • left and right SPI-based microphones • standalone DSP for audio processing • SPI serial 32-Mbit Flash IC (dedicated to DSP, optional usage) • twin dedicated audio DAC, filter, and headphone amplifiers for audio outputs (3.5 mm connectors) • radio-tuner daughtercard connector • I^2C header for custom-made daughtercard powered from 3.3 V • I^2C header for daughtercard powered from 5 V • bluetooth daughtercard header • MLB daughtercard connector • board-to-board connector bearing one 10 / 100 Mbit/s RMII MAC (Ethernet) interface • generic CD header • 20-pin JTAG debug header • 10-pin Cortex™ debug header • two Vybrid USB interfaces based on On-The-Go Micro AB and Type A Host connectors with full 500 mA support each • high-speed CAN transceiver • SCI / RS232 and LIN transceivers on shared Vybrid SCI0 channel
Schematic	Schematic and Layout available on request.
Layout	
User Guide	Quick Start Guide and User Guide available at freescale.com/EVB-VF522R3
Quick Start Guide	

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