PQ–MDS–T1
084-00214-2
PMC T1/Slic-Slac add in module
User's Manual

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Section1 General Information

1.1 Introduction

The **PQ-MDS-T1** - T1/E1/DS3/T3/SLIC-SLAC (Subscriber Line Interface Controller/Subscriber Line Access Controller) module serves as a platform for S/W and H/W development around the 83xx host device.
Using **MPC83xxE-MDS-PB/ PQ-MDS-PIB** on-board resources and **PQ-MDS-T1** module T1/E1, DS3/T3 and /or Voice Over IP dual interfaces, a developer able to load his code, run it, set breakpoints, display memory and registers and debug his own proprietary software.
This module may be used as an evaluation and demonstration tool, i.e. application S/W may be programmed into **MPC83xxE-MDS-PB** on-board flash memory and run at university's sites, exhibitions etc.

1.2 PQ-MDS-T1 module features

- PMC mezzanine card form-factor
- Compatibility with **PQ-MDS-PIB**
- 8 E1/T1 channels
- 2 DS3/T3 channels
- Legerity Line Module Le71HR0826 (**LM**) interconnection compatible connector to provide all the necessary dual-channel voice interface functions from the high voltage subscriber line to the CPU digital interface
- Full board SW programmable control
- Network Interface Protection for Over-voltage and Over-current Events

1.3 PQ-MDS-T1 Host interface

PQ-MDS-T1 interconnects with **PQ-MDS-PIB** through PMC standard connectors set.

- 8 Host TDM channels operate with the card.
- **PQ-MDS-T1** SW control provided through Host Local Bus interface.
- Power supply provided from **PQ-MDS-PIB**

1.4 PQ-MDS-T1 main functions support:

1.4.1 Octal T1/E1/J1 Framer

Octal T1/E1/J1 is a single-chip 8-port framer and line interface unit (LIU) combination for T1, E1, and J1 applications. Each port is independently configurable, supporting both long-haul and short-haul lines. The main features are:

- Eight Complete T1, E1, or J1 Long-Haul/Short-Haul Transceivers (LIU plus Framer)
- Independent T1, E1, or J1 Selections for Each Transceiver
- Internal Software-Selectable Transmit- and Receive-Side Termination for 100Ω T1 Twisted Pair, 110Ω J1 Twisted Pair, 120Ω E1 Twisted Pair, and 75Ω E1 Coaxial Applications
- Crystal-Less Jitter Attenuators can be selected for Transmit or Receive Path. The Jitter Attenuator meets ETSI CTR 12/13, ITU G.736, G.742, G.823, and AT&T PUB 62411.
- External Master Clock can be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 operation. This Clock is Internally Adapted for T1 or E1 Usage in the Host Mode.
- Receive Signal Level Indication from -2.5dB to -36dB in T1 Mode and -2.5dB to -44dB in E1 Mode in Approximate 2.5dB Increments
- Transmit Open and Short Circuit Detection
- LIU LOS in Accordance with G.775, ETSI300233, and T1.231
- Transmit Synchronizer
- Flexible Signaling Extraction and Insertion Using Either the System Interface or Microprocessor Port
- Alarm Detection and Insertion
- T1 Framing Formats of D4, SLC-96, and ESF
- J1 Support
- E1 G.704 and CRC-4 Multiframe
- T1 to E1 Conversion

1.4.2 Dual DS3/T3 framer

Dual DS3/E3 chip include Framing, Line Interface Unit with Jitter Attenuator. A flexible parallel microprocessor interface is provided for configuration and control. The main features are:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- Operates in either in “Serial” or the “Nibble-Parallel” mode
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola or PowerPC
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE, 1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b, ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Maximum power consumption 1.7W
- DS3 framer supports both M13 and C-bit parity.

- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF, LOF, AIS, and RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832, G.751 standards.
- Framers can be bypassed.

1.5 PQ-MDS-T1 module control functions:

All module control functions implemented through Local Bus mapped set registers incorporated into the on-board PLD device. The corresponding software has the opportunity to control:

1. T1/E1 framer setting
2. DS3/T3 framer setting
3. SLIC/SLAC modem (LM card) setting
4. Additional functions like:

- Board identification number
- Board revision number
- PLD revision number
- T1/E1 Framer MCLK and REFCLKIO Source
- T1/E1 Framer Configuration Pin Settings
- T1/E1 Framer Tx and Rx SYSCLK Source
- T1/E1 Framer TSSYNC Source
- T1/E1 Framer TCLK, TSYNC, RSYNC, TSER, RSER sources

5. SLIC/SLAC modem (LM card) TDM channel selection
6. T1/E1 and/or DS3/E3 modem disabling

1.6 PQ-MDS-T1 module visual indicators:

- Operating mode T1/E1, DS3/T3 LED's are populated on the board
- RLOS LED's provide Receive/Syncro/ Clock Loss visual indication of the each framer's corresponding channel
- LED "Connection" used to confirm correct and reliable interconnection between **PQ-MDS-T1** and the **PQ-MDS-PIB** boards

1.7 PQ-MDS-T1 module main circuit elements:

The following main circuit elements are used in the module design:

- T1/E1 Framer **DS26528** from Dallas Semi.
- DS3/T3 Framer **XRT79L72** from Exar Co.
- PLD **EPM3512AFC256-7N** from Altera

Section2 PQ-MDS-T1 module Block Diagram

PQ-MDS-T1 Block Diagram represented in the **Figure 1**

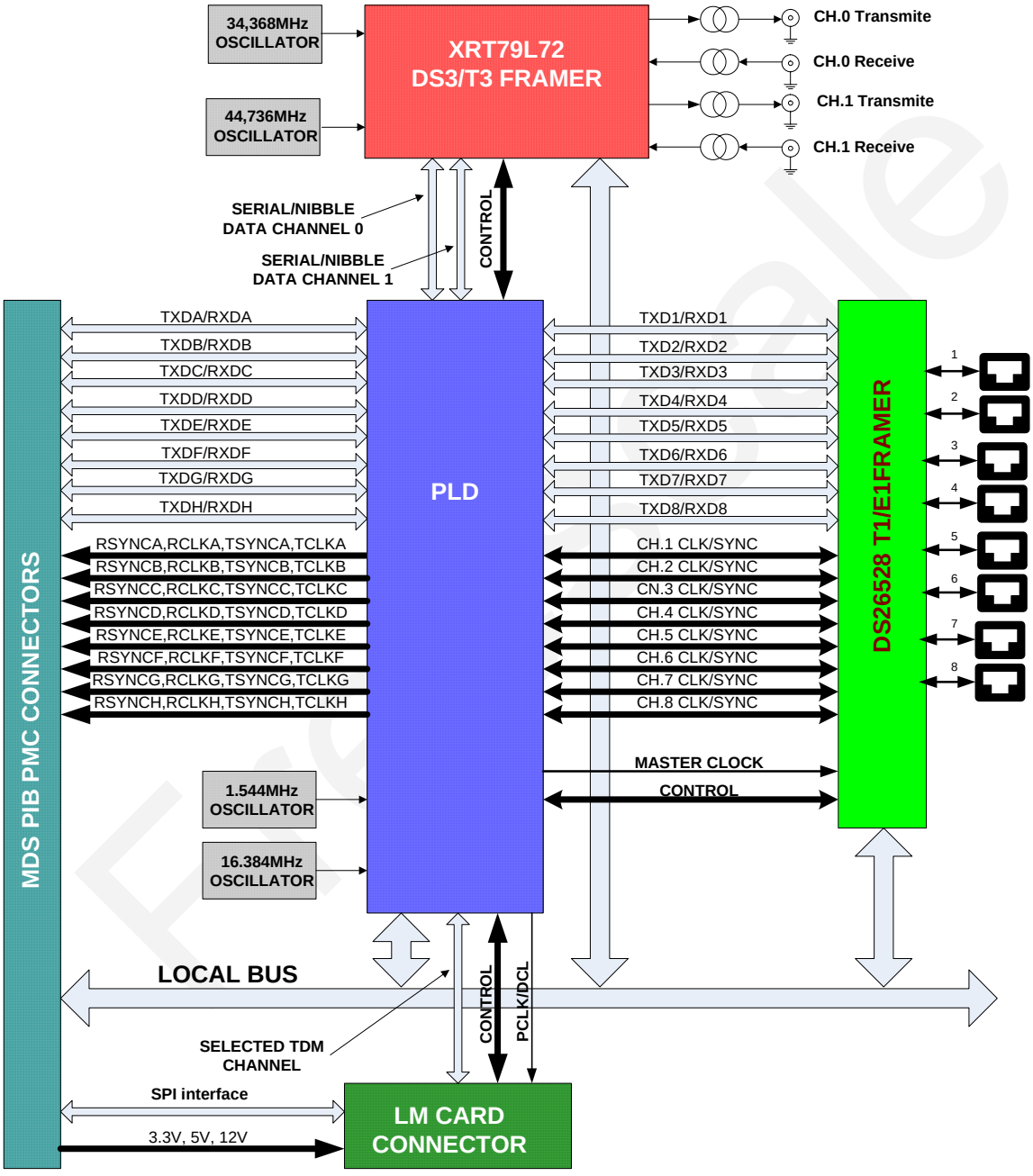

Figure 1

Section3 PQ-MDS-T1 Address map

3.1 General address space

Accordingly to **Figure 1** the following components: T1/E1Framer, DS3/T3 Framer, and PLD are mapped on the Host Local Bus to provide theirs SW control. Control of the LM card provided through Host independent SPI interface. The corresponding memory map represented in the **Table 1**

Table 1

#	Address range	Device	Data bus (bit)	Description	Note
1	0000-1FFF	T1/E1 Framer	8	DS26528 T1/E1/J1 transceiver	**A19-A31** (A12-A0)
2	2000-2FFF	PLD	8	Board identification, control and clock/signal routing	**A16-A31** (A15-A0)
3	3000-7FFF	-	8	Reserved	
4	8000-FFFF	DS3/T3 Framer	8	XRT79L72 DS3/T3 transceiver	**A17-A31** (A14-A0)
5	-	LM card	MPI/SPI(serial)	Universal Voice Board Line Module	-

3.2 PLD Register Map

On-board control PLD register map represented in the **Table 2**

Table 2

#	Address	Name	Functionality	Description
1	**2000**	**BRDID**	Read only	00h (Initial value)
2	**2001**	**BRDREV**	Read only	00h (Initial value)
3	**2002**	**PLDREV**	Read only	00h (Initial value)
4	**2003**	**PINSET**	Write/Read	T1/E1 Framer Configuration pin setting
5	**2004**	**CSR**	Write/Read	T1/E1 Framer MCLK and REFCLKIO Source
6	**2005**	**SYSCLK_TR**	Write/Read	T1/E1 Framer Tx and Rx SYSCLK Source
7	**2006**	**SYNCTSS**	Write/Read	T1/E1 Framer TSSYNCIO Source
8	**2007**	**TCSR1**	Write/Read	T1/E1 Framer TCLK Source, Ports 1…4 (/1.544MHz/2.048MHz/TCLKi-RCLKi/REFCLKIO)
9	**2008**	**TCSR2**	Write/Read	T1/E1 Framer TCLK Source, Ports 5…8 (/1.544MHz/2.048MHz/TCLKi-RCLKi/REFCLKIO)
10	**2009**	**TSYNCS1**	Write/Read	T1/E1 Framer TSYNC Source, Ports 8…1 (GND/TSYNC_out/TSYNCi-RSYNCi) T1/E1 Framer TSER Source, Ports 8..1 (Tri state/RSER/Input)
11	**200A**	**DS3SET**	Write/Read	DS3/E3 Framer Configuration pin setting
12	**200B**	**GCR**	Write/Read	General Control Register
13	200C	RSRV1	-	Reserved for future use
14	200D	RSRV2	-	Reserved for future use
15	200E	RSRV3	-	Reserved for future use
16	200F	RSRV4	-	Reserved for future use

3.3 PLD Control Register Description

- **BRDID**

Register Description: **Board ID Value**
Register Address: **2000**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Initial value is 00h

- **BRDREV**

Register Description: **Board Assembly Revision**
Register Address: **2001**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Initial value is 00h

- **PLDREV**

Register Description: **Board PLD Firmware Revision**
Register Address: **2002**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Initial value is 00h

- **PINSET**

Register Name: **PINSET**
Register Description: **DS26528 Configuration Pin Settings**
Register Address: **2003.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	DIGIOEN	TXEN	-	-	-	OUT_EN	JTRST	T1RST-
Default	0	0	0	0	0	0	0	0

PLD:
Bit 0: DS26528 DIGIOEN PIN
0 = Drive DS26528 DIGIO ENABLE pin Low (Tri-state all DS26528 digital I/O pins, if JTRST is low)
1 = Drive DS26528 DIGIO ENABLE pin High (Normal operation)
Bit 1: DS26528 TXEN PIN
0 = Drive DS26528 TX ENABLE pin Low (Tri-state TTIP and TRING)
1 = Drive DS26528 TX ENABLE pin High (Normal operation, drive TTIP and TRING with data)
Bit 5: DS26528 OUT_EN
0 = Enables normal operation mode
1 = TRI-State B_TXCLK and C_RXCLK TDM signals to avoid these signal's contention in case of operating with **MPC8360E-MDS-PB** host board when its on-board GETH interface is active.
Bit 6: DS26528 JTRST
0 = Enables normal operation mode
1 = Provide TRST signal to DS26528 device
Bit 7: DS26528 RST (T1RST-)
0 = Enables normal operation mode
1 = Provide RESET- signal to DS26528 device

- **CSR**

Register Name: **CSR**
Register Description: **DS26528 MCLK and REFCLKIO Source**
Register Address: **2004.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	MSRC0	MSRC1	-			-	RCSRC0	RCSRC1
Default	0	0	0	0	0	0	0	0

PLD:
Bits 0 and 1: DS26528 MCLK Source MSRC [0:1]
00 Drive MCLK with the 1.544MHz clock
10 Drive MCLK with the 2.048MHz clock
x1 MCLK connected to GND
Bits 6 and 7: DS26528 REFCLKIO Source RCSRC [6:7]
00 Drive REFCLKIO with the 1.544MHz clock
10 Drive REFCLKIO with the 2.048MHz clock
x1 Tri-state REFCLKIO (REFCLKIO pin OUTPUT)

- **SYSCLK_TR**

Register Name: **SYSCLK_TR**
Register Description: **DS26528 TSYSCLK and RSYSCLK Source**
Register Address: **2005.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TS0	TS1	-	-	-	-	RS0	RS1
Default	0	0	0	0	0	0	0	0

PLD:
Bits 0 and 1: DS26528 Port 1 TSYSCLK Source (TS0, TS1)
00 Drive TSYSCLK with the 1.544MHz clock
10 Drive TSYSCLK with the 2.048MHz clock
01 Drive TSYSCLK with 16.384MHz clock
11 Drive TSYSCLK with DS26528 port BPCLK
Bits 6 and 7: DS26528 Port 4 RSYSCLK Source (RS0, RS1)
00 Drive RSYSCLK with the 1.544MHz clock
10 Drive RSYSCLK with the 2.048MHz clock
01 Drive RSYSCLK with 16.384MHz clock
11 Drive RSYSCLK with DS26528 port BPCLK

- **SYNCTSS**

Register Name: **SYNCTSS**
Register Description: **DS26528 TSSYNCIO Source**
Register Address: **2006.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TSRC0	TSRC1	TSRC2	TSRC3	-	-	-	-
Default	0	0	0	0	0	0	0	0

PLD:
Bit 0 to 3: DS26528 TSSYNCIO Source Select TSRC [0:3]
0000 Not using transmit-side elastic store, tri-state - PLD pin connected to TSSYNCIO (weak pull-down, **TSSYNCIO pin OUTPUT**)
0001 Drive TSSYNCIO with RSYNC 1 **(08h)**
1001 Drive TSSYNCIO with RSYNC 2 **(09h)**
0101 Drive TSSYNCIO with RSYNC 3 **(0Ah)**
1101 Drive TSSYNCIO with RSYNC 4 **(0Bh)**
0011 Drive TSSYNCIO with RSYNC 5 **(0Ch)**
1011 Drive TSSYNCIO with RSYNC 6 **(0Dh)**
0111 Drive TSSYNCIO with RSYNC 7 **(0Eh)**
1111 Drive TSSYNCIO with RSYNC 8 **(0Fh)**
Note: When driving TSSYNCIO with RSYNCx, the corresponding DS26528 port should be configured such that RSYNCx is an output (RIOCR.2 = 0).

- **TCSR1**

Register Name: **TCSR1 (n = 1 to 4)**
Register Description: **DS26528 TCLK Source Ports 1-4**
Register Address: **2007.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TDS10	TDS11	TDS20	TDS21	TDS30	TDS31	TDS40	TDS41
Default	0	0	0	0	0	0	0	0

PLD:
Bits 0, 1: DS26528 Port 1 TCLK Source TDS [10:11]
00 Drive TCLK1 with the 1.544MHz clock
10 Drive TCLK1 with the 2.048MHz clock
01 Drive TCLK1 with RCLK1
11 Drive TCLK1 with REFCLKIO
Bits 2, 3: DS26528 Port 2 TCLK Source TDS [20:21]
00 Drive TCLK2 with the 1.544MHz clock
10 Drive TCLK2 with the 2.048MHz clock
01 Drive TCLK2 with RCLK2
11 Drive TCLK2 with REFCLKIO
Bits 4, 5: DS26528 Port 3 TCLK Source TDS [30:31]
00 Drive TCLK3 with the 1.544MHz clock
10 Drive TCLK3 with the 2.048MHz clock
01 Drive TCLK3 with RCLK3
11 Drive TCLK3 with REFCLKIO
Bits 6, 7: DS26528 Port 4 TCLK Source TDS [40:41]
00 Drive TCLK4 with the 1.544MHz clock
10 Drive TCLK4 with the 2.048MHz clock
01 Drive TCLK4 with RCLK4
11 Drive TCLK4 with REFCLKIO

- **TCSR2**

Register Name: **TCSR2 (n = 5 to 8)**
Register Description: **DS26528 TCLK Source Ports 5-8**
Register Address: **2008.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TDS50	TDS51	TDS60	TDS61	TDS70	TDS71	TDS80	TDS81
Default	0	0	0	0	0	0	0	0

PLD:
Bits 0, 1: DS26528 Port 5 TCLK Source TDS [50:51]
00 Drive TCLK5 with the 1.544MHz clock
10 Drive TCLK5 with the 2.048MHz clock
01 Drive TCLK5 with RCLK5
11 Drive TCLK5 with REFCLKIO
Bits 3, 2: DS26528 Port 6 TCLK Source TDS [60:61]
00 Drive TCLK6 with the 1.544MHz clock
10 Drive TCLK6 with the 2.048MHz clock
01 Drive TCLK6 with RCLK6
11 Drive TCLK6 with REFCLKIO
Bits 5, 4: DS26528 Port 7 TCLK Source TDS [70:71]
00 Drive TCLK7 with the 1.544MHz clock
10 Drive TCLK7 with the 2.048MHz clock
01 Drive TCLK7 with RCLK7
11 Drive TCLK7 with REFCLKIO
Bits 7, 6: DS26528 Port 8 TCLK Source TDS [80:81]
00 Drive TCLK8 with the 1.544MHz clock
10 Drive TCLK8 with the 2.048MHz clock
01 Drive TCLK8 with RCLK8
11 Drive TCLK8 with REFCLKIO

- **TSYNCS1**

Register Name: **TSYNCS1 (n = 1 to 4)**
Register Description: **DS26528 TSYNC and TSER Source Ports 1-8**
Register Address: **2009.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TSSTATE	TSSRC	-	-	-	-	TSERSTATE	TSERSRC
Default	0	0	0	0	0	0	0	0

PLD:
Bit 0: DS26528 Port 1-8 TSYNC State TSSTATE [0]
0 TSYNC1-8 are 3-State (TSYNC1-8 are OUTPUT)
1 TSYNC1-8 are INPUT
Bit 1: DS26528 Ports 1-8 TSYNC Source TSSRC [1]
0 TSYNC1-8 are connected to RSYNC1-8 correspondingly
1 TSYNC1-8 are connected to GND
Bit 6: DS26528 Ports 1-8 TSER State TSERSTATE [6]
0 TSER1-8 are INPUT
1 TSER1-8 are 3-State (Disconnected)
Bit 7: DS26528 Ports 1-8 TSER Source TSERSRC [7]
0 TSER1-8 are connected to Host TDM A-H correspondingly
1 TSER1-8 are connected to RSER1-8 correspondingly

- **DS3SET**

Register Name: **DS3SET**
Register Description: **DS3/E3 Framer Configuration pin setting**
Register Address: **200A.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	TXON	NIBBLE	DBEN	MODE	-	-	TRST	RST
Default	0	0	0	0	0	0	0	0

PLD:
Bit 0: XRT79L72 TXON pin
0 = Disables the Transmit Output Drivers. In this setting, the TTIP and TRING output pins will be tri-stated
1 = Enables the Transmit Output Drivers if the individual register bits are set to "1". In this setting, the TTIP and TRING output pins will be enabled.
Bit 1: XRT79L72 NibbleIntf pin
0 = configures each of Transmit Payload Data Input Interface and the Receive Payload Data Output Interface blocks to operate in the Nibble-Parallel Mode
1 = Configures each of Transmit Payload Data Input Interface and the Receive Payload Data Output Interface blocks to operate in the Serial Mode
Bit 2: XRT79L72 DBEN pin
0 = Tri-states the Bi-directional Data Bus.
1 = Enables the Bi-directional Data bus.
Bit 3: XRT79L72 MODE
0 = Enables normal operation mode
1 = Enables local timing mode (CLKOUT used as TXINCLK)
Bit 6: XRT79L72 TRST
0 = Enables normal operation mode
1 = Provide TRST signal to XRT79L72 device
Bit 7: XRT79L72 RST
0 = Enables normal operation mode
1 = Provide RESET signal to XRT79L72 device

- **GCR**

Register Name: **GCR**
Register Description: **General Control Register**
Register Address: **200B.** Reset value is **00h**

LB Bit #	7	6	5	4	3	2	1	0
PLD Bit #	0	1	2	3	4	5	6	7
	LSB							MSB
Name	BEIT	LCE	LRST	LCC0	LCC1	LCC2	LCC3	BRST
Default	0	0	0	0	0	0	0	0

PLD:
Bit 0: Board External Interface Type (BEIT)
0 = Enables T1/E1 external interface type
1 = Enables DS3/E3 external interface type.
Bit 1: SLIC-SLAC Legerity Card Clock Enable (LCE)
0 = Line Module Le71HR0826 clock disabled (Log.”0”)
1 = Drive Line Module Le71HR0826 with the T1/E1 framer BPCLK signal
Bit 2: SLIC-SLAC Legerity Card Reset (LRST)
0 = Enables normal operation mode
1 = Provide RESET signal to Line Module Le71HR0826
Bit 3 - 6: SLIC-SLAC Legerity Card Channel Connection (LCC [0:3])
xxx0 = Disconnect Line Module Le71HR0826 from Host TDM **(default)**
0001 = LM card connected to Host TDM channel A instead of T1/E1 framer channel #1
1001 = LM card connected to Host TDM channel B instead of T1/E1 framer channel #2
0101 = LM card connected to Host TDM channel C instead of T1/E1 framer channel #3
1101 = LM card connected to Host TDM channel D instead of T1/E1 framer channel #4
0011 = LM card connected to Host TDM channel E instead of T1/E1 framer channel #5
1011 = LM card connected to Host TDM channel F instead of T1/E1 framer channel #6
0111 = LM card connected to Host TDM channel G instead of T1/E1 framer channel #7
1111 = LM card connected to Host TDM channel H instead of T1/E1 framer channel #8
Bit 7: Board RESET (BRST)
0 = Enables normal operation mode
1 = Provide RESET signal to the following board populated components: T1/E1 framer, DS3/T3 framer and LM card

Section4 PQ-MDS-T1 Configuration scenario's

4.1 T1 mode possible scenario

The corresponding data/clock flow for 1 channel represented in the **Figure 2**
Setting PLD for this mode represented in the **Table 3**

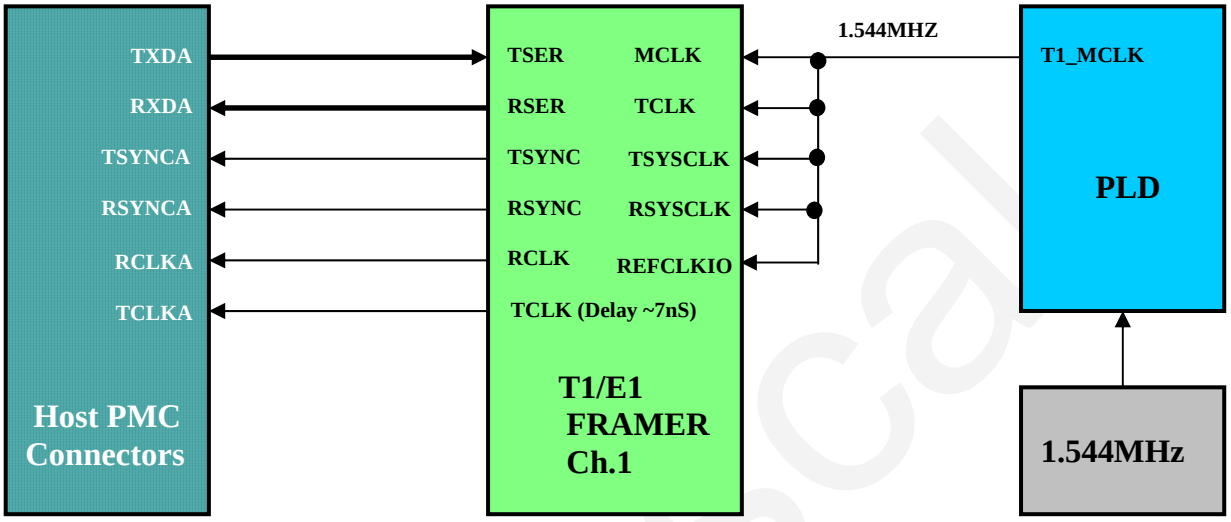

Figure 2

Table 3

#	Register		Setting	Comment
	Address	Name		
1	**2003**	PINSET	**0x03**	T1 Framer DIGIO and TXEN pins are active
2	**2004**	CSR	**0x00**	Drive MCLK and REFCLKIO with 1.544MHz
3	**2005**	SYSCLK_TR	**0x00**	Drive TSYSCLK and RSYSCLK with 1.544MHz
4	**2006**	SYNCTSS	**0x00**	Not using transmit-side elastic store. TSSYNCIO pin Output
5	**2007**	TCSR1	**0x00**	Drive TCLK1…4 with 1.544MHz
6	**2008**	TCSR2	**0x00**	Drive TCLK5…8 with 1.544MHz
7	**2009**	TSYNCS1	**0x00**	TSYNC1…8 are Output. TSER1…8 are connected to Host TDM TXD(A-H) correspondingly
8	**200A**	DS3SET	**0x00**	Disables the DS3 framer Transmit Output Drivers, 3-state DATA-bus, Nibble normal mode configured.
9	**200B**	GCR	**0x00**	T1/E1 external interface type selected. Drive SLIC-SLAC card with 1.544MHz and disconnect from Host TDM

4.2 E1 mode possible scenario

The corresponding data/clock flow for 1 channel represented in the **Figure 3**
Setting PLD for this mode represented in the **Table 4**

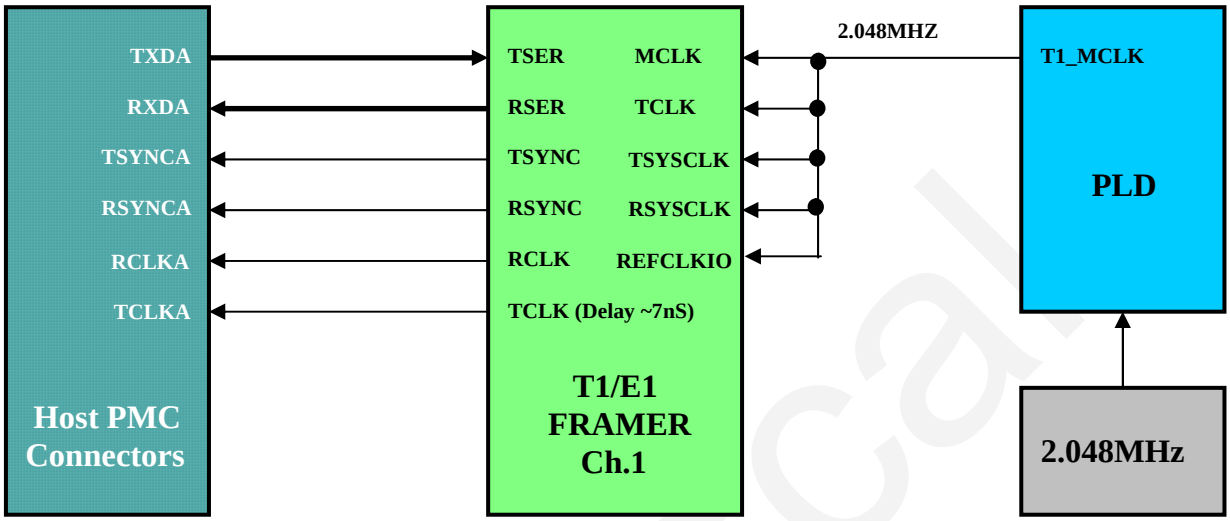

Figure 3

Table 4

#	Register		Setting	Comment
	Address	**Name**		
1	**2003**	PINSET	**0x03**	T1 Framer DIGIO and TXEN pins are active
2	**2004**	CSR	**0x41**	Drive MCLK and REFCLKIO with 2.048MHz
3	**2005**	SYSCLK_TR	**0x41**	Drive TSYSCLK and RSYSCLK with 2.048MHz
4	**2006**	SYNCTSS	**0x00**	Not using transmit-side elastic store. TSSYNCIO pin Output
5	**2007**	TCSR1	**0x55**	Drive TCLK1…4 with 2.048MHz
6	**2008**	TCSR2	**0x55**	Drive TCLK5…8 with 2.048MHz
7	**2009**	TSYNCS1	**0x00**	TSYNC1…8 are Output. TSER1…8 are connected to Host TDM TXD(A-H) correspondingly
8	**200A**	DS3SET	**0x00**	Disables the DS3 framer Transmit Output Drivers, 3-state DATA-bus, Nibble normal mode configured.
9	**200B**	GCR	**0x00**	T1/E1 external interface type selected. Drive SLIC-SLAC card with 1.544MHz and disconnect from Host TDM

4.3 DS3 nibble mode possible scenario

The corresponding data/clock flow for 1 channel represented in the **Figure 4**
Setting PLD for this mode represented in the **Table 5**

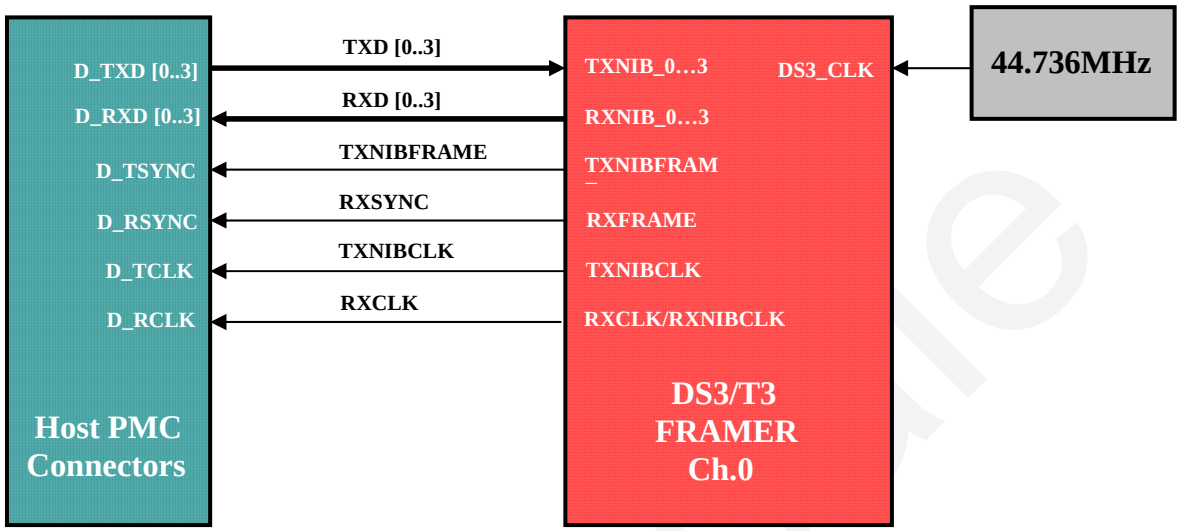

Figure 4

Table 5

#	Register		Setting	Comment
	Address	Name		
1	**2003**	PINSET	**0x00**	T1 Framer DIGIO and TXEN pins are Tri-state
2	**2004**	CSR	**0x82**	MCLK connected to GND. REFCLKIO is Tri-state
3	**2005**	SYSCLK_TR	**0xC3**	Drive TSYSCLK and RSYSCLK with BPCLK
4	**2006**	SYNCTSS	**0x00**	Not using transmit-side elastic store. TSSYNCIO pin Output
5	**2007**	TCSR1	**0xFF**	Drive TCLK1…4 with REFCLKIO
6	**2008**	TCSR2	**0xFF**	Drive TCLK5…8 with REFCLKIO
7	**2009**	TSYNCS1	**0x40**	TSYNC1…8 are Output. TSER1…8 are Tri-state (Disconnected)
8	**200A**	DS3SET	**0x05**	Enables the DS3 framer Transmit Output Drivers, DATA-bus, Nibble normal mode configured.
9	**200B**	GCR	**0x05**	DS3/E3 external interface type selected. SLIC-SLAC card constantly RESET and disconnect from Host TDM

4.4 DS3 serial mode possible scenario

The corresponding data/clock flow for 1 channel represented in the **Figure 5**
Setting PLD for this mode represented in the **Table 6**

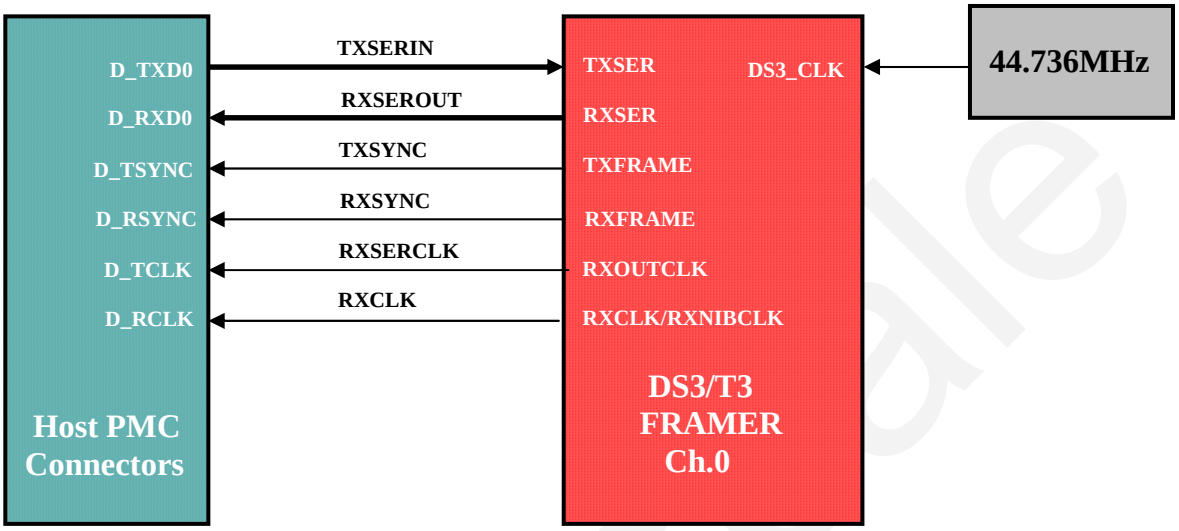

Figure 5

Table 6

#	Register		Setting	Comment
	Address	**Name**		
1	**2003**	PINSET	**0x00**	T1 Framer DIGIO and TXEN pins are Tri-state
2	**2004**	CSR	**0x82**	MCLK connected to GND. REFCLKIO is Tri-state
3	**2005**	SYSCLK_TR	**0xC3**	Drive TSYSCLK and RSYSCLK with BPCLK
4	**2006**	SYNCTSS	**0x00**	Not using transmit-side elastic store. TSSYNCIO pin Output
5	**2007**	TCSR1	**0xFF**	Drive TCLK1…4 with REFCLKIO
6	**2008**	TCSR2	**0xFF**	Drive TCLK5…8 with REFCLKIO
7	**2009**	TSYNCS1	**0x40**	TSYNC1…8 are Output. TSER1…8 are Tri-state (Disconnected)
8	**200A**	DS3SET	**0x07**	Enables the DS3 framer Transmit Output Drivers, DATA-bus, Serial normal mode configured.
9	**200B**	GCR	**0x05**	DS3/E3 external interface type selected. SLIC-SLAC card constantly RESET and disconnect from Host TDM

4.5 SLIC-SLAC LM card possible scenario

The corresponding data/clock flow for Channel E represented in the **Figure 6**
Setting PLD for this mode represented in the **Table 7**

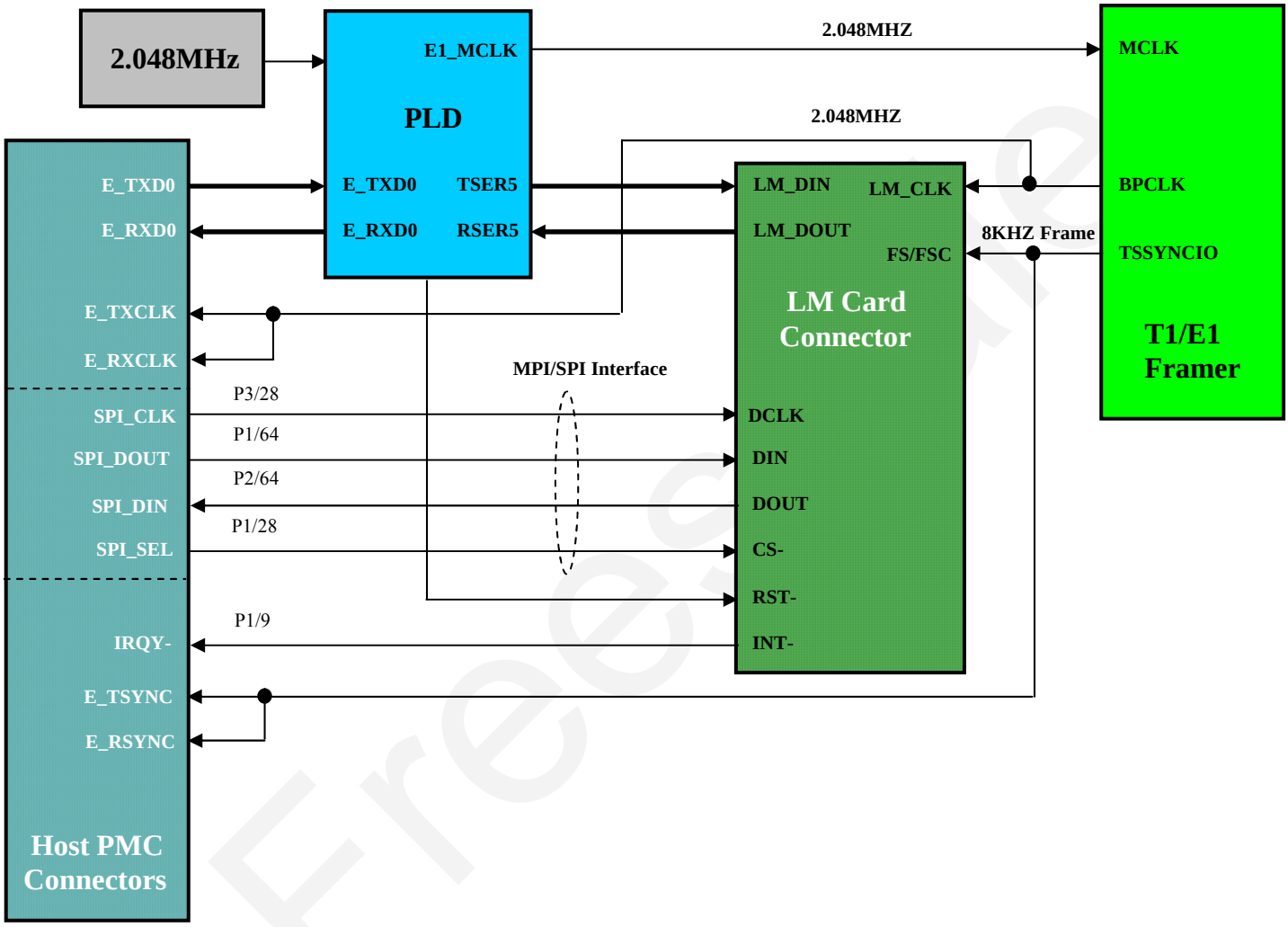

Figure 6

Table 7

#	Register		Setting	Comment
	Address	Name		
1	**2003**	PINSET	**0x03**	T1 Framer DIGIO and TXEN pins are active
2	**2004**	CSR	**0x41**	Drive MCLK and REFCLKIO with 2.048MHz
3	**2005**	SYSCLK_TR	**0x41**	Drive TSYSCLK and RSYSCLK with 2.048MHz
4	**2006**	SYNCTSS	**0x00**	Not using transmit-side elastic store. TSSYNCIO pin Output
5	**2007**	TCSR1	**0x55**	Drive TCLK1…4 with 2.048MHz
6	**2008**	TCSR2	**0x55**	Drive TCLK5…8 with 2.048MHz
7	**2009**	TSYNCS1	**0x00**	TSYNC1…8 are Output. TSER1…8 are connected to Host TDM TXD(A-H) correspondingly
8	**200A**	DS3SET	**0x00**	Disables the DS3 framer Transmit Output Drivers, 3-state DATA-bus, Nibble normal mode configured.
9	**200B**	GCR	**0x62**	T1/E1 external interface type selected. Drive SLIC-SLAC card with E1_BPCLK and connect to Host TDM Channel E instead of T1/E1 framer channel #5

Section5 PQ-MDS-T1 module floor plan

The module realized as PMC form-factor mezzanine card enclosed all mentioned above components besides SLIC-SLAC LM card. This add-in card could be connected to the board through special LM-connector.
PQ-MDS-T1 layout represented in the following **Figure 7 and 8**
Draft represented in the **Figure 7** assumes that the external Add-in Card enclosed 8 RJ-45 female connectors provide standard T1/E1 interface while interconnect with **PQ-MDS-T1** module by extra mini edge-card socket. The advantage of the solution that the **PQ-MDS-T1** module complies with PMC-mezzanine card height standard (without SLIC-SLAC LM card assembled)
Figure 8 represented side view of the assembly
In case when **PQ-MDS-PIB** board with **PQ-MDS-T1** module and LM card assembled on it are inserted into the ATCA enclosure it's occupy two adjoining slots.

Figure 9 represented CS assembly while **Figure 10** represented PS assembly of the module

Figure 11 represented CS assembly of the Add-in-Card with 8 RJ-45 connectors which targeted to provide 8 T1/E1 standard connectors.

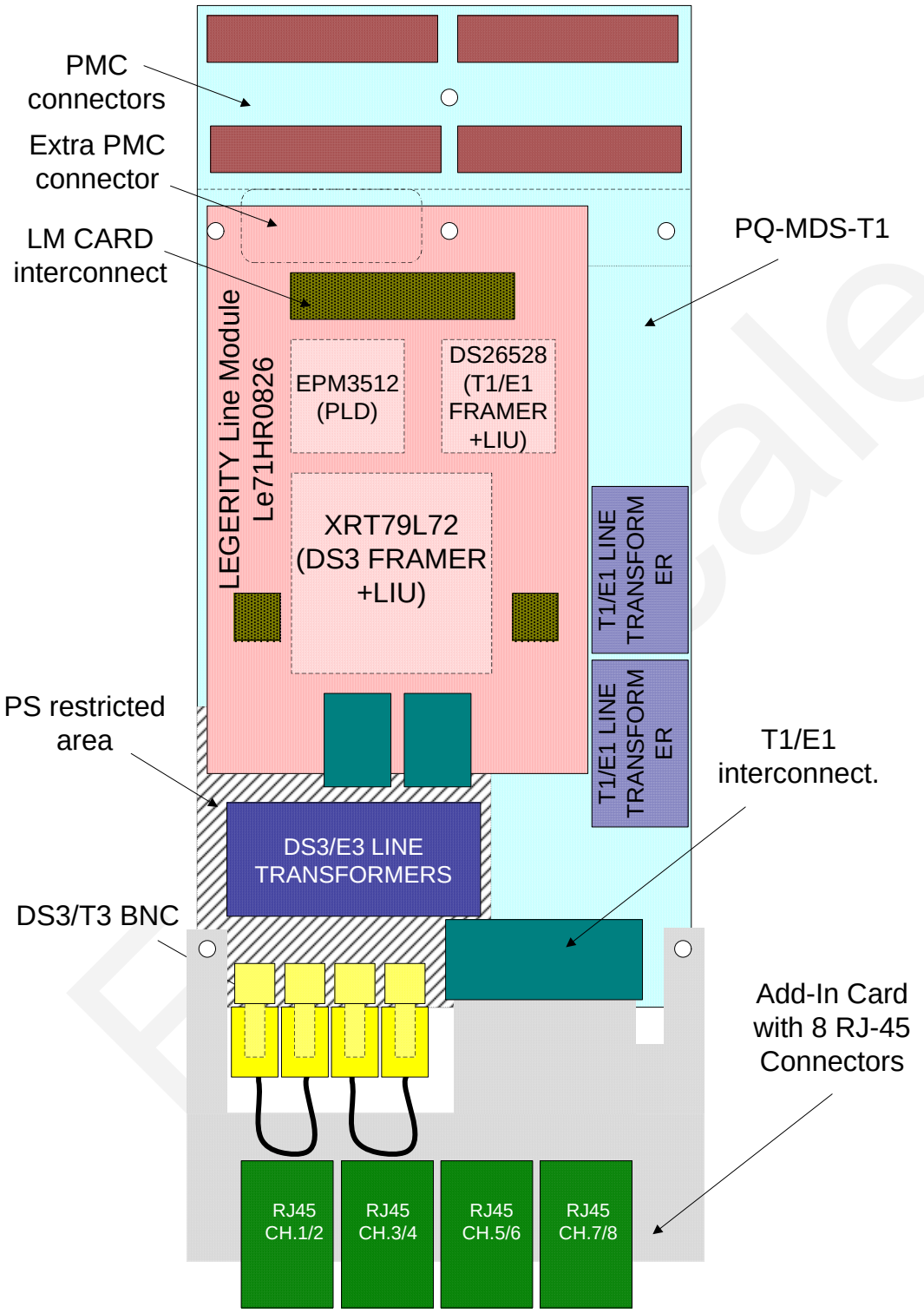
PMC connectors
Extra PMC connector
LM CARD interconnect
PQ-MDS-T1
LEGERITY Line Module Le71HR0826
EPM3512 (PLD)
DS26528 (T1/E1 FRAMER +LIU)
XRT79L72 (DS3 FRAMER +LIU)
T1/E1 LINE TRANSFORM ER
T1/E1 LINE TRANSFORM ER
PS restricted area
T1/E1 interconnect.
DS3/E3 LINE TRANSFORMERS
DS3/T3 BNC
Add-In Card with 8 RJ-45 Connectors
RJ45 CH.1/2
RJ45 CH.3/4
RJ45 CH.5/6
RJ45 CH.7/8

Figure 7

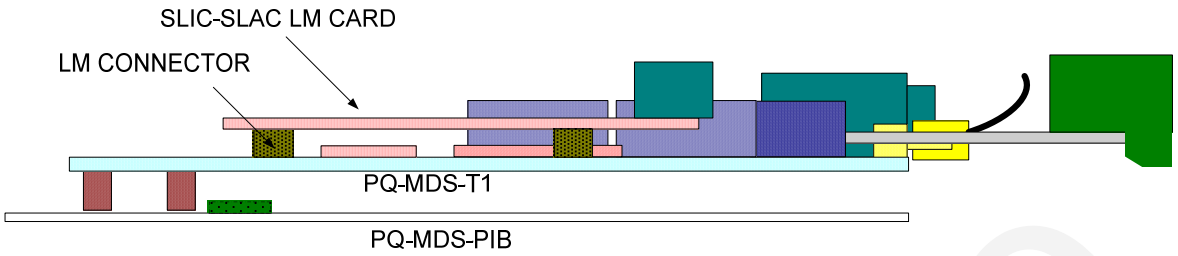

Figure 8

SLIC-SLAC Module assembled

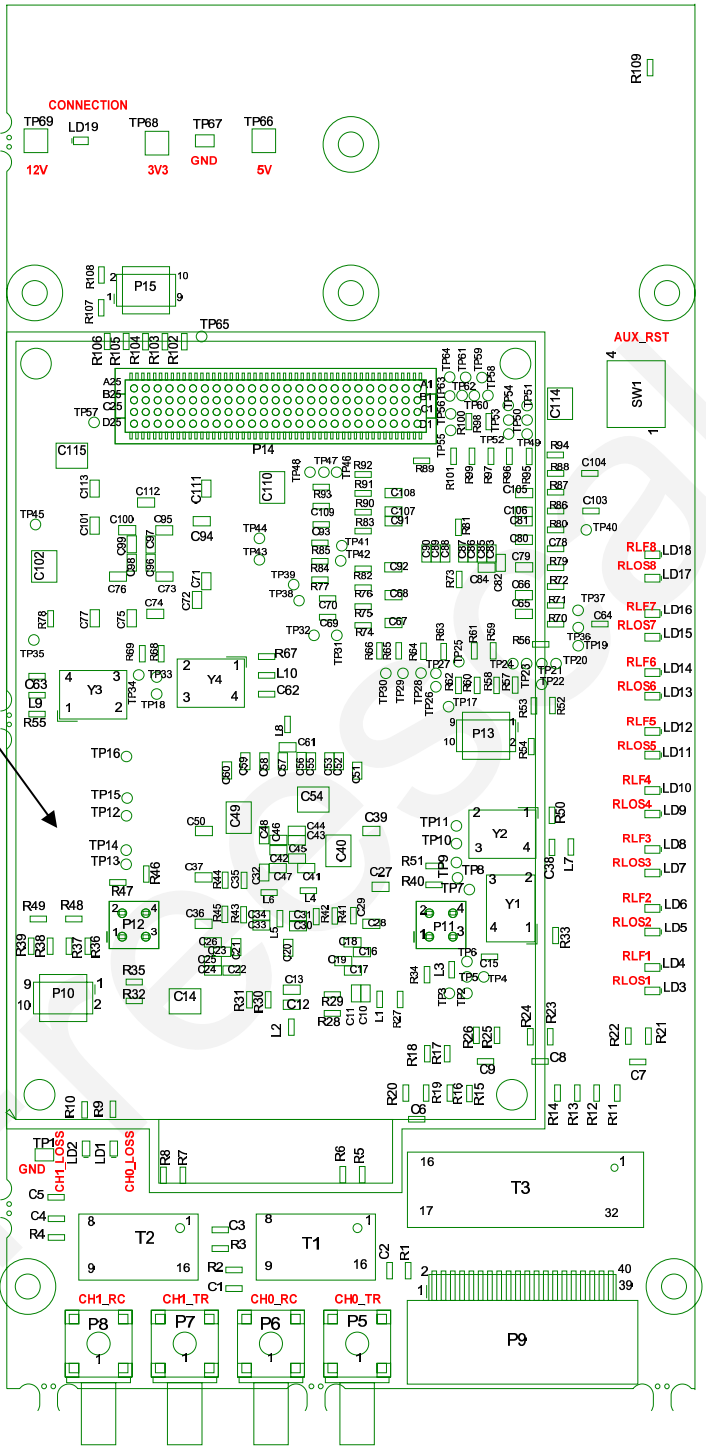

Figure 9

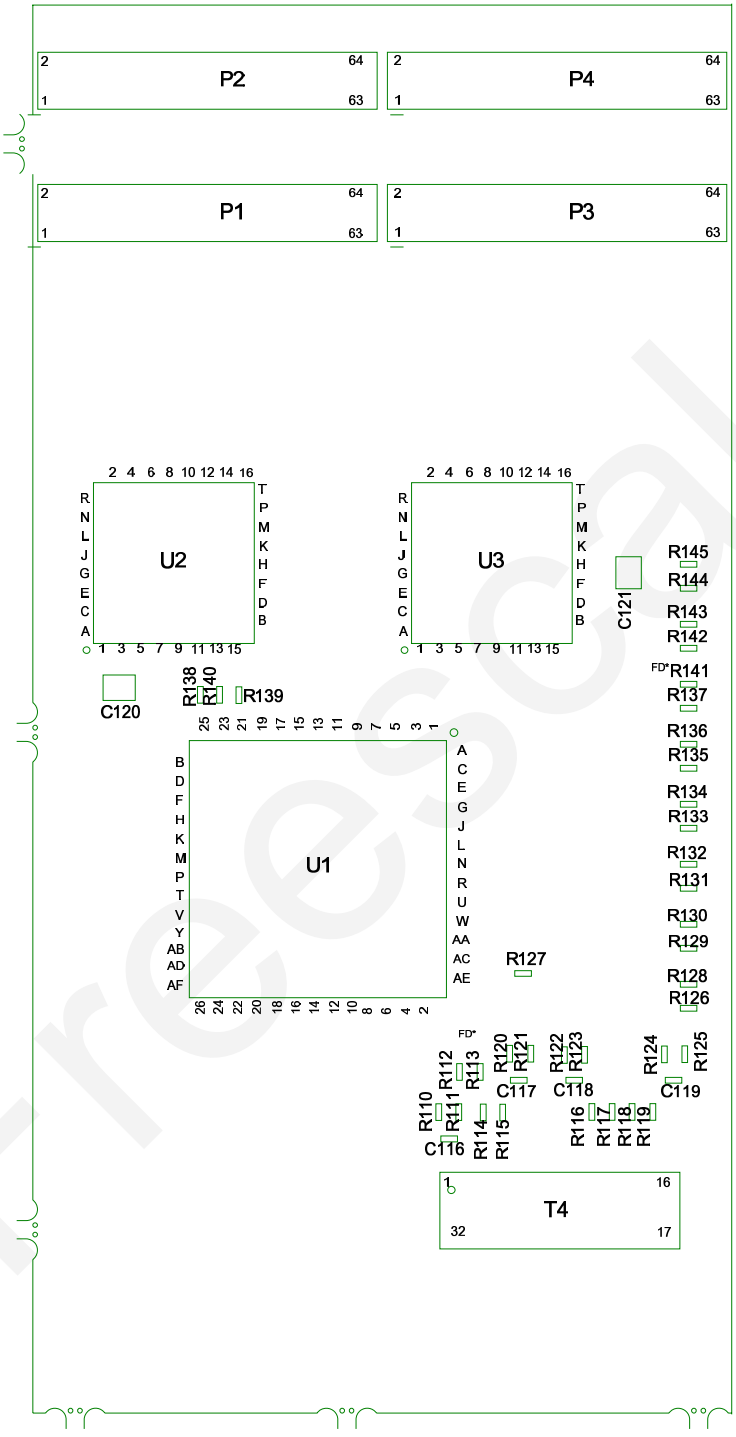
P2
P4
P1
P3
U2
U3
U1
T4
C120
C121
C116
C117
C118
C119
R127
R138
R140
R139
R145
R144
R143
R142
R141
R137
R136
R135
R134
R133
R132
R131
R130
R129
R128
R126
R125
R124
R123
R122
R121
R120
R119
R118
R117
R116
R115
R114
R113
R112
R111
R110

Figure 10

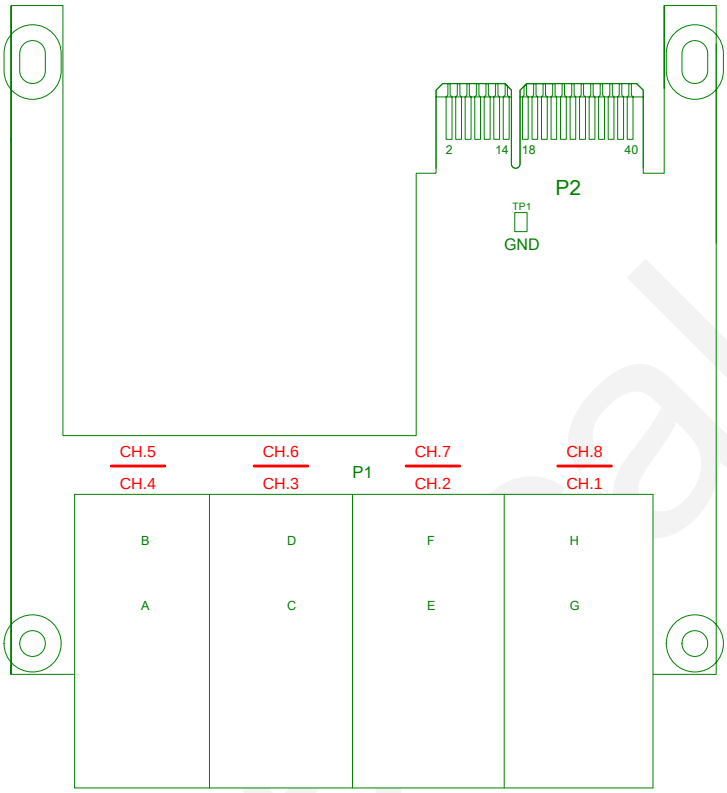

Figure 11

Section6 PQ-MDS-T1 DS3/T3 Functionality

Block-diagram of the interconnections between XRT79L72 and Host CPU MPC83xx family (1 channel) represented in the **Figure 12**

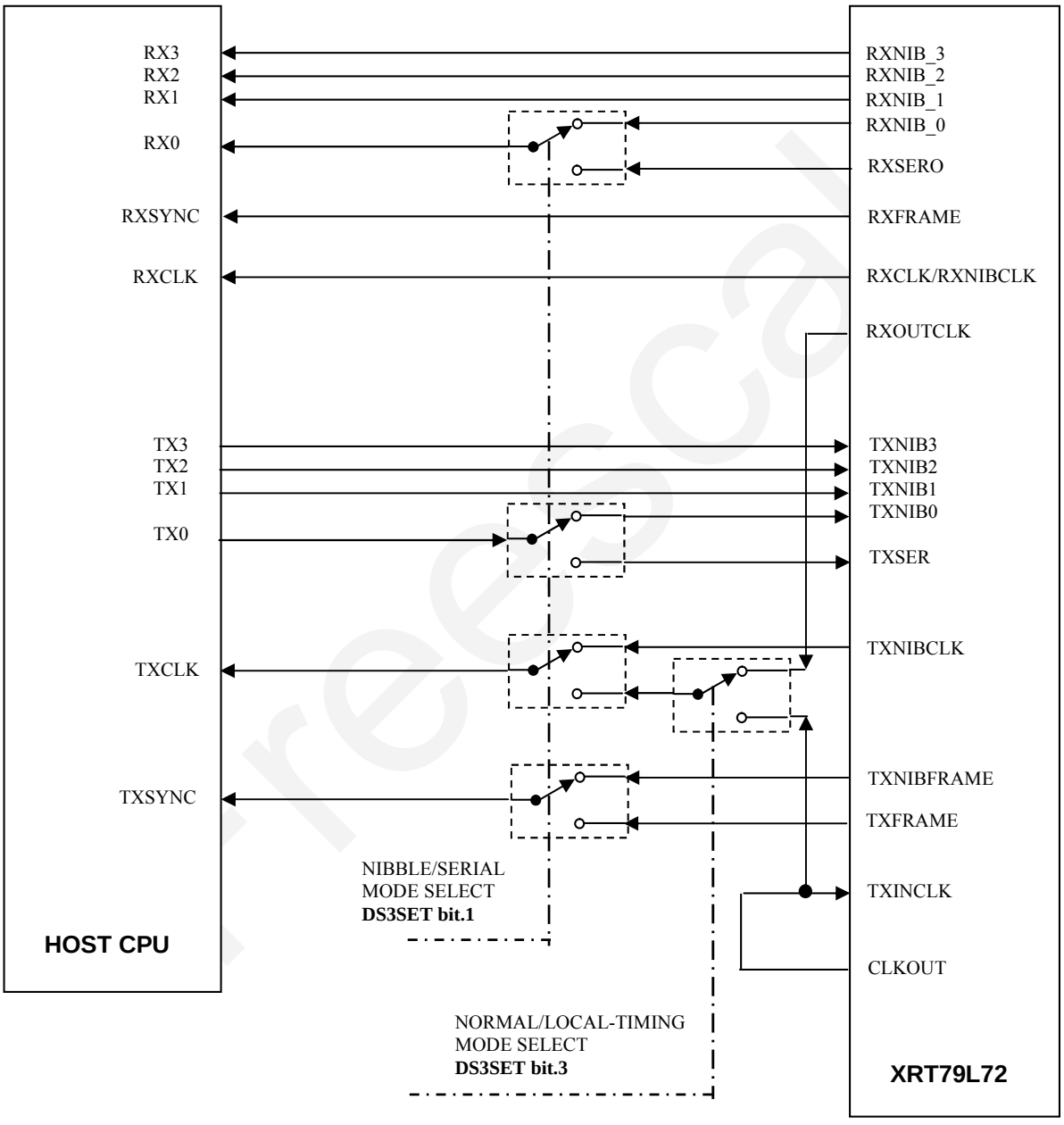

Figure 12

Section7 PQ-MDS-T1 T1/E1/J1 Functionality

Block-diagram of the interconnections between DS26528 and Host CPU MPC83xx family (1 channel) represented in the **Figure 13**

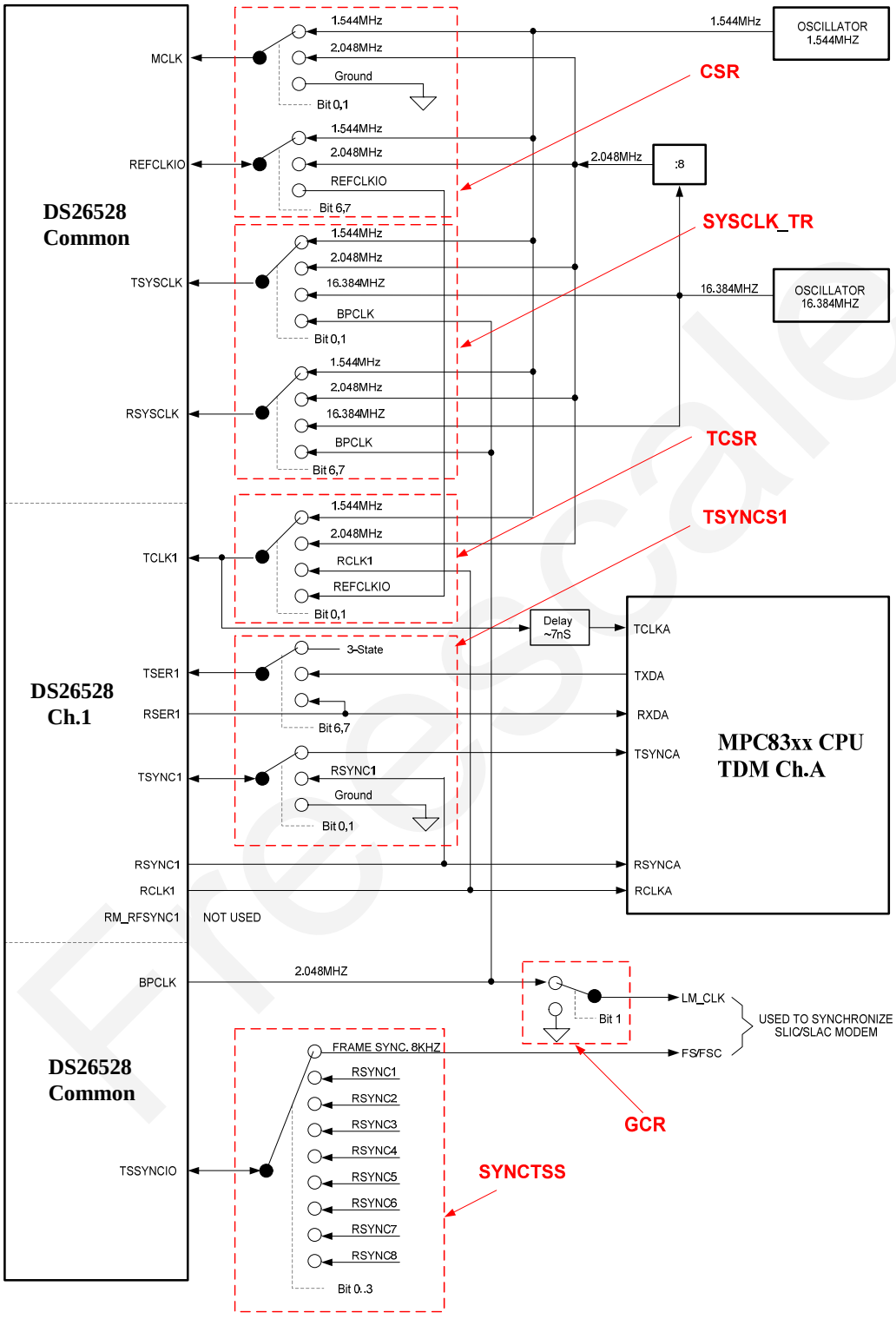
DS26528
Common
MCLK
REFCLKIO
TSYSCLK
RSYSCLK
1.544MHz
2.048MHz
Ground
Bit 0,1
REFCLKIO
Bit 6,7
16.384MHZ
BPCLK
OSCILLATOR
1.544MHZ
OSCILLATOR
16.384MHZ
:8
CSR
SYSCLK_TR
TCSR
TSYNCS1
DS26528
Ch.1
TCLK1
RCLK1
TSER1
RSER1
TSYNC1
RSYNC1
3-State
Delay
~7nS
TCLKA
TXDA
RXDA
TSYNCA
RSYNCA
RCLKA
MPC83xx CPU
TDM Ch.A
RM_RFSYNC1
NOT USED
BPCLK
2.048MHZ
Bit 1
LM_CLK
FS/FSC
USED TO SYNCHRONIZE
SLIC/SLAC MODEM
GCR
DS26528
Common
FRAME SYNC. 8KHZ
RSYNC2
RSYNC3
RSYNC4
RSYNC5
RSYNC6
RSYNC7
RSYNC8
Bit 0..3
TSSYNCIO
SYNCTSS

Figure 13

Section8 PQ-MDS-T1 PMC connectors pin mapping

Pin-mapping of the **PQ-MDS-T1** mezzanine card set connectors used to interface to **PQ-MDS-PIB** board represented in the **Table 8**

Table 8

Connector P1							
#	**Standard Function**	**Module Function**	**Note**	**#**	**Standard Function**	**Module Function**	**Note**
1	TCK	**Optional**	DFT usage	2	-12V	-12V	Check Connection
3	GND	GND		4	INTA#	**G_RSYNC**	
5	INTB#	-		6	INTC#	-	
7	BUSMODE1#	-		8	5V	5V	
9	INTD#	**INT-**		10	PCI-RSRVD	**C_TSYNC**	
11	GND	GND		12	3.3Vaux	3.3V	
13	CLK	-		14	GND	GND	
15	GND	GND		16	GNT#	**C_RXD0**	
17	REQ#	**G_TXCLK**		18	5V		
19	V(I/O)	3.3V		20	AD31	**H_RXCLK**	
21	AD28	-		22	AD27	-	
23	AD25	-		24	GND	GND	
25	GND	GND		26	C/BE3#	-	
27	AD22	-		28	AD21	-	
29	AD19	-		30	5V		
31	V(I/O)	3.3V		32	AD17	**D_TXD1**	
33	FRAME#	**E_RXD1**		34	GND	GND	
35	GND	GND		36	IRDY#	-	
37	DEVSEL#	-		38	5V	5V	
39	GND			40	LOCK#	-	
41	PCI-RSRVD	**H_TSYNC**		42	PCI-RSRVD	-	
43	PAR	-		44	GND	GND	
45	V(I/O)	3.3V		46	AD15	-	
47	AD12	**B_RXD0**		48	AD11	**A_RXD0**	
49	AD09	**D_RXD2**		50	5V	5V	
51	GND	GND		52	C/BE0#	**E_TXD2**	
53	AD06	-		54	AD05	**H_RXD0**	
55	AD04	**G_RXD0**		56	GND	GND	
57	V(I/O)	3.3V		58	AD03	**G_TSYNC**	
59	AD02	-		60	AD01	-	
61	AD00	-		62	5V	5V	
63	GND	GND		64	REQ64#	**SPI-DOUT**	

Continue Table 8

Connector P2							
#	Standard Function	Module Function	Note	#	Standard Function	Module Function	Note
1	12V	12V		2	TRST#	**Optional**	DFT usage
3	TMS	**Optional**	DFT usage	4	TDO	**Optional**	DFT usage
5	TDI	**Optional**	DFT usage	6	GND	GND	
7	GND	GND		8	PCI-RSRVD	-	
9	PCI-RSRVD	-		10	PCI-RSRVD	-	
11	BUSMODE2#	-		12	3.3V	3.3V	
13	RST#	**G_TXD0**		14	BUSMODE3#	-	
15	3.3V	3.3V		16	BUSMODE4#	-	
17	PME#	-		18	GND	GND	
19	AD30	**A_TSYNC**		20	AD29	**D_TXD3**	
21	GND	GND		22	AD26	-	
23	AD24	**B_TXD0**		24	3.3V	3.3V	
25	IDSEL	-		26	AD23	**D_RXD1**	
27	3.3V	3.3V		28	AD20	-	
29	AD18	**D_TXD2**		30	GND	GND	
31	AD16	-		32	C/BE2#	-	
33	GND	GND		34	PMC-RSRVD	**D_RXCLK**	
35	TRDY#	**E_RXD2**		36	3.3V	3.3V	
37	GND	GND		38	STOP#	-	
39	PERR#	**E_RXD3**		40	GND	GND	
41	3.3V	3.3V		42	SERR#	**E_TXD3**	
43	C/BE1#	-		44	GND	GND	
45	AD14	**E_TXD1**		46	AD13	**A_TXD0**	
47	M66EN	-		48	AD10	**D_RXD3**	
49	AD08	-		50	3.3V	3.3V	
51	AD07	**C_RSYNC**		52	PMC-RSRVD	**F_RXCLK**	
53	3.3V	3.3V		54	PMC-RSRVD	-	
55	PMC-RSRVD	**C_TXD0**		56	GND	GND	
57	PMC-RSRVD	**A_RSYNC**		58	PMC-RSRVD	**E_TXCLK**	
59	GND	GND		60	PMC-RSRVD		
61	ACK64#	**G_RXCLK**		62	3.3V	3.3V	
63	GND	GND		64	PMC-RSRVD	**SPI-DIN**	

Continue Table 8

Connector P3							
#	Standard Function	Module Function	Note	#	Standard Function	Module Function	Note
1	PCI-RSRVD	**H_TXCLK**		2	GND	GND	
3	GND	GND		4	C/BE7#	**B_TSYNC**	
5	C/BE6#	-		6	C/BE5#	**B_TXCLK**	
7	C/BE4#	**E_RXCLK**		8	GND	GND	
9	V(I/O)	3.3V		10	PAR64	**B_RXCLK**	
11	AD63	**F_TXD0**		12	AD62	**B_RSYNC**	
13	AD61	-		14	GND	GND	
15	GND	GND		16	AD60	**F_TSYNC**	
17	AD59	**F_RXD0**		18	AD58	**F_RSYNC**	
19	AD57	-		20	GND	GND	
21	V(I/O)	3.3V		22	AD56	**F_TXCLK**	
23	AD55	-		24	AD54	-	
25	AD53	**A_RXCLK**		26	GND	GND	
27	GND	GND		28	AD52	**SPI-CLK**	
29	AD51	**A_TXCLK**		30	AD50	**H_RSYNC**	
31	AD49	**E_RSYNC**		32	GND	GND	
33	GND	GND		34	AD48	**H_TXD0**	
35	AD47	**E_TSYNC**		36	AD46	-	
37	AD45	**E_RXD0**		38	GND	GND	
39	V(I/O)	3.3V		40	AD44	-	
41	AD43	**E_TXD0**		42	AD42	-	
43	AD41	**C_RXCLK**		44	GND	GND	
45	GND	GND		46	AD40	-	
47	AD39	**C_TXCLK**		48	AD38	-	
49	AD37	**D_TSYNC**		50	GND	GND	
51	GND	GND		52	AD36	-	
53	AD35	**D_TXD0**		54	AD34	-	
55	AD33	**D_RSYNC**		56	GND	GND	
57	V(I/O)	3.3V		58	AD32	-	
59	PCI-RSRVD	**D_RXD0**		60	PCI-RSRVD	**SPI-SEL**	
61	PCI-RSRVD	**D_TXCLK**		62	GND	GND	
63	GND	GND		64	PCI-RSRVD	-	

Continue Table 8

Connector P4							
#	Standard Function	Module Function	Note	#	Standard Function	Module Function	Note
1	I/O	**LB_D0**		2	I/O	**LB_D1**	
3	I/O	**LD_D2**		4	I/O	**LB_D3**	
5	I/O	-		6	I/O	**LB_D5**	
7	I/O	**LB_D4**		8	I/O	**LB_D7**	
9	I/O	**LB_D6**		10	I/O	**GND**	
11	I/O	-		12	I/O	-	
13	I/O	-		14	I/O	-	
15	I/O	**GND**		16	I/O	-	
17	I/O	-		18	I/O	-	
19	I/O	-		20	I/O	**GND**	
21	I/O	**LB_A16**		22	I/O	**LB_A17**	
23	I/O	**LB_A18**		24	I/O	**LB_A19**	
25	I/O	**GND**		26	I/O	**LB_A21**	
27	I/O	**LB_A20**		28	I/O	**LB_A23**	
29	I/O	**LB_A22**		30	I/O	**GND**	
31	I/O	**LB_A24**		32	I/O	**LB_A25**	
33	I/O	**LB_A26**		34	I/O	**LB_A27**	
35	I/O	**GND**		36	I/O	**LB_A29**	
37	I/O	**LB_A28**		38	I/O	**LB_A31**	
39	I/O	**LB_A30**		40	I/O	**GND**	
41	I/O	-		42	I/O	-	
43	I/O	-		44	I/O	**LB_CS5#**	
45	I/O	**GND**		46	I/O	-	
47	I/O	**LB_RD#**		48	I/O	-	
49	I/O	-		50	I/O	**GND**	
51	I/O	**LB_RDY#**		52	I/O	-	
53	I/O	-		54	I/O	-	
55	I/O	**GND**		56	I/O	-	
57	I/O	**LB_RESET#**		58	I/O	-	
59	I/O	**LB_WR#**		60	I/O	**Isolated GND**	Check Connection
61	I/O	-		62	I/O	-	
63	I/O	-		64	I/O	-	

Section9 PQ-MDS-T1 PLD TDM channels routing

PLD internal routing used to interface **PQ-MDS-T1** on board T1/E1or DS3 framers and LM card to **PQ-MDS-PIB** board Host TDM channels. This routing represented in the **Figure 14- Figure 18**

Note:

- Signals marked in "**Black**" are general
- Signals marked in "**Blue**" assigned for LM SLIC-SLAC card interconnections
- Signals marked in "**Red**" assigned to interface DS3/T3 framer

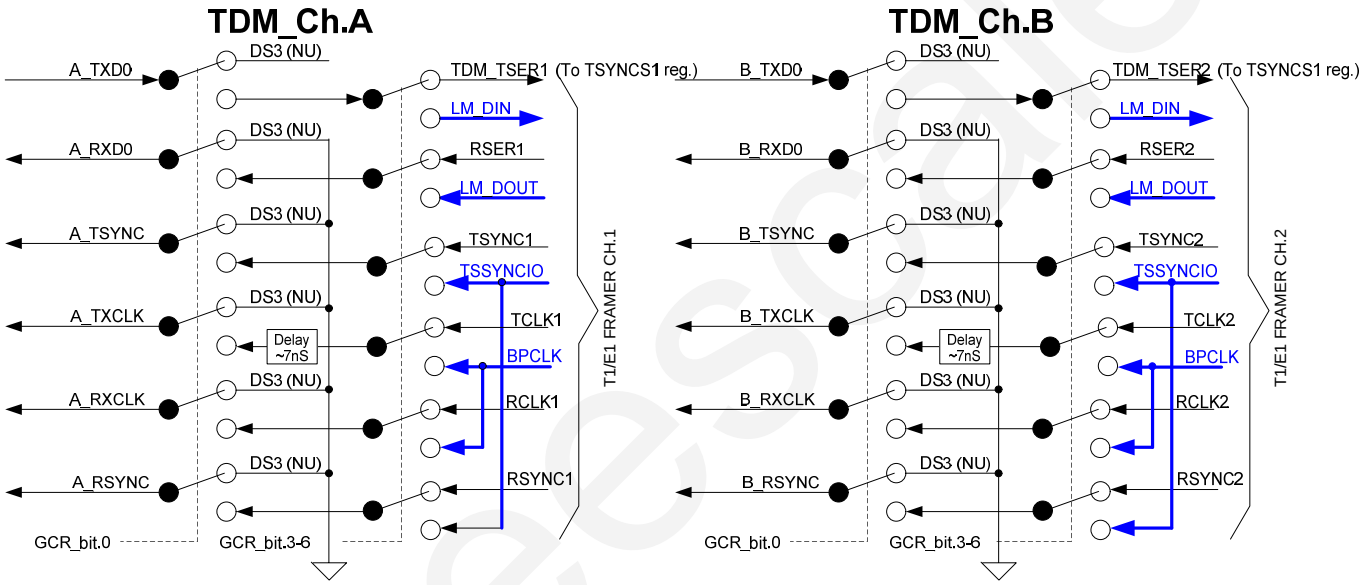

Figure 14

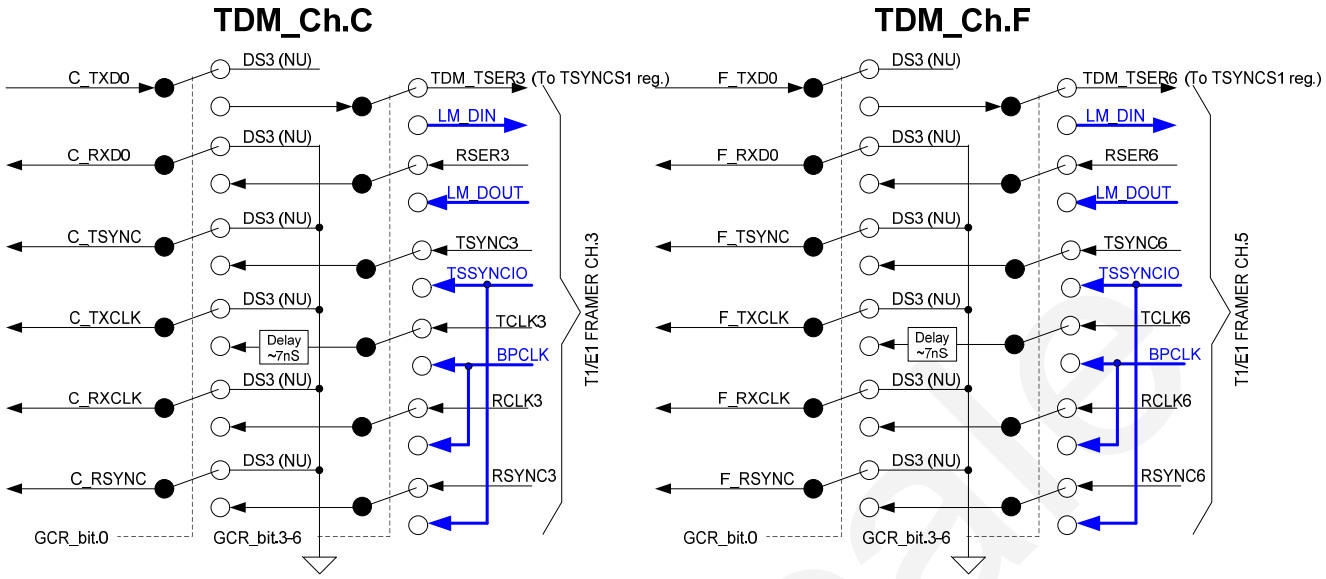

Figure 15

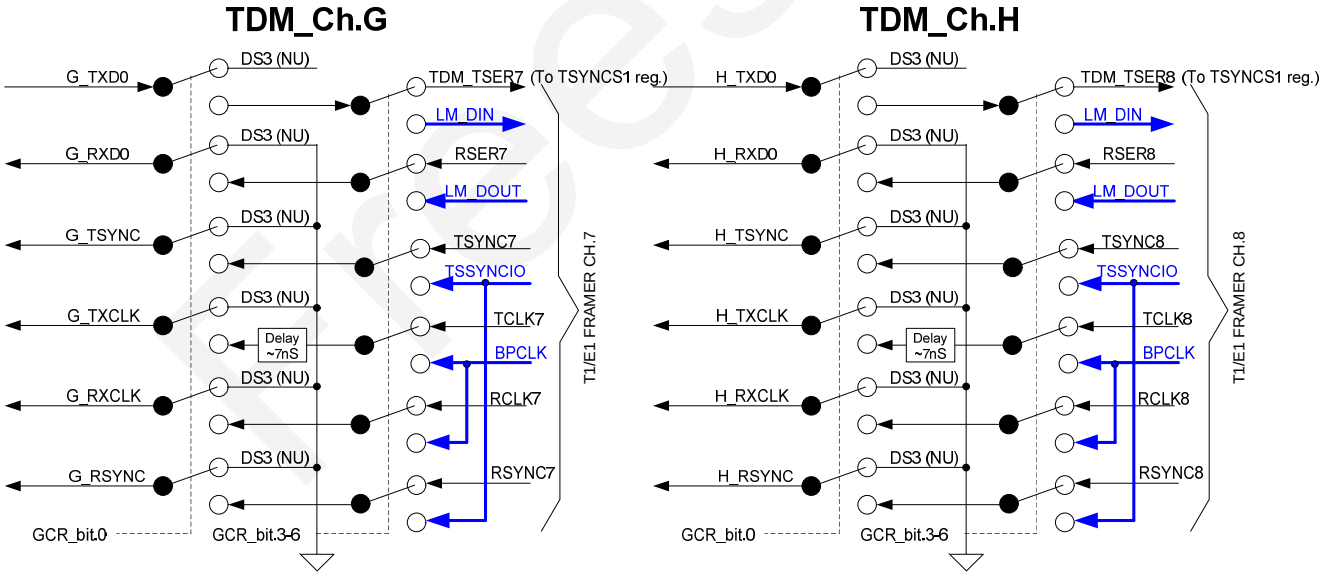

Figure 16

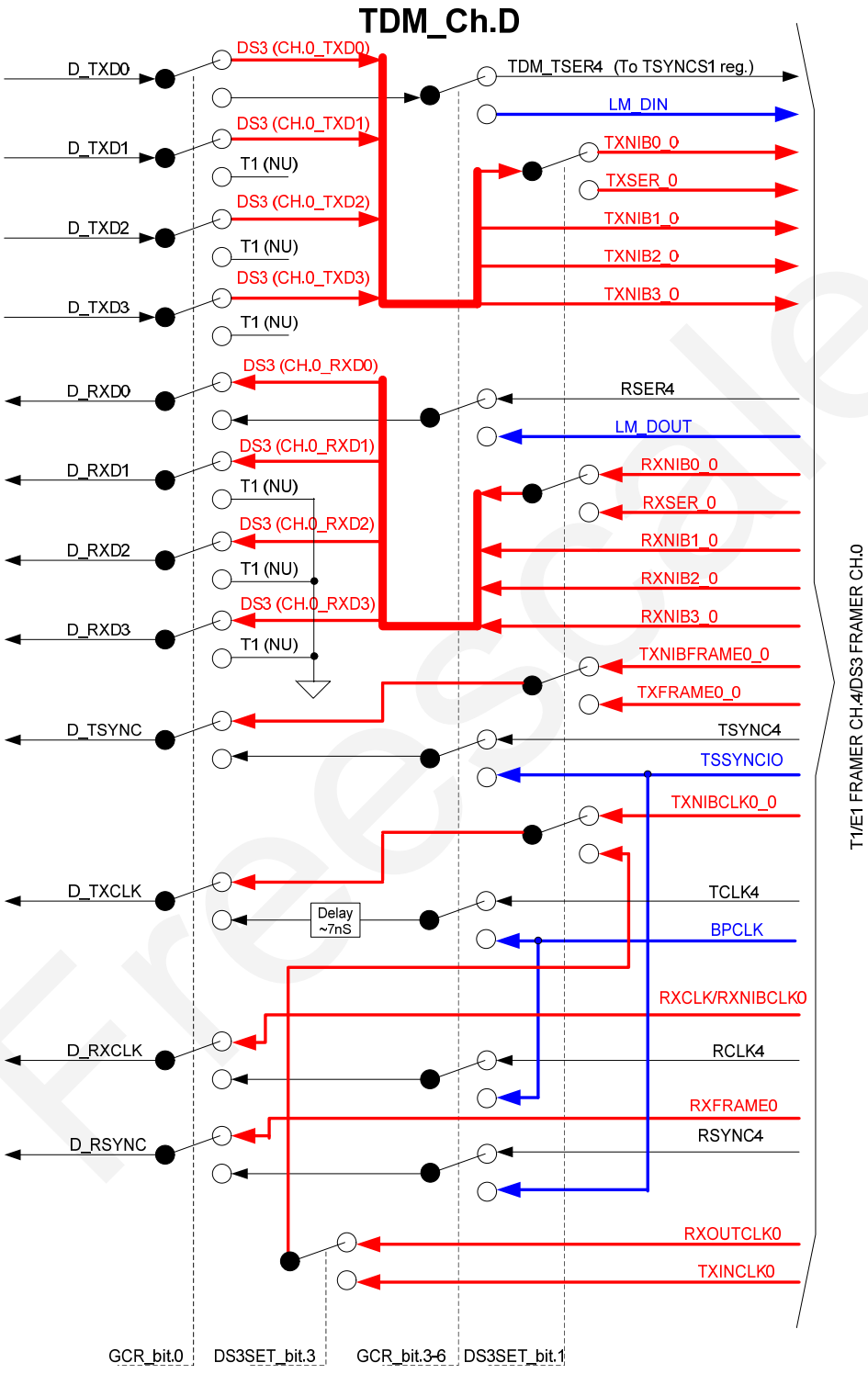
TDM_Ch.D
D_TXD0
D_TXD1
D_TXD2
D_TXD3
D_RXD0
D_RXD1
D_RXD2
D_RXD3
D_TSYNC
D_TXCLK
D_RXCLK
D_RSYNC
DS3 (CH.0_TXD0)
DS3 (CH.0_TXD1)
T1 (NU)
DS3 (CH.0_TXD2)
T1 (NU)
DS3 (CH.0_TXD3)
T1 (NU)
DS3 (CH.0_RXD0)
DS3 (CH.0_RXD1)
T1 (NU)
DS3 (CH.0_RXD2)
T1 (NU)
DS3 (CH.0_RXD3)
T1 (NU)
Delay ~7nS
TDM_TSER4 (To TSYNCS1 reg.)
LM_DIN
TXNIB0_0
TXSER_0
TXNIB1_0
TXNIB2_0
TXNIB3_0
RSER4
LM_DOUT
RXNIB0_0
RXSER_0
RXNIB1_0
RXNIB2_0
RXNIB3_0
TXNIBFRAME0_0
TXFRAME0_0
TSYNC4
TSSYNCIO
TXNIBCLK0_0
TCLK4
BPCLK
RXCLK/RXNIBCLK0
RCLK4
RXFRAME0
RSYNC4
RXOUTCLK0
TXINCLK0
T1/E1 FRAMER CH.4/DS3 FRAMER CH.0
GCR_bit.0
DS3SET_bit.3
GCR_bit.3-6
DS3SET_bit.1

Figure 17

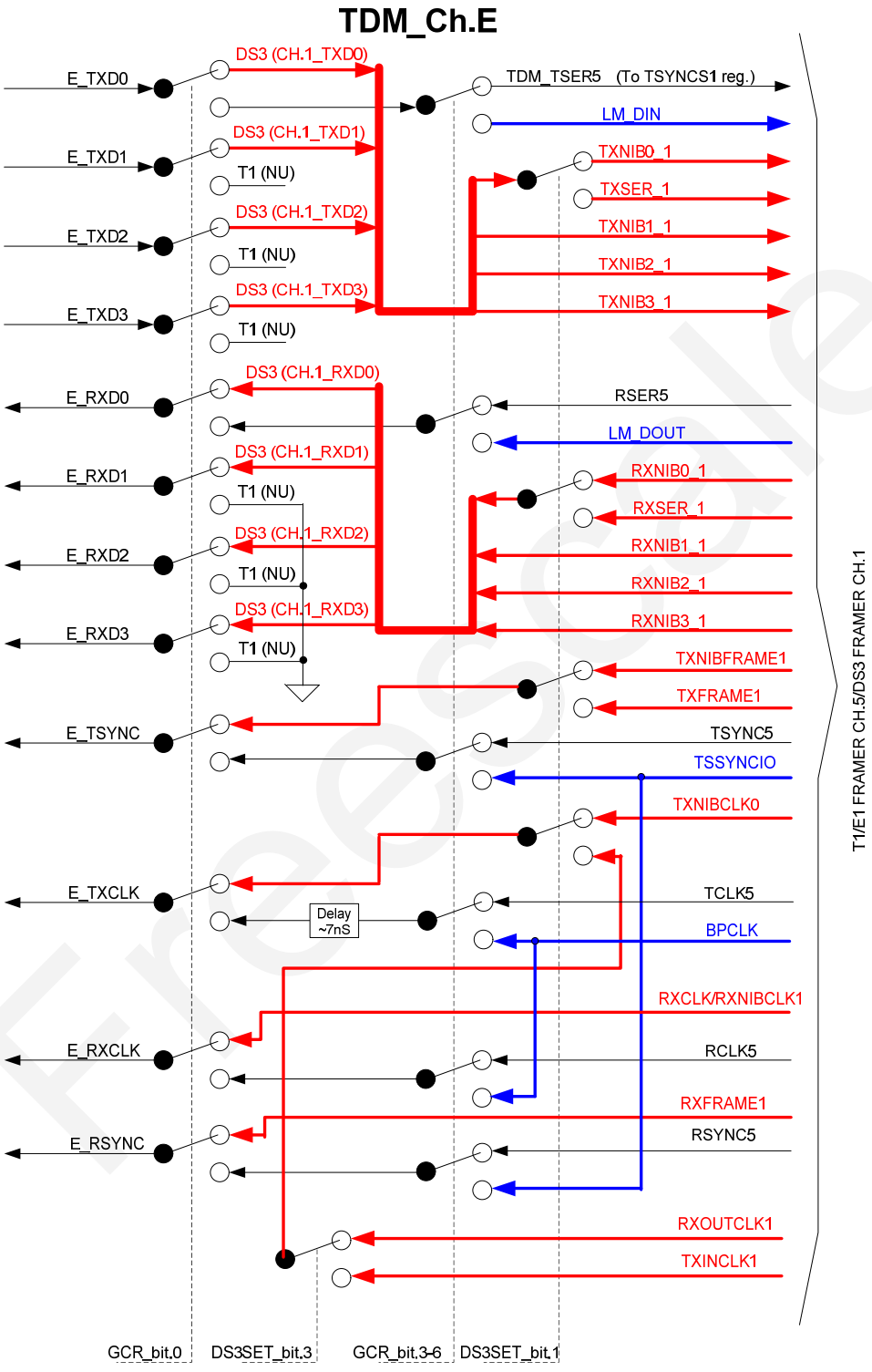
TDM_Ch.E
E_TXD0
E_TXD1
E_TXD2
E_TXD3
E_RXD0
E_RXD1
E_RXD2
E_RXD3
E_TSYNC
E_TXCLK
E_RXCLK
E_RSYNC
DS3 (CH.1_TXD0)
DS3 (CH.1_TXD1)
T1 (NU)
DS3 (CH.1_TXD2)
T1 (NU)
DS3 (CH.1_TXD3)
T1 (NU)
DS3 (CH.1_RXD0)
DS3 (CH.1_RXD1)
T1 (NU)
DS3 (CH.1_RXD2)
T1 (NU)
DS3 (CH.1_RXD3)
T1 (NU)
Delay ~7nS
TDM_TSER5 (To TSYNCS1 reg.)
LM_DIN
TXNIB0_1
TXSER_1
TXNIB1_1
TXNIB2_1
TXNIB3_1
RSER5
LM_DOUT
RXNIB0_1
RXSER_1
RXNIB1_1
RXNIB2_1
RXNIB3_1
TXNIBFRAME1
TXFRAME1
TSYNC5
TSSYNCIO
TXNIBCLK0
TCLK5
BPCLK
RXCLK/RXNIBCLK1
RCLK5
RXFRAME1
RSYNC5
RXOUTCLK1
TXINCLK1
T1/E1 FRAMER CH.5/DS3 FRAMER CH.1
GCR_bit.0
DS3SET_bit.3
GCR_bit.3-6
DS3SET_bit.1

Figure 18

Section10 PQ-MDS-T1 PLD control signals routing

PLD mapped control signal routing used to configure **PQ-MDS-T1** on board T1/E1or DS3/T3 framers and LM card to various operation modes. Internal interconnections control provided by corresponding control registers (see **3.3 PLD Control Register Description**). This routing represented in the **Figure 19- Figure 22**

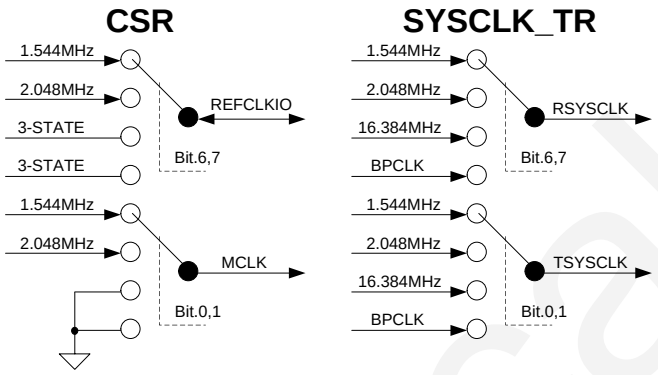

Figure 19

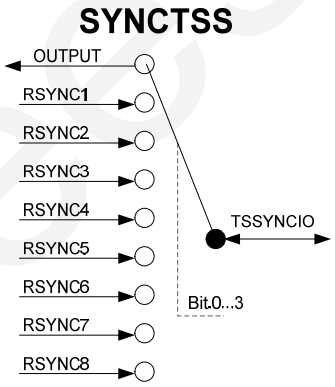

Figure 20

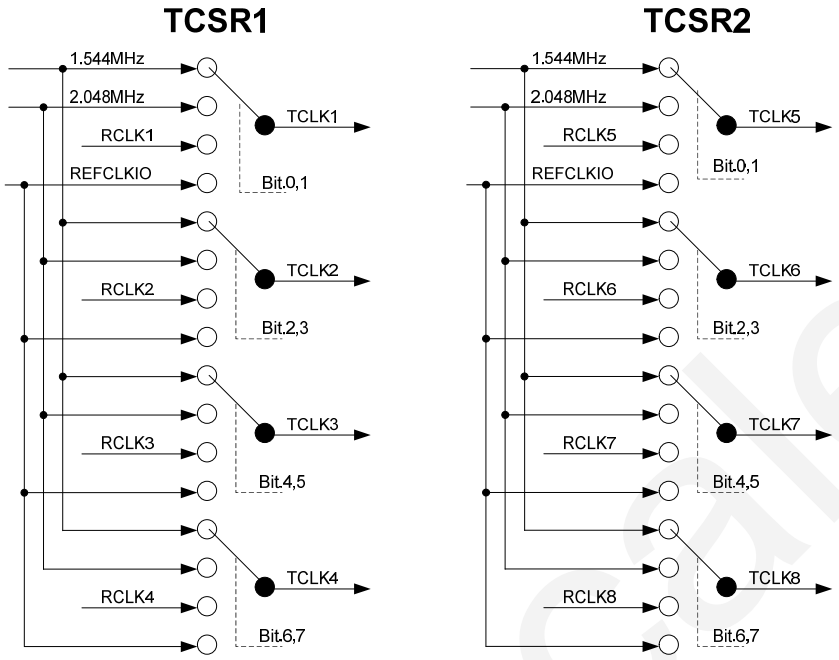

Figure 21

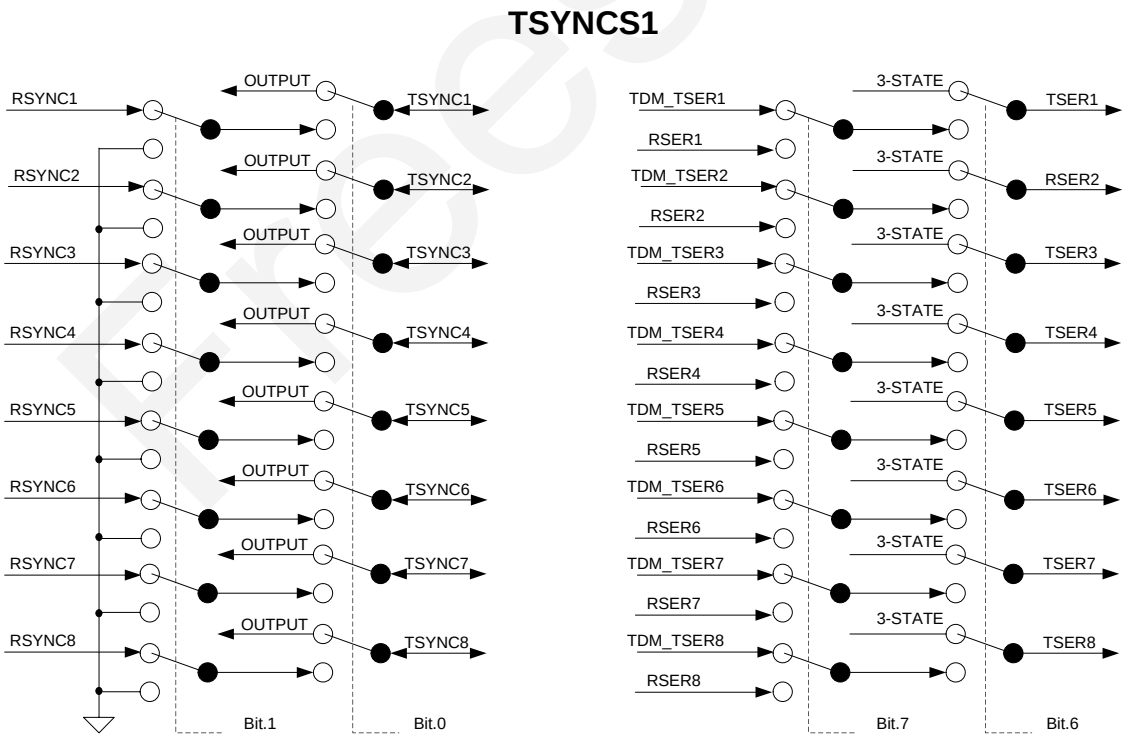

Figure 22

Board RESET signals generated by PLD mapped glue logic like shows in the **Figure 23** User has opportunity to RESET each framer/SLIC-SLAC module separately or provide general SW/HW RESET by control corresponding bits in the PLD mapped registers any time he need it.

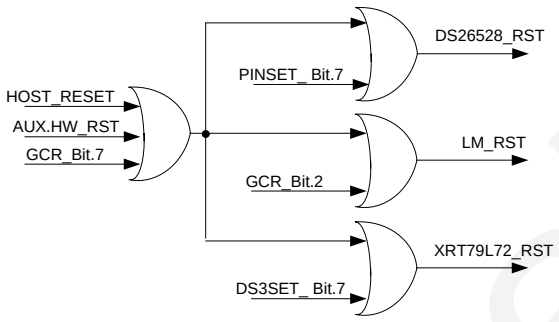

Figure 23

PLD internal divider like shows in the **Figure 24** used to provide 8.192MHz, 4.096MHz and 2.048MHz clock to corresponding parts. The source of the divider is external oscillator 16.384MHz.

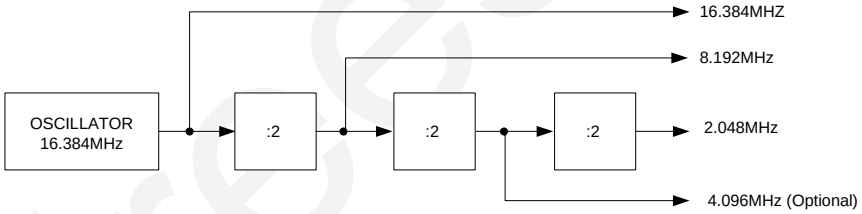

Figure 24