Technical Data

MPC561AEVBUM/D
Rev. 1, 12/2003

Dual MPC561/2/3/4
Autotemp Evaluation Board
User's Manual

1. Introduction

This document details how to use the dual MPC561/2/3/4 automotive temperature
specified EVB (hereafter referred to as the EVB). This product is designed to allow evaluation of the above parts within a temperature range of –40°C to +125°C in a dual controller application.

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2. EVB Features

This EVB provides the following features:

- ZIF type socket for MCU
- Single External Power supply regulated on board to provide the 5V, 3.3V and 2.6V supplies
- External SRAM devices in either Burst or Asynchronous configurations
- External Burst FLASH with option to protect a boot block
- Full reset configuration and mode selection switches
- Prototype area consisting of 0.1” pad grid and power/ground sections.
- NEXUS and BDM Debug connectors
- 6* Physical CAN interface drivers
- On board filtered supply and VRH / VRL ADC reference.
- Breakout connectors for all Microcontroller(MCU) signals
- Logic Analyser Connectors (MICTOR)
- 20 Mhz clock circuit

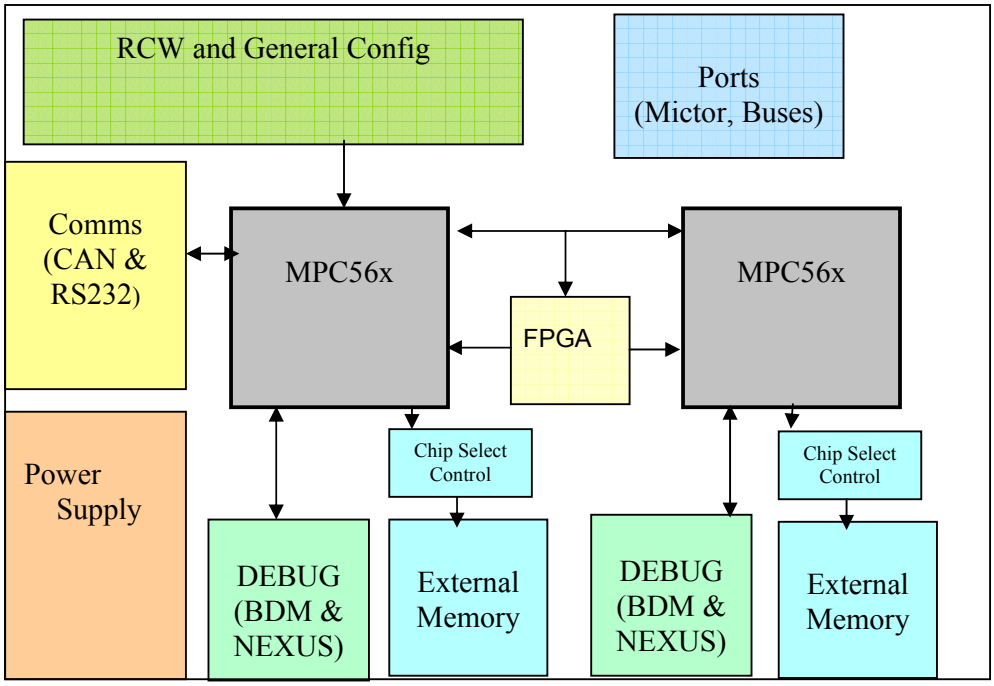


Figure 1 - EVB Functional Layout (not to scale)

Note – The size and location of each of the blocks shown in Figure 1 are not representative of the final PCB layout. This acts only as an indication as to the main functional blocks. The PCB layout can be seen in Appendix A

MCU Support

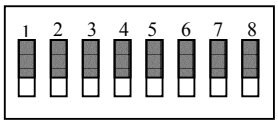
As mentioned above, the EVB will support MPC561, MPC562, MPC563 and MPC564 devices.

MCU Socket

In order to provide an easy mechanism for changing the MCU, a ZIF style socket is incorporated on the EVB.

Clock Circuitry

A 20 MHz crystal is used to supply the clock reference to the PLL circuitry, which is multiplied to the desired operating frequency. The MODCK settings of 0b001 and 0b011 can be used for the master and 0b100,0b101,0b111 for the slave as selected by SW1 and SW3 as shown below. This input is fed into the master device as detailed on the silkscreen. The clock reference to the slave device is fed from the CLKOUT pin of the master to the EXTCLK of the slave.



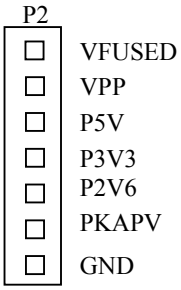
SW11 & SW3

1. MODCK1
2. MODCK2
3. MODCK3
4. RSTCONF
5. B0EPEE
6. EPEE
7. FLSH_VPP
8. FLSH_WP

EVB Power Supply

The EVB should be powered by a single external 12V power supply. This will be regulated on board to the required 5V, 3.3V and 2.6V supplies. Power is supplied to the EVB via a 2.1mm standard power jack and a single pole single throw switch SW1.

The EVB is designed to support 2 different regulator circuits as defined below. In order to easily select which regulator is used, the outputs of each regulator along with the 12V supply line are switched using SW2. SW2 selects between the MC33394(PowerOak) and a custom regulator. Jumpers J37-40, J7-10, P9 and P30 are provided on the EVB to allow direct connection to the EVB 5V, 3.3V and 2.6V power rails. LED's (DS 6-10) will indicate the status of each of the EVB power supply lines. Port P2 can be used to monitor the level of each supply.



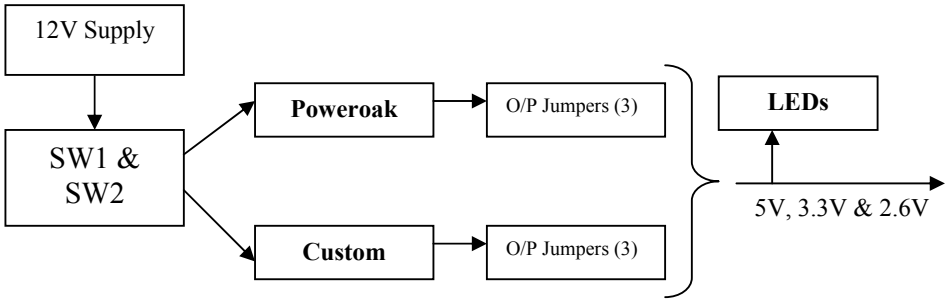


Figure 2 - Power Supply Selection

IRAMSTBY Supply / Keep Alive Power

Both the PowerOak and the custom regulator have the facility to provide a “keep alive” power supply. This allows the MCU to continue operating in a limited manner, using a much reduced power supply with the main 5V and 2.6V supplies turned off. In order for the MCU to continue operating, the CALRAM must be powered from an external source, typically the keep alive power (or the main vehicle battery).

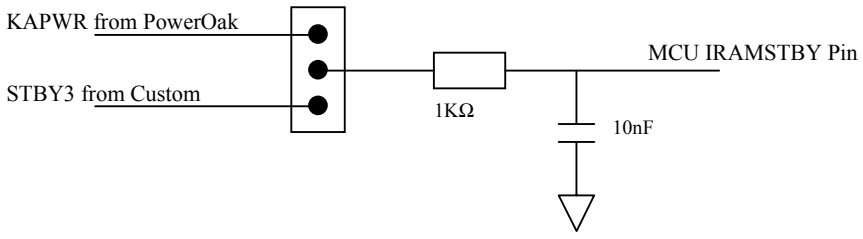


Figure 3 - IRAMSTBY Power Supply Filter and Selection

MC33394 (Power Oak)

The PowerOak integrated voltage regulator offers a high number of configuration possibilities.

CAN & SPI

Rather than defining a routing scheme for the PowerOak CAN module, a 4-way header (P5) provides access to the input and output signals. If it is required to use the CAN transceiver, wires can be routed from the desired MCU channel to the jumper block. Note that the ignition input (VIGN) is jumpered and for correct operation J2 has to be shorted. Similarly the SPI signals are connected to header P4.

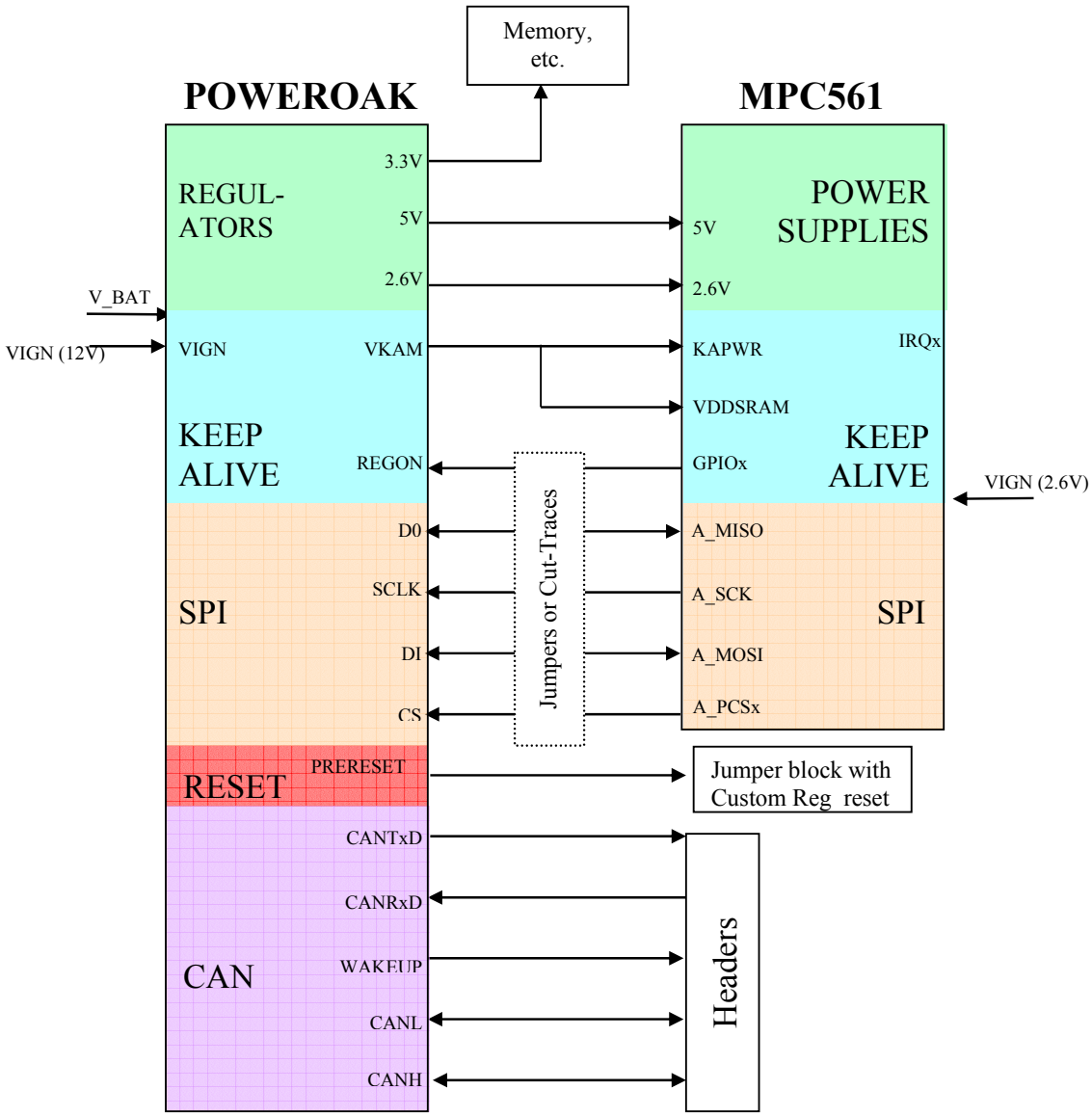


Figure 4 - PowerOak Integrated Regulator Solution

Note – As the Power Oak is designed as a companion for the MPC56x, no issues should occur with the MCU power sequencing requirements.

Custom Regulator

The initial EVB had the facility to accommodate a custom regulator however this device is no longer required as the PowerOak provides all the supplies. Note JP1-6 should be shorted for correct operation with the PowerOak.

External Bus Interface

Both MPC56x devices will communicate with one another and external memory over the External Bus Interface.

External Bus Interface Signals

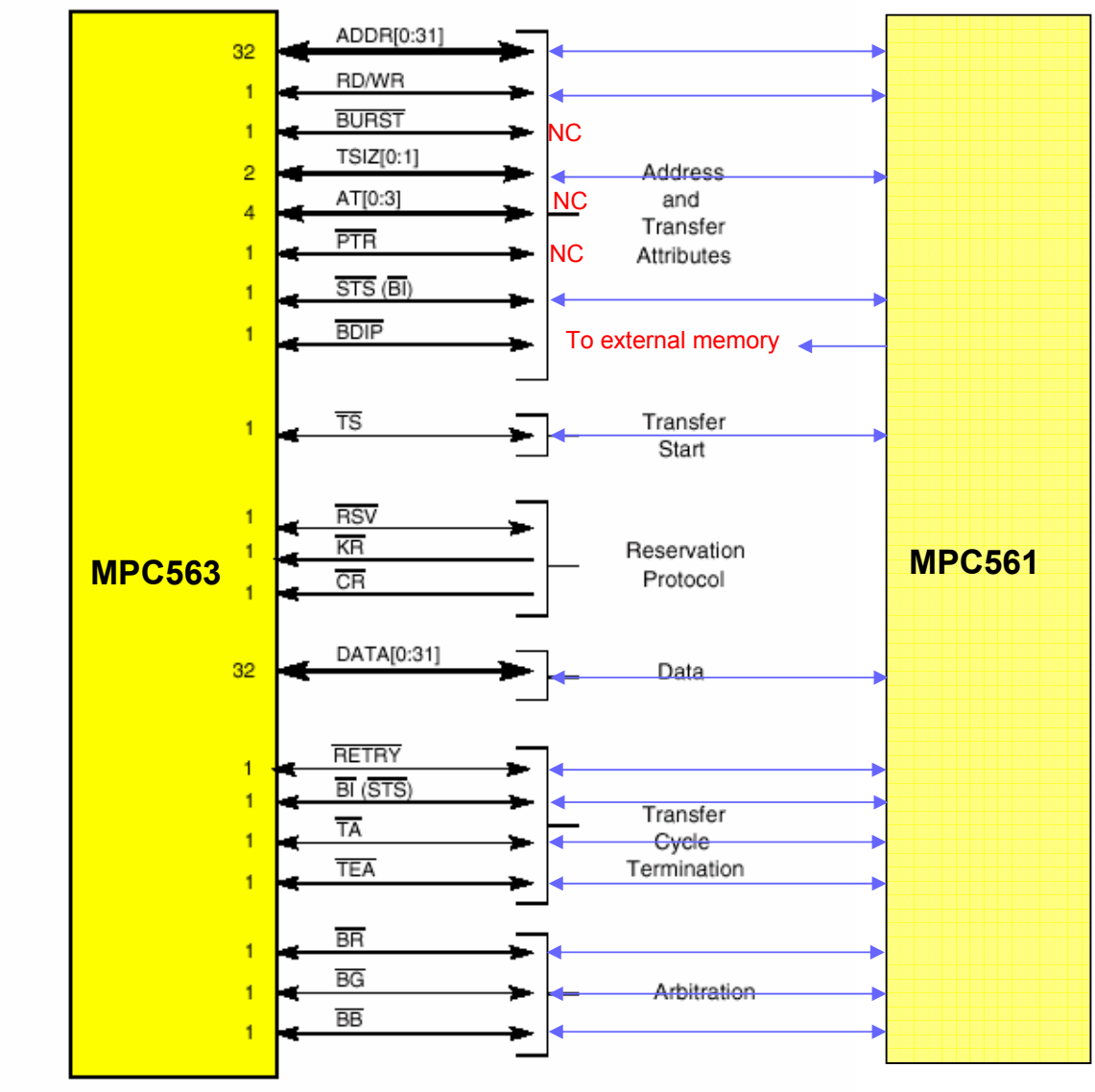


Figure 5 – EBI Signal Connections

NOTE
The BDIP signal is not required to be connected between the two MCUs as it is not possible for the external master to burst the internal memory of the slave. In the above figure the MPC563 is the master and the MPC561 is the slave. Similarly the BURST signal is not required on either inter-oak accesses or external memory accesses. #PTR is used by the debugging tool for program trace and is therefore not required for inter-oak communication.

External Memory – Overview

The following sections detail how external SRAM and FLASH are incorporated onto the EVB. There are 3 types of SRAM and 2 types of flash supported on the EVB. Due to the various voltages and thresholds of the different memories, the interconnection needs to be carefully selected.

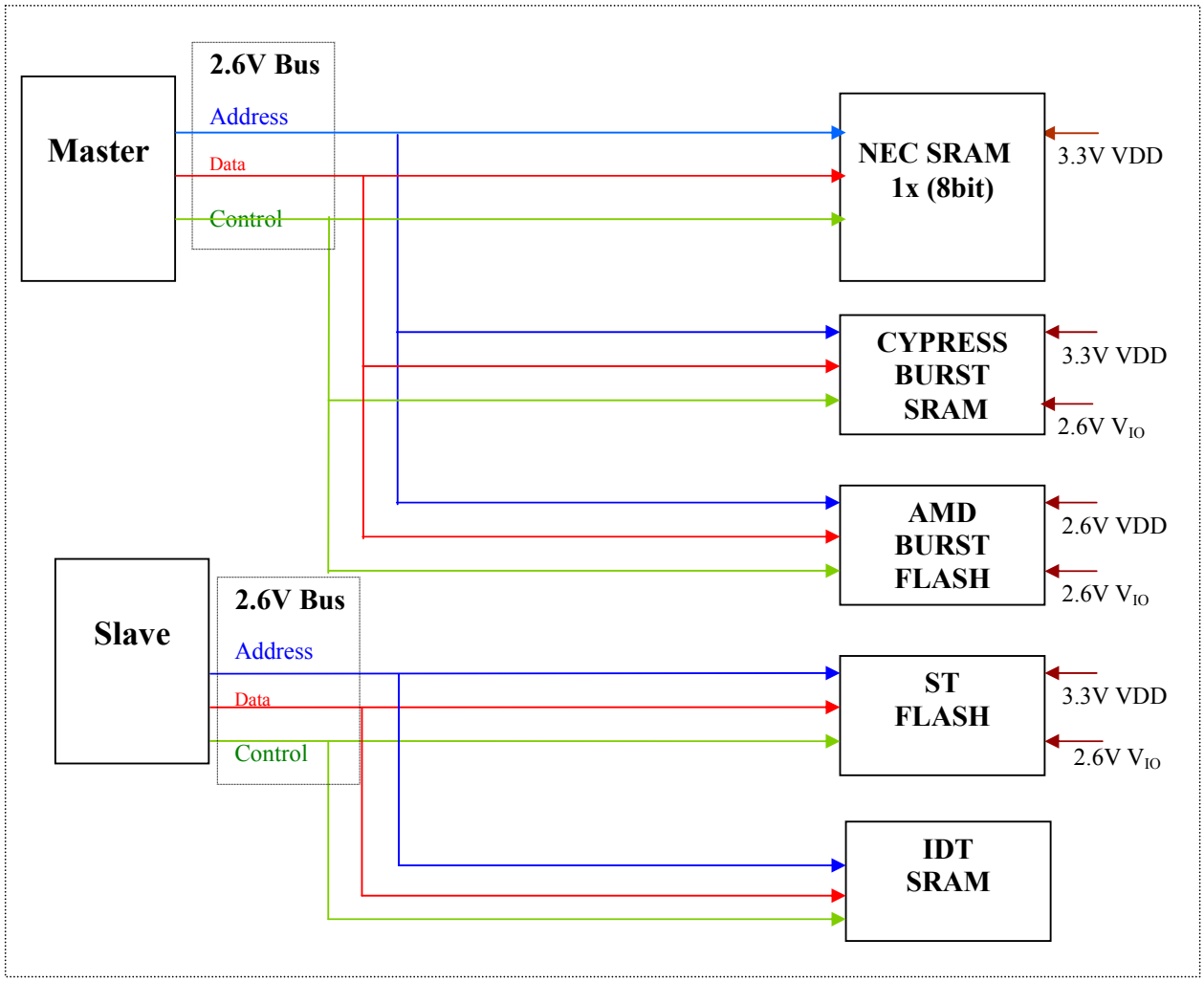
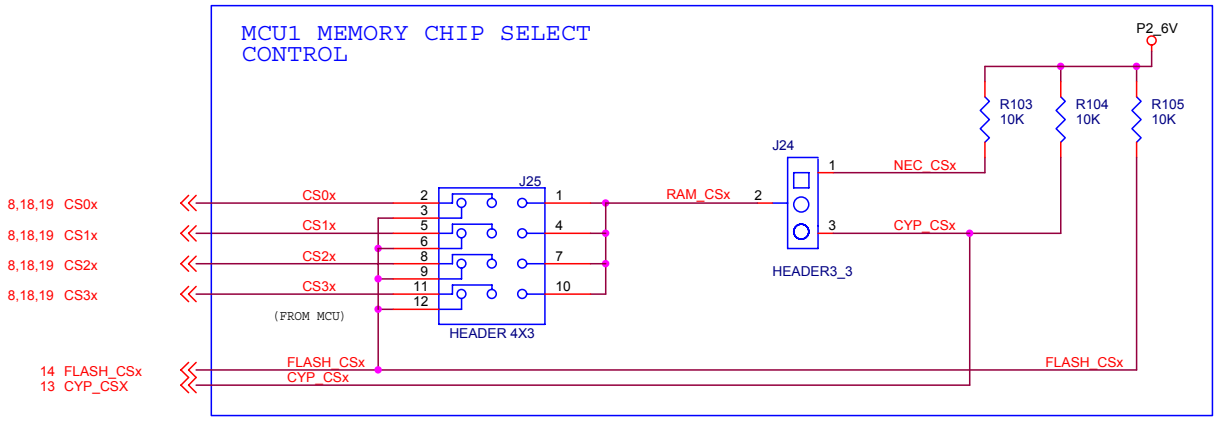


Figure 6 - Memory Hierarchy

As shown above in Figure 6 the master (MCU1) can read and write to the AMD29BDD160 burst flash EEPROM, the NEC uPD43256 and the CYPRESS CY7C1339 SRAMS. The slave MCU2 can read and write the ST M58BW016 burst flash EEPROM and the IDT IDT71T016 SRAM.

Master MCU1 Chip Select Connections



Jumper block J25 can be used to select which chip select (CS0 – CS3 from the master MCU) is used to select either the AMD flash EEPROM memory (U28 socketed) or SRAM. When used in conjunction with J24 either the NEC or CYPRESS device can be selected. The silkscreen on the board details how the connections are made. This can be seen in figures 7 and 8 below.

Each chip select signal is routed to pin 2 on each row of the jumper block. If the connection is made between pins 1 and 2 then the chip select is routed pin 2 of J24. If the connection is made between pins 2 and 3 then the chip select is routed to the AMD FLASH. On J24 if the connection is made between pins 1 and 2 then the NEC RAM is selected and similarly if the connection is made between pins 2 and 3 then the CYPRESS RAM is selected.

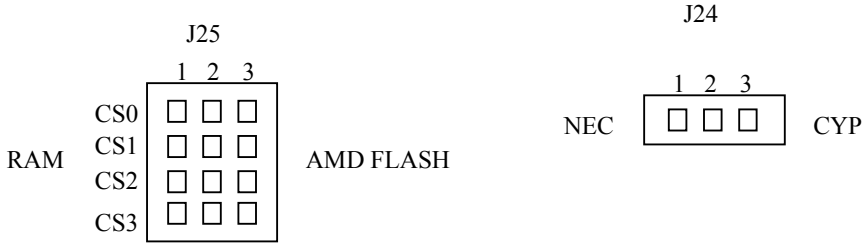


Figure 7

Slave MCU2 Chip Select Connections

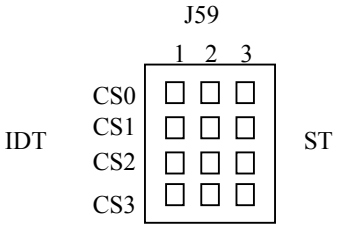


Figure 8

A similar scheme is implemented for the slave memory selection as detailed in Figure 8.

AMD Burst Flash Interface

This device is socketed on the EVB. The reason being that it can be inter-changed with the ST M58BW016. The pinouts of both devices are similar but not identical however both devices work correctly.

EVB Switch Configuration

Reset Configuration

This section details the possible configuration options latched at reset.

Reset Configuration Word (RCW):

Since the system has a common data bus, it is necessary to program RESET configuration in different ways for each device. One possibility is to program one chip with the external RESET configuration (RSTCONF=0) from the data bus, with the other taking the internal default RCW (RSTCONF=1 on an MPC561 and (RSTCONF=1 + HC = 1 on an MPC563)).

A third possibility is that every chip in the system will take the RESET configuration word from its internal flash (RSTCONF=1 + HC = 0 for all the chips). This way may be preferable, since there is no requirement to drive the external data bus by the RESET configuration word. This is only applicable if every device in the system has internal flash memory.

RSTCONF	Has Configuration (HC)	Internal Configuration Word
0	x	DATA[0:31] pins
1	0	NVM flash EEPROM register (UC3FCFIG)
1	1	Internal data word default (0x0000 0000)

Table 1- Reset Configuration Selection

NOTE
Switches 3 and 11, position 4 can be used to select whether the RSTCONF pin is pulled high or low.

To program the “shadow” RCW in the flash it is recommended that each device is programmed separately using the master socket on the board and the RCW from the external data bus to configure the device.

When both devices are programmed the system must be RESET once more in order for the new RCWs to take effect.

The following bits of a RCW are of great importance when configuring a multi-chip environment:

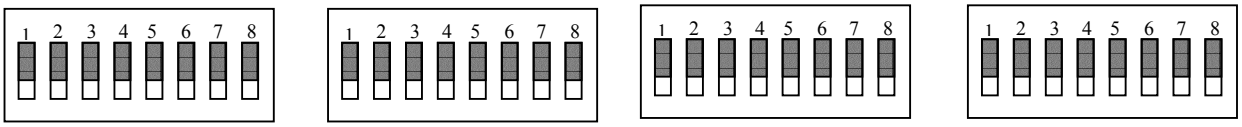
ISB [0:2] — This field determines the location of internal address space of a chip. It must be different for each chip. In an access to some internal address the **ISB[0]** is not considered, so there are only four different combinations possible. This limits the number of chips in the system. The only possible way to use more than four chips in the system (up to eight) is to configure four of them as masters that do not allow any other master to access

their internal locations. In any case, the maximum capacitance of each line should not exceed a value, stated in the electrical characteristics.

• **PRPM** — If this bit is set, the core of the chip is shut off and an alternative master on the external bus can access any internal slave module. This operation mode is called peripheral mode. At least one part in the system must have this bit cleared.

• **EARB** — If this bit is set then external arbitration on external bus is assumed. If there are only two chips in the environment, it is possible to use an internal arbiter of one of them. Then, **EARB** bits should be programmed as “1” and as “0” on each chip. If there are more than two chips in the system, the only choice is to use some other external arbiter. On the chip where **EARB** = “0”, there is a need to program an **EARP** field of SIUMCR as well. The **EARP** field determines the priority of external arbitration request.

D0……..D31



SW7 **SW8** **SW9** **SW10**

Switches 7,8,9,10 are used to set the external RCW on the data bus. SW7 position 1 selects D0 high or low with each subsequent switch selecting the polarity of its corresponding bit on the data bus up to SW10 position 8 selecting D31.

Each bit refers to the same bit in the RCW as defined below.

RCW— Reset Configuration Word

MSB

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EARB	IP	BDRV	BDIS	BPS[0:1]		Reserved			DBGC[0:1]		Re-served	ATWC	EBDF[0:1]		Re-served
Reset															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

LSB

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
PRPM	SC		ETRE	FLEN	EN COMP[1]	EXC COMP[1]	Re-served	OERC		RESERVED		ISB			DME
Reset															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTES:
1. Available only on the MPC563.

Bit(s)	Name	Description
0	EARB	External Arbitration — Refer to **9.5.7 Arbitration Phase** for a detailed description of Bus arbitration. The default value is that internal arbitration hardware is used. 0 = Internal arbitration is performed 1 = External arbitration is assumed
1	IP	Exception Prefix — This bit defines the initial value of the MSR[IP] bit immediately after reset. The setting of the MSR[IP] bit specifies the location of the exception vector table. 0 = MSR[IP] = 0 after reset, exception vector table starts at the physical address 0x0000 0000. 1 = MSR[IP] = 1 after reset, exception vector table starts at the physical address 0xFFF0 0000.
2	BDRV	Bus Pins Drive Strength — This bit determines the bus pins (address, data and control) drive capability to be either full or reduced drive. The bus default drive strength is full. Upon default, it also affects the CLKOUT drive strength to be full. BDRV controls the default state of COM[1] in the SIUMCR. See Table 8-9 for more information. 0 = Full drive 1 = Reduced drive
3	BDIS	Boot Disable — If the BDIS bit is set, the memory controller is not activated after reset. If it is cleared then the memory controller bank 0 is active immediately after reset such that it matches any addresses. If a write to the OR0 register occurs after reset this bit definition is ignored. The default value is that the memory controller is enabled to control the boot with the $\overline{CS}$[0] pin. See **10.7 Global (Boot) Chip-Select Operation** for more information. 0 = Memory controller bank 0 is active and matches all addresses immediately after reset 1 = Memory controller is not activated after reset.
4:5	BPS	Boot Port Size — This field defines the port size of the boot device on reset (BR0[PS]). If a write to the OR0 register occurs after reset this field definition is ignored. See**Table 10-5** and **Table 10-8** for more information. 00 = 32-bit port (default) 01 = 8-bit port 10 = 16-bit port 11 = Reserved
6:8	—	Reserved. These bits must not be high in the reset configuration word.

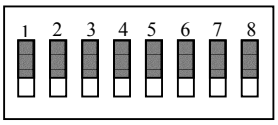
Bit(s)	Name	Description
9:10	DBGC[0:1]	Debug Pins Configuration — See 6.14.1.1 SIU Module Configuration Register (SIUMCR) for this field definition. The default value is that these pins function as: VFLS[0:1], $\overline{BI}$, $\overline{BR}$, $\overline{BG}$ and $\overline{BB}$. See Table 6-8.
11	—	Reserved.
12	ATWC	Address Type Write Enable Configuration — This bit controls the initial value of SIUMCR[ATWC], that configures the pins to function as byte write enables or address types for debugging purposes. The default value is that these pins function as $\overline{WE}$ pins. See Table 6-7. 0 = $\overline{WE}$[0:3]/$\overline{BE}$[0:3]/AT[0:3] functions as $\overline{WE}$[0:3]/$\overline{BE}$[0:3] 1 = $\overline{WE}$[0:3]/$\overline{BE}$[0:3]/AT[0:3] functions as AT[0:3]
13:14	EBDF	External Bus Division Factor — This field controls the initial value of SCCR[EBDF] that defines the initial value of the external bus frequency. The default value is that CLKOUT frequency is equal to that of the internal clock (no division). See Table 8-9.
15	—	Reserved. This bit must not be high in the reset configuration word.
16	PRPM	Peripheral Mode Enable — This bit controls the initial value of EMCR[PRPM], that determines if the device is in peripheral mode. See Table 6-13. Default is peripheral mode not enabled. 0 =Normal operation 1 = Peripheral mode operation
17:18	SC	Single Chip Select — This field determines the initial value of SIUMCR[SC], that configures the functionality of the address and data buses. See Table 6-7 and Table 6-10 for more information. 00 = Extended chip, 32 bits data 01 = Extended chip, 16 bits data 10 = Single chip and show cycles (address) 11 = Single chip
19	ETRE	Exception Table Relocation Enable — This bit determines the initial value of BBCMCR[ETRE], that defines whether the exeption table relocation feature is enabled or disabled. See Table 4-4. 0 = Exception table relocation is off 1 = Exception table relocation is on
20	FLEN	Flash Enable — This bit controls the value of IMMR[FLEN], that determines whether the on-chip flash memory is enabled or disabled out of reset . The default state is disabled, which means that by default, the boot is from external memory. Refer to Table 6-12 for more details. 0 = Flash disabled — boot is from external memory 1 = Flash enabled
21	EN_ COMP[1]	Enable Compression — This bit determines the initial value of BBCMCR[EN_COMP] on devices with code compression enabled. The default state is disabled. See Table 4-4 for more information.
22	EXC_ COMP[1]	Exception Compression — This bit determines the initial value of BBCMCR[EXC_COMP] on devices with code compression enabled. See Table 4-4 for more information.
23	—	Reserved. This bit must not be high in the reset configuration word.
24:25	OERC	Other Exceptions Relocation Control — This field determines the initial value of BBCMCR[OERC]. They only have an effect if BBCMCR[ETRE] is set. See 4.5.2 ETR Operation. Relocation offset: 00 = Offset 0 01 = Offset 64 Kbytes 10 = Offset 512 Kbytes 11 = Offset to 0x3F E000
26:27	—	Reserved

Bit(s)	Name	Description
28:30	ISB	Internal Space Base Select — This field defines the initial value of the ISB field in the IMMR register. A detailed description is in Table 6-12. The default state is that the internal memory map is mapped to start at address 0x0000 0000. This bit must not be high in the reset configuration word.
31	DME	Dual Mapping Enable — This bit controls the DMBR[DME] in the memory controller, that determines whether dual mapping of the internal flash is enabled. For a detailed description refer to Table 10-11. The default state is that dual mapping is disabled. 0 = Dual mapping disabled 1 = Dual mapping enabled

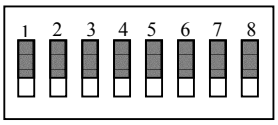
NOTES:
1. Available only on the MPC563.

Clock Circuitry

A 20 MHz crystal is used to supply the clock reference to the PLL circuitry of the master device, which is multiplied to the desired operating frequency. The MODCK settings can be selected by SW1 and SW3 as shown below. The clock reference to the slave device is fed from the CLKOUT pin of the master device to the EXTCLK of the slave device.



SW3



SW11

1. MODCK1
2. MODCK2
3. MODCK3
4. RSTCONF
5. B0EPEE
6. EPEE
7. FLSH_VPP
8. FLSH_WP

The MODCLK[1-3] pins are driven via buffers when PORESET is low.

MODCK[1:3][1]	LME	Default Values after PORESET			SPLL Options
		MF + 1	PITCLK Division	TMBCLK Division	
000	0	1	4	4	Used for testing purposes.
001	0	1	256	16	Normal operation, PLL enabled. Main timing reference is crystal osc (20 MHz). Limp mode disabled.
010	1	5	256	4	Normal operation, PLL enabled. Main timing reference is crystal osc (4 MHz). Limp mode enabled.
011	1	1	256	16	Normal operation, PLL enabled. Main timing reference is crystal osc (20 MHz). Limp mode enabled.
100 101	0	1	256	16	Normal operation, PLL enabled. 1:1 Mode Main timing reference is EXTCLK pin (>15MHz) Limp mode disabled.
110	0	5	256	4	Normal operation, PLL enabled. Main timing reference is EXTCLK (3-5 MHz). Limp mode disabled.
111	1	1	256	16	Normal operation, PLL enabled. 1:1 Mode Main timing reference is EXTCLK pin (>15MHz) Limp mode enabled.

Table 2- MODCK Settings

Other Control Switches

Internal Flash Protect

The MPC563 has 2 input pins that are used to control the internal flash program / erase protection. These are controlled using SW3 and SW11 position 5 and 6.

EPEE (Complete Flash Protect) position 6.
B0EPEE (Block 0 Protection) position 5.

For both these pins, a logic 1 (2.6V) allows erasure / program of the flash. A logic 0 means the flash is protected.

External Flash Protect

SW3 position 8 controls the write protect for the AMD flash and similarly SW11 position 8 controls the ST flash write protect. When these switches are in the OFF position the flashes are write protected. Similarly position 7 on both switches controls the ACC(AMD) pin and VPP(ST) respectively.

For the AMD flash it makes no difference whether this switch is in the on or off position as the voltage will only be switched between 0-2.6V. The voltage on this pin needs to be 12V for the program acceleration to take place. However if the switch for the ST device is in the OFF position then the full array is write protected. Again as this pin can not be connected to 12V the programming cannot be accelerated.

MCU Reset Control

The MPC563 has 3 dedicated reset pins as detailed below:

PORESET* - Power on reset (input only pin). Used mainly for low voltage reset (LVI). Rising edge latches all reset configuration data. Asserting PORESET* causes the MCU to drive HRESET* and SRESET* lines.

HRESET* - Hard Reset (bi-directional pin). Can be asserted by the MCU or an external source. If the MCU detects the HRESET* pin going low, it drives HRESET* and SRESET* lines low.

SRESET* - Soft Reset (bi-directional pin). As with HRESET*, the SRESET* line can be asserted by the MCU or by an external source. If the MCU detects the SRESET* line going low, it then drives SRESET* low.

Pushbutton reset switches SW4,5,6 for the master device and SW12,13,14 for the slave device are connected to each of these MCU reset pins (PORESET* via the LVI, see below). In addition, an LED is connected to the MCU SRESET* line to indicate every reset condition. External pullup resistors will hold the MCU reset lines at 2.6V when not in a reset condition.

CLKOUT & Reset Considerations

If the slave device is clocked from the master device using the CLKOUT signal then there is an issue. When the system frequency is changed from the default (determined by the crystal used and MODCK settings) by increasing the multiplication factor PLPRCR [MF] the PLL temporarily loses lock and the CLKOUT is lost hence losing communication with the slave device.

To overcome this the following solution was employed:-

Using an I/O pin from the master device hold the slave device in reset until the PLL locks at the required system frequency on the master. It is then safe to release reset on the slave device without losing communication between the two devices.

In order to provide protection against low voltage power interruption the reset circuitry provided by the PowerOak and custom regulators are used on the EVB to hold the MCU in reset if VDD drops below 2.5V. The resets from these regulators are switched to the master using SW2. Only one regulator can be selected at any given time therefore only one source of PORESET is available.

As the PowerOak and custom devices have the facility to use keep-alive power, the LVI circuit must take into account the fact that when in low power mode, the 2.6V and 5V supplies are removed.

PowerOak cannot turn off KAPWR therefore the TEXP functionality can only be tested with the custom regulator. However PowerOak does have the SLEEP pin to turn off the 5V, 3.3V and 2.6V supplies which can be controlled via an MPC56x I/O pin.

Debug Interface

The MPC56x supports both standard BDM and Nexus Class-3 debug interfaces. Both interface connectors will be fitted to the EVB. Care should be taken that these connectors are located in an easily accessible area, close to the MCU socket.

Each connector will have pin1 clearly labeled. If board space allows, keyed connectors may be fitted.

Standard BDM Interface

The diagram below details the standard BDM connector pinout:

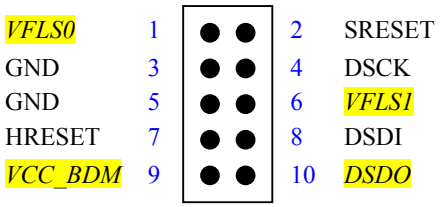
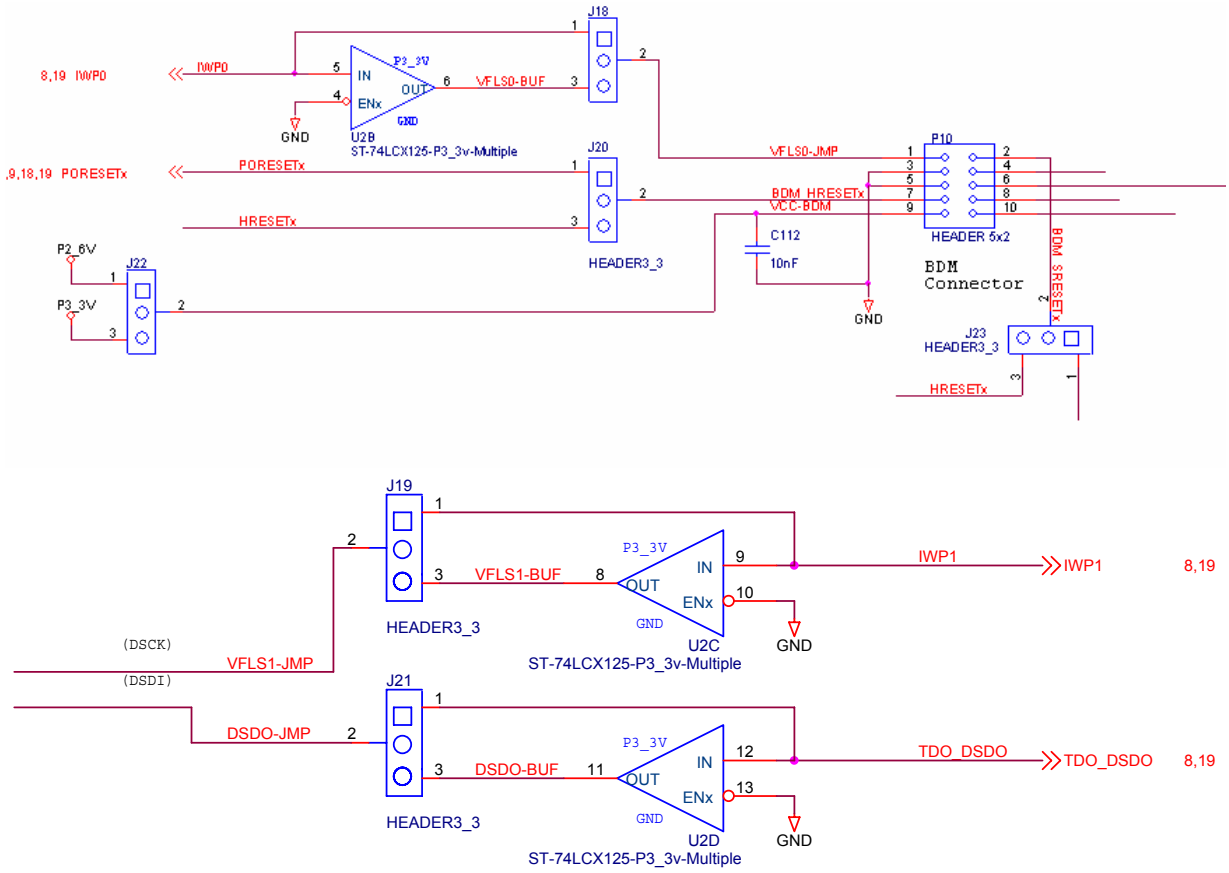


Figure 7- BDM Connector Pinout

In order to support some of the older BDM interface cables which work on 3.3V signal levels, the VFLS0, VCC_BDM, VFLS1 and DSDO signals have the option of being increased from 2.6V to 3.3V using a buffer as shown:



DEVICE	JUMPER NUMBER	PINS SHORTED	FUNCTIONALITY
Master	J18	1&2 2&3	VFLS0 Buffered VFLS0
Master	J19	1&2 2&3	VFLS1 Buffered VFLS1
Master	J20	1&2 2&3	PORESET HRESET
Master	J21	1&2 2&3	DSDO Buffered DSDO
Master	J22	1&2 2&3	2.6V 3.3V
Master	J23	1&2 2&3	SRESET HRESET
Slave	J45	1&2 2&3	HRESET SRESET
Slave	J46	1&2 2&3	VFLS0 Buffered VFLS0
Slave	J47	1&2 2&3	VFLS1 Buffered VFLS1
Slave	J48	1&2 2&3	PORESET HRESET
Slave	J49	1&2 2&3	DSDO Buffered DSDO
Slave	J50	1&2 2&3	2.6V 3.3V

Note – No signal translation is required for the MCU Input signals such as DSDI and DSCK.

Nexus Interface Connector

In addition to the BDM connectors (P10 (Master) & P31 (Slave)), the 50 Pin NEXUS connectors (P11 (Master) & P32 (Slave)) are fitted to the EVB (see pinout below).

Table 2 MPC56x Nexus 50 Pin Definition (Full Port Mode)

MPC56x Signal	Nexus Auxiliary Signal		Pin	Pin		Nexus Auxiliary Signal	MPC56x Signal
-	UBATT	OUT	1	2	OUT	UBATT	-
VSTBY2.6	VSTBY	OUT	3	4	IN or OUT	TOOL_IO0	-
-	TOOL_IO1	IN or OUT	5	6	IN or OUT	TOOL_IO2	-
$\overline{\text{HRESET}}$	/RESET	IN[1]	7	8	OUT	VREF	VDD2.6
$\overline{\text{EVTI}}$	/EVTI	IN[1]	9	10	-	GND	GND
$\overline{\text{RSTI}}$	/RSTI	IN[2]	11	12		GND	GND
$\overline{\text{MSEI}}$	/MSEI	IN[1]	13	14	-	GND	GND
MDI[0]	MDI0	IN[1]	15	16	-	GND	GND
MCKI	MCKI	IN[1]	17	18	-	GND	GND
MDO[0]	MDO0	OUT	19	20	-	GND	GND
MCKO	MCKO	OUT	21	22		GND	GND
LWP[1]	/EVTO	OUT	23	24	-	GND	GND
$\overline{\text{MSEO}}$	/MSEO0	OUT	25	26	IN or OUT	VENDOR_IO0	LWP[0]
MDO[1]	MDO1	OUT	27	28	-	GND	GND
MDO[2]	MDO2	OUT	29	30	-	GND	GND
MDO[3]	MDO3	OUT	31	32	-	GND	GND
MDI[1]	MDI1	IN[1]	33	34	-	GND	GND
-	/MSEO1	OUT	35	36	-	GND	GND
MDO[4]	MDO4	OUT	37	38	-	GND	GND
MDO[5]	MDO5	OUT	39	40	-	GND	GND
MDO[6]	MDO6	OUT	41	42	-	GND	GND
MDO[7]	MDO7	OUT	43	44	-	GND	GND
-	MDI2	IN[1]	45	46	-	GND	GND
-	MDI3	IN[1]	47	48		GND	GND
EPEE & B0EPEE	VENDOR_IO1	IN or OUT	49	50		GND	GND

NOTES:
1. The Nexus standard recommends that inputs should have 10K ? pull-up resistors to VREF.
2. The Nexus standard recommends that inputs should have 10K ? pull-up resistors to VREF. This is being changed in the new revision of the standard to state that $\overline{\text{RSTI}}$ should be pulled down. The $\overline{\text{RSTI}}$ input however requires a pull-up value of less than 6.1K ? . This is in line with the proposed new standard.

Please take this table from Randy's apps note.

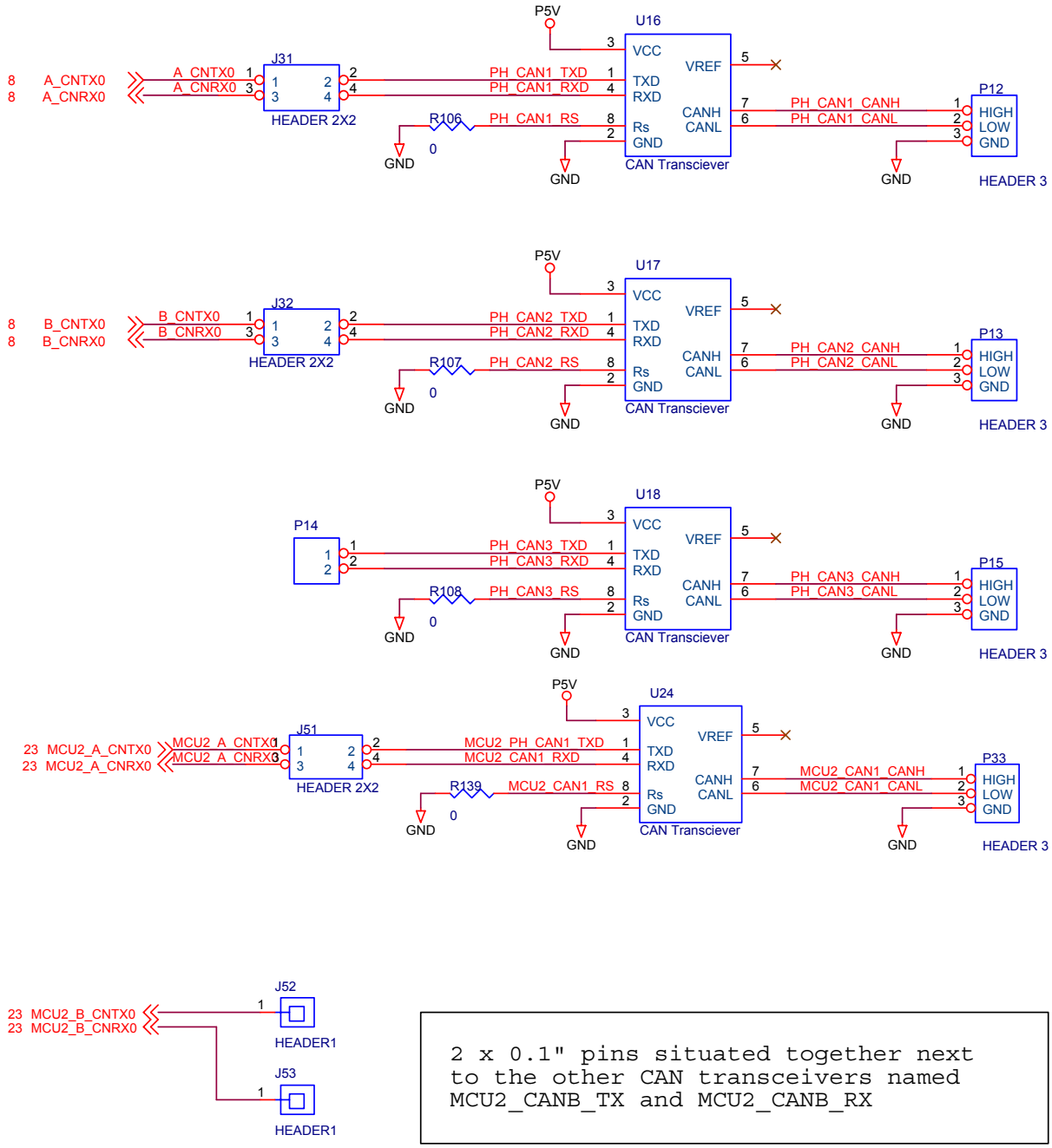
Table 3 – 50 pin Nexus Connections

CAN Interface

Four Philips PCA82C250 physical CAN interface drivers are fitted to the EVB (U16,17,18,24). Jumpers J31,32 and 51 can be used to isolate each MCU CAN signal from the physical driver if required.

The CAN bus (CANH and CANL) is brought out to headers P12,13 and 15 at the edge of the board.

Note that the PowerOak and custom regulator CAN transceivers are available in addition to the 4 Philips drivers.



2 x 0.1" pins situated together next to the other CAN transceivers named MCU2_CANB_TX and MCU2_CANB_RX

From above it can be seen that

DEVICE	JUMPER NUMBER	PINS SHORTED	FUNCTIONALITY
Master	J31	1&2 2&3	CANA_TX CANA_RX
Master	J32	1&2 2&3	CANB_TX CANB_RX
Master	P14		Header to allow CANC TX and RX connection. PIN1=TX PIN2= RX
Slave	J51	1&2 2&3	CANA_TX CANA_RX
Slave	J52	1	CANB_TX
Slave	J53	1	CANA_RX

J52 and J53 can be used to connect to J51 pins 2 and 4 respectively to allow slave CAN B to be used.

SCI Interface
Master SCI1(queued) and slave SCI2(no queue) are routed via a transceiver to two 9-way D Type female connectors P16 and P17 respectively.

A Maxim MAX232 transceiver is used on this board

ADC Support
All of the QADCE pins are available on a dedicated header block P19(master) and P35(slave).

Connectors
This section defines the pinout for each of the breakout connectors that are fitted to the EVB.

All connectors are 0.1” pitch standard through-hole, with the exception of the Logic Analyser connectors which are MICTOR style.

TPU

Pin No	Function	Pin No.	Function
1	A_TPUCH0	2	A_TPUCH1
3	A_TPUCH2	4	A_TPUCH3
5	A_TPUCH4	6	A_TPUCH5
7	A_TPUCH6	8	A_TPUCH7
9	A_TPUCH8	10	A_TPUCH9
11	A_TPUCH10	12	A_TPUCH11
13	A_TPUCH12	14	A_TPUCH13
15	A_TPUCH14	16	A_TPUCH15
17	AT2CLK	18	GND
19	B_TPUCH0	20	B_TPUCH1
21	B_TPUCH2	22	B_TPUCH3
23	B_TPUCH4	24	B_TPUCH5
25	B_TPUCH6	26	B_TPUCH7
27	B_TPUCH8	28	B_TPUCH9
29	B_TPUCH10	30	B_TPUCH11
31	B_TPUCH12	32	B_TPUCH13
33	B_TPUCH14	34	B_TPUCH15
35	BT2CLK	36	GND

Table 4- TPU Connector Pinout

QADC

Pin No	Function	Pin No.	Function
1	A_PQA0	2	A_PQB0
3	A_PQA1	4	A_PQB1
5	A_PQA2	6	A_PQB2
7	A_PQA3	8	A_PQB3
9	A_PQA4	10	A_PQB4
11	A_PQA5	12	A_PQB5
13	A_PQA6	14	A_PQB6
15	A_PQA7	16	A_PQB7
17	B_PQA0	18	B_PQB0
19	B_PQA1	20	B_PQB1
21	B_PQA2	22	B_PQB2
23	B_PQA3	24	B_PQB3
25	B_PQA4	26	B_PQB4
27	B_PQA5	28	B_PQB5
29	B_PQA6	30	B_PQB6
31	B_PQA7	32	B_PQB7
33	ETRIG1	34	ETRIG2
35	VRH	36	VRL
37	ALTREF	38	GND

Table 5- QADC Connector Pinout

QSMCM

Pin No	Function	Pin No.	Function
1	QGPIO[0] / (A_PCS0)	2	QGPIO[1] / (A_PCS1)
3	QGPIO[2] / (A_PCS2)	4	QGPIO[3] / (A_PCS3)
5	QGPIO[4] / (MISO)	6	QGPIO[5] / (MOSI)
7	QGPIO[6] / (SCK)	8	GND
9	QGPO[1] / TXD1	10	QGPI[1] / RXD1 / C_CNRX0
11	QGPO[2] / TXD2/ C_CNTX0	12	QGPI[2] / RXD2

Table 6- QSMCM Connector Pinout

MIOS

Pin No	Function	Pin No.	Function
1	MPIO[0]	2	MPIO[1]
3	MPIO[2]	4	MPIO[3]
5	MPIO[4]	6	MPIO[5]
7	MPIO[6]	8	MPIO[7]
9	MPIO[8]	10	MPIO[9]
11	MPIO[10]	12	MPIO[11]
13	MPIO[12]	14	MPIO[13]
15	MPIO[14]	16	MPIO[15]
17	MPWM[0]	18	MPWM[1]
19	MPWM[2]	20	MPWM[3]
21	MPWM[16]	22	MPWM[17]
23	MPWM[18]	24	MPWM[19]
25	MDA[11]	26	MDA[12]
27	MDA[13]	28	MDA[14]
29	MDA[15]	30	MDA[27]
31	MDA[28]	32	MDA[29]
33	MDA[30]	34	MDA[31]
35	PUL_SEL	36	GND

Table 7- MIOS Connector Pinout

Interrupt port

Pin No	Function	Pin No.	Function
1	IRQ[0]	2	IRQ[1]
3	IRQ[2]	4	IRQ[3]
5	IRQ[4]	6	IRQ[5]
7	IRQ[6]	8	IRQ[7]
9	IRQOUT	10	FRZ

Table 8- IRQ Connector Pinout

Control Port

Pin No	Function	Pin No.	Function
1	CS0	2	CS1
3	CS2	4	CS3
5	WE0	6	WE1
7	WE2	8	WE3
9	TSIZ[0]	10	TSIZ[1]
11	RD_WR	12	BURST
13	BDIP	14	TS
15	TA	16	TEA
17	RSTCONF	18	BI
19	OE	20	RD_WR
21	SRESET	22	HRESET
23	EPEE	24	PORESET
25	BOEPEE	26	BG
27	BB	28	BR
29	GND	30	GND
31	EXTCLK	32	CLKOUT
33	ENGCLK	34	GND

Table 9 - Control Port Connector Pinout (0.1")

Address Port

Pin No	Function	Pin No.	Function
1	ADDR31	2	ADDR30
3	ADDR29	4	ADDR28
5	ADDR27	6	ADDR26
7	ADDR25	8	ADDR24
9	ADDR23	10	ADDR22
11	ADDR21	12	ADDR20
13	ADDR19	14	ADDR18
15	ADDR17	16	ADDR16
17	ADDR15	18	ADDR14
19	ADDR13	20	ADDR12
21	ADDR11	22	ADDR10
23	ADDR9	24	ADDR8
25	GND	26	GND

Table 10- Address Port Connector Pinout (0.1")

Databus Port

Pin No	Function	Pin No.	Function
1	DATA0	2	DATA1
3	DATA2	4	DATA3
5	DATA4	6	DATA5
7	DATA6	8	DATA7
9	DATA8	10	DATA9
11	DATA10	12	DATA11
13	DATA12	14	DATA13
15	DATA14	16	DATA15
17	DATA16	18	DATA17
19	DATA18	20	DATA19
21	DATA20	22	DATA21
23	DATA22	24	DATA23
25	DATA24	26	DATA25
27	DATA26	28	DATA27
29	DATA28	30	DATA29
31	DATA30	32	DATA31
33	GND	34	GND

Table 11- Databus Connector Pinout (0.1")

Logic Analyser Connectors

MICTOR A – Address and Chip Selects

Pin No	Function	Pin No.	Function
1	---	2	---
3	GND	4	---
5	TS*	6	CLKOUT
7	PORESET*	8	A16
9	KAPWR	10	A17
11	EXTCLK	12	A18
13	---	14	A19
15	CS0*	16	A20
17	CS1*	18	A21
19	CS2*	20	A22
21	CS3*	22	A23
23	A8 (MSB)	24	A24
25	A9	26	A25
27	A10	28	A26
29	A11	30	A27
31	A12	32	A28
33	A13	34	A29
35	A14	36	A30
37	A15	38	A31 (LSB)

Table 12- Logic Analyser Connector 1

MICTOR B - Data

Pin No	Function	Pin No.	Function
1	---	2	---
3	GND	4	---
5	BI* / STS*	6	TA*
7	D0 (MSB)	8	D16
9	D1	10	D17
11	D2	12	D18
13	D3	14	D19
15	D4	16	D20
17	D5	18	D21
19	D6	20	D22
21	D7	22	D23
23	D8	24	D24
25	D9	26	D25
27	D10	28	D26
29	D11	30	D27
31	D12	32	D28
33	D13	34	D29
35	D14	36	D30
37	D15	38	D31 (LSB)

Table 13- Logic Analyser Connector 2

MICTOR C – Control

Pin No	Function	Pin No.	Function
1	---	2	---
3	GND	4	---
5	RD/WR*	6	TEA*
7	CR* / IRQ2*	8	BURST*
9	KR & on ETAS (IRQ1*)	10	BDIP*
11	RSTCONF*	12	OE*
13	IWP0	14	WE0*
15	IWP1	16	WE1*
17	BR*	18	WE2*
19	BB*	20	WE3*
21	LWP0 / IRQOUT*	22	AT[2] / IRQ4*
23	BG*	24	TSIZ0
25	DSCK	26	TSIZ1
27	DSDO	28	VFLS[0] / MPIO32B[3] / MSEO
29	DSDI	30	VFLS[1] / MPIO32B[4]
31	---	32	PTR / FRZ
33	VF[0] / MPIO32B[0] / MDO[1]	34	RETRY* / IRQ3*
35	VF[1] / MPIO32B[1] / MCKO	36	SRESET*
37	VF[2] / MPIO32B[2] / MSEI	38	HRESET*

Table 14- Logic Analyser Connector 3

CPLD

Accomodation for a complex programmable logic device (Altera EPM7064B) (U25) has been made on this board. The reason it is included is to allow the demonstration of the hardware reservation protocol used in a multi-master system.

Table 1. MAX 7000B Device Features

Feature	EPM7032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	3.5	3.5	4.0	5.0	5.5
t_{SU} (ns)	2.1	2.1	2.5	3.3	3.6
t_{FSU} (ns)	1.0	1.0	1.0	1.0	1.0
t_{CO1} (ns)	2.4	2.4	2.8	3.3	3.7
f_{CNT} (MHz)	303.0	303.0	243.9	188.7	163.9

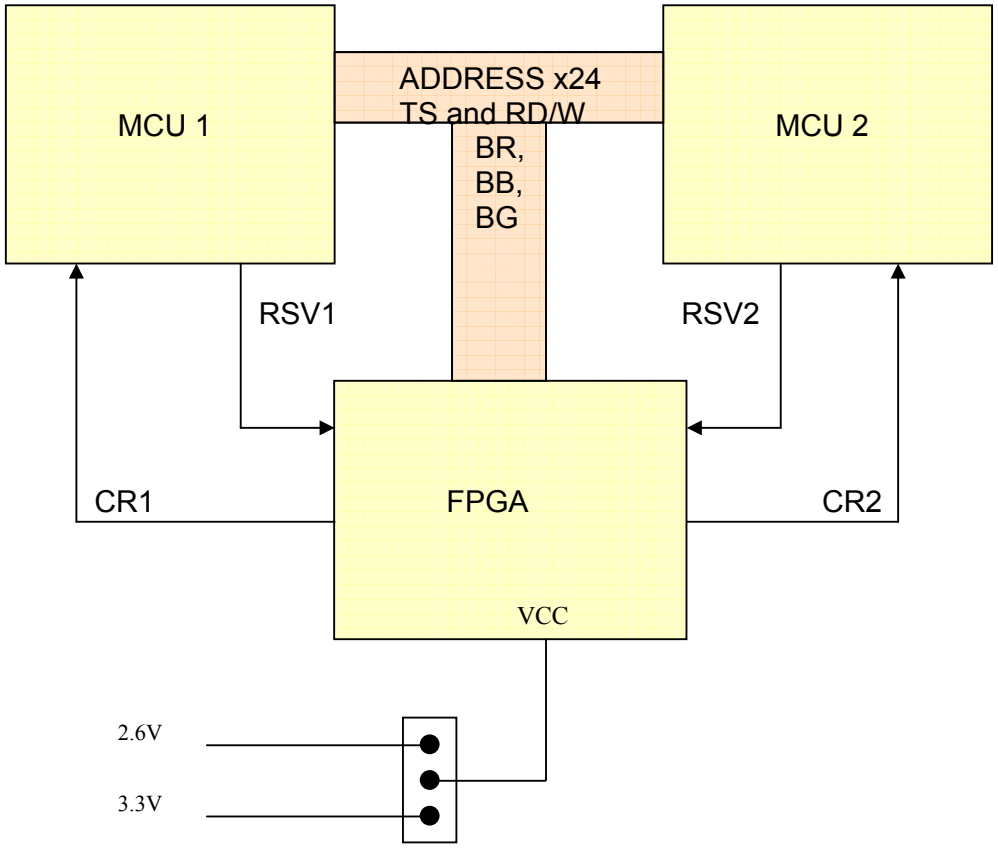


Figure 8– FPGA connections

Layout

The EVB was designed with EMC and signal integrity in mind. The board was an eight layer design with the following stack up:

1. Signal
2. 5V
3. Signal
4. 2V6
5. GND
6. Signal
7. 5V
8. Signal

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