MPC5604EEVB64 Evaluation board User Manual

For MPC5604E Evaluation/Validation

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1 Introduction

The MPC5604EEVB64 Evaluation Board (EVB) is based on the e200z0 Power Architecture®. This board is shipped with the PPC5604EEMLH 64-pin LQFP MCU populated to allow the evaluation of the full functionality of this part.

This board is designed as a validation platform with the maximum flexibility. Where possible it is also designed for power and speed but the primary goal of this system is to allow main usecases of this processor.

2 References

- MPC5604ERM Reference Manual
- MPC5604E Data Sheet

Contents

freescale™ semiconductor

3 EVB Features

The following is a list of evaluation board features:

MPC5604E External Interfaces

- Video Encoder Wrapper connected to Omnivision connector
- Serial Audio Interface connected to the Audio connector
- Onboard Ethernet physical interface plus MII lite connector
- Crystal / clock
- JTAG
- One LIN and one UART interface selectable through Jumper setting
- One FlexCAN interface
- External Interrupts
- ADC connector

NOTE

Before the EVB is used or power is applied, please read the complete document on how to correctly configure the board. Failure to correctly configure the board may cause irreparable component, MCU or VB damage.

4 Configuration

This section details the configuration of each of the EVB functional blocks.

Throughout this document, all of the default jumper and switch settings are clearly marked with "(D)" and are shown in blue text. This should allow a more rapid return to the default state of the EVB if required. The EVB is designed with ease of use in mind and is segmented into functional blocks as shown below. Detailed silkscreen legend is used throughout the board to identify all switches, jumpers and user connectors.

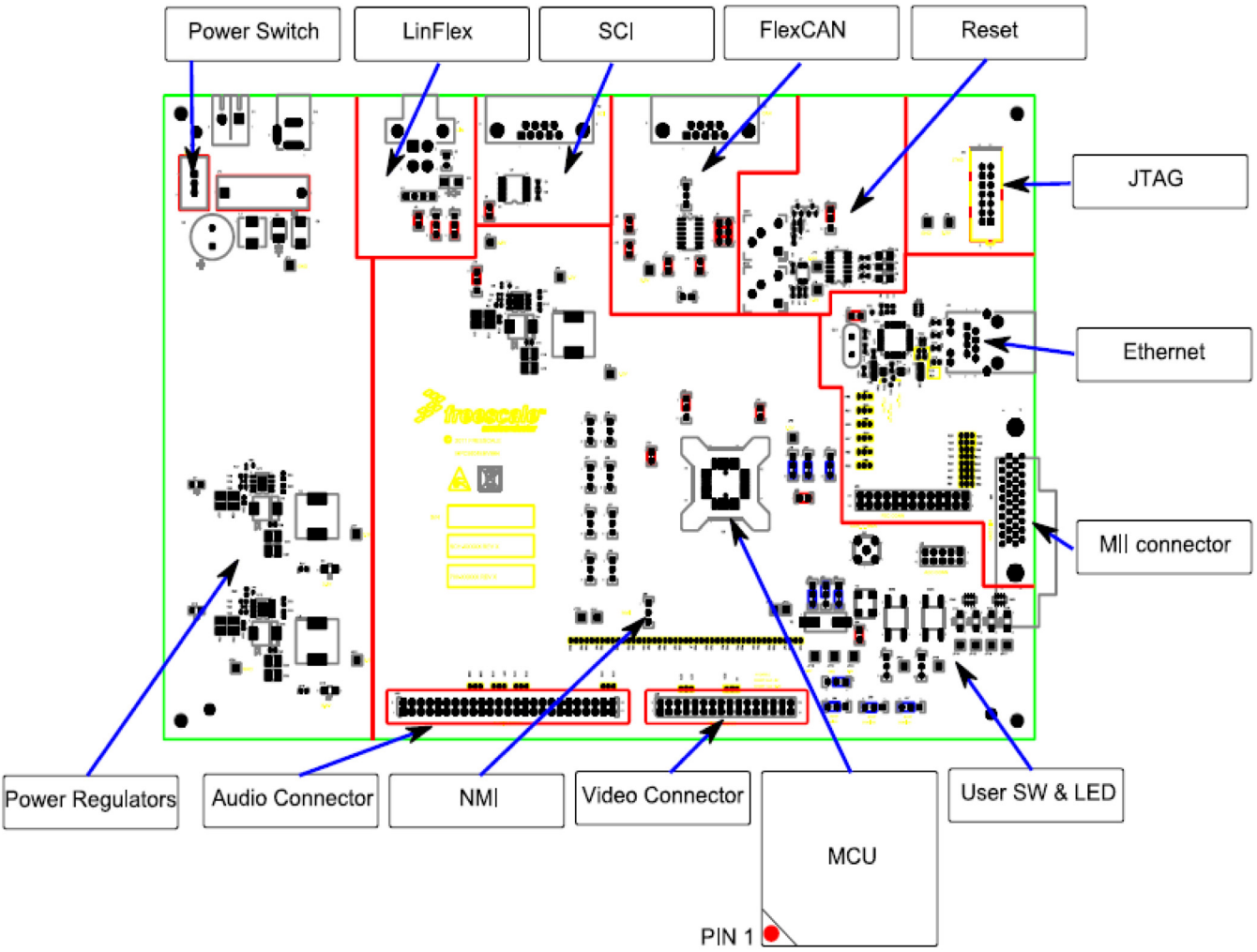


Figure 1. Evaluation board silkscreen legend

4.1 Processor

The MPC5604E processor is the fundamental control chip on the MPC5604EEVB64. This is a version 1 Power Architecture running at a maximum core speed of 64 MHz. The MPC5604EEVB64 allows you to fully evaluate the feature set of the MPC5604E MCU. Refer to Section 3, "EVB Features to review the list of board features.

4.2 Power

The EVB requires an external power supply voltage of 12V DC, minimum 1A. This allows the EVB to be easily used in a vehicle if required. The single input voltage is regulated on-board using switching regulators to provide the necessary EVB and MCU operating voltages of 5.0 V, 3.3 V and 1.2 V. For flexibility there are two different power supply input connectors on the EVB as detailed below.

4.3 Power supply Connectors

2.1 mm Barrel Connector – P4:

This connector should be used to connect the supplied wall-plug mains adapter.

NOTE

If a replacement or alternative adapter is used, care must be taken to ensure that the 2.1 mm plug uses the correct polarization as shown in Figure 2.

Figure 2. 2.1 mm Power Connector

2-Way Lever Connector – P1:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarization of the connectors is clearly marked on the bottom site of the EVB. Care must be taken to ensure correct connection.

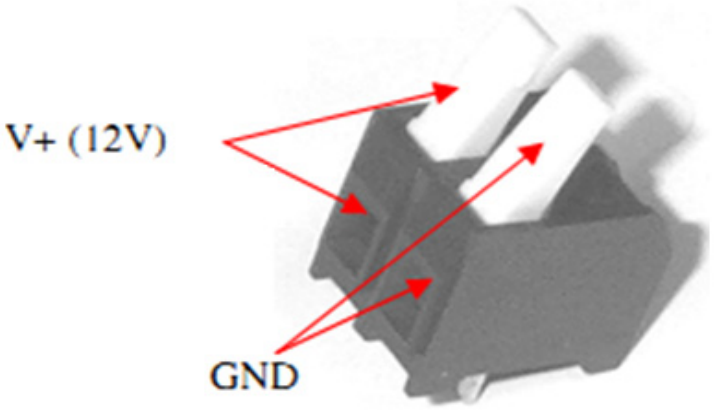


Figure 3. 2-Level Power Connector

4.4 Power Switch (SW1)

Side switch SW1 can be used to isolate power supply input from the EVB voltage regulators if required:

- Position 1 will turn the EVB OFF
- Position 3 will turn the EVB ON

4.5 Power Status—LEDs and Fuse

When Power is applied to the EVB, the Green Power LEDs adjacent to 5 V and 3.3 V of the voltage regulators show the presence of the supply voltage.

Green LED D9 = 3.3 V for EVB supply

Green LED D16 = 5 V for EVB supply

If there is no power to the MCU it is possible that either power switch SW1 is in the “OFF” position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the bias of your power supply connection then replace fuse F1 with a 20 mm 2 A fast blow fuse.

4.6 MCU supply routing and Jumpers (J16, J18, J19, J20, J23)

The EVB is designed to run the MCU at two supported regulation modes:

Internal regulation mode

In this mode the I/O supply, Ballast supply and ADC supply are at the same potential of typical 3.3 V

(+/- 10%). To reduce power dissipation on the chip, the possibilities of connecting the I/O supply with the Ballast supply via a small resistor 2.5 Ω is being explored. This will lead to the Ballast supply being lower than the I/O supply.

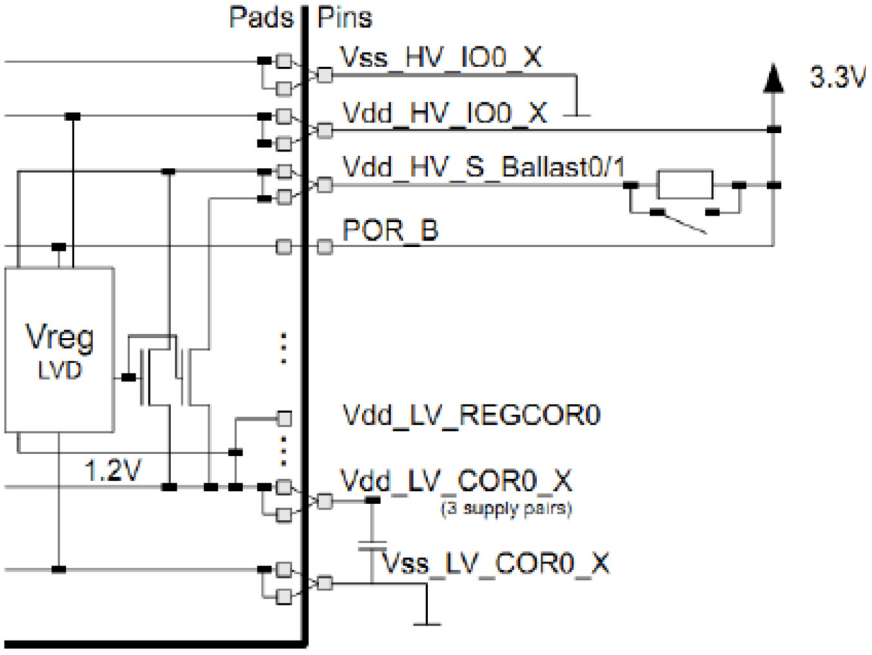


Figure 4. Internal regulation mode

External regulation mode

In this mode, the Ballast supply is shorted to 1.2 V (+/-10%) generated from an external regulator. The I/O supply and the MCU ADC supply continues to be at 3.3 V (+/-10%).

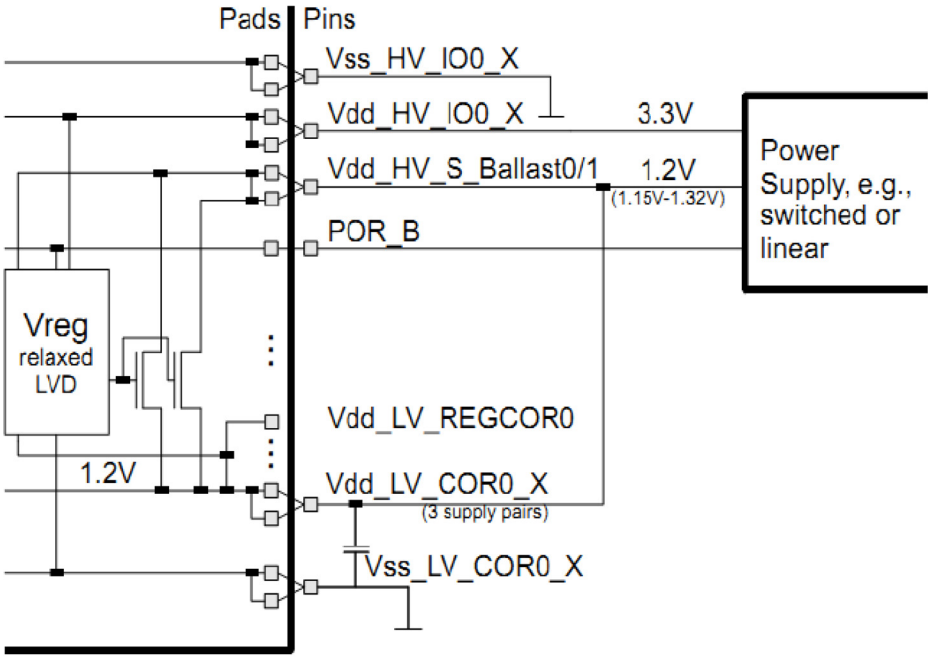


Figure 5. External regulation mode

The FlexCAN circuity also has 5 V supplier to the transceiver.

Table 1. MCU Power Supply Jumpers – internal regulation mode

Power Domain	Jumper	Position	Description
1.2 V	J18 (VDD_LV)	X	This supplies VDD_LV supply pins
3.3 V	J19 (V_BALLAST_IN)	1-2	This supplies VDD_S_BALAST supply pin
3.3 V	J20 (V_BALLAST_IN_HDR)	2-3 **(D)**	VDD_S_BALAST routed via BALAST resistor
3.3 V	J16 (VDD_HV)	1-2 **(D)**	This supplies VDD_HV supply pins
3.3 V	J23 (VDD_HV_ADDR)	1-2 **(D)**	ADC reference voltage 3.3 V

The jumper configuration shown in Table 1, details the default state (D) of the EVB. In this configuration all power is supplied from the regulators.

Table 2. MCU Power Supply Jumpers – external regulation mode

Power Domain	Jumper	Position	Description
1.2 V	J18 (VDD_LV)	1-2 **(D)**	This supplies VDD_LV supply pins
3.3 V	J19 (V_BALLAST_IN)	2-3 **(D)**	This supplies VDD_S_BALAST supply
3.3 V	J20 (V_BALLAST_IN_HDR)	2-3 **(D)**	VDD_S_BALAST routed via BALAST resistor
3.3 V	J16 (VDD_HV)	1-2 **(D)**	This supplies VDD_HV supply pins
3.3 V	J23 (VDD_HV_ADR)	1-2 **(D)**	ADC reference voltage 3.3 V

The jumper configuration shown in Table 2, details the default state **(D)** of the EVB. In this configuration all power supplied from the regulators.

4.7 MCU clock control - Main Clock Selection (J30, J31, J32, J34)

EVB supports three possible MCU clock sources:

- The local 25 MHz oscillator circuit (Y2)
- An 8 MHz Oscillator module (Y1) on the EVB, driving the MCU EXTAL signal
- An external clock input to the EVB via the SMA connector, driving the MCU EXTAL signal

The clock circuity is shown in the diagram below. Please refer to the appropriate EVB schematic for specific jumper numbers and circuity.

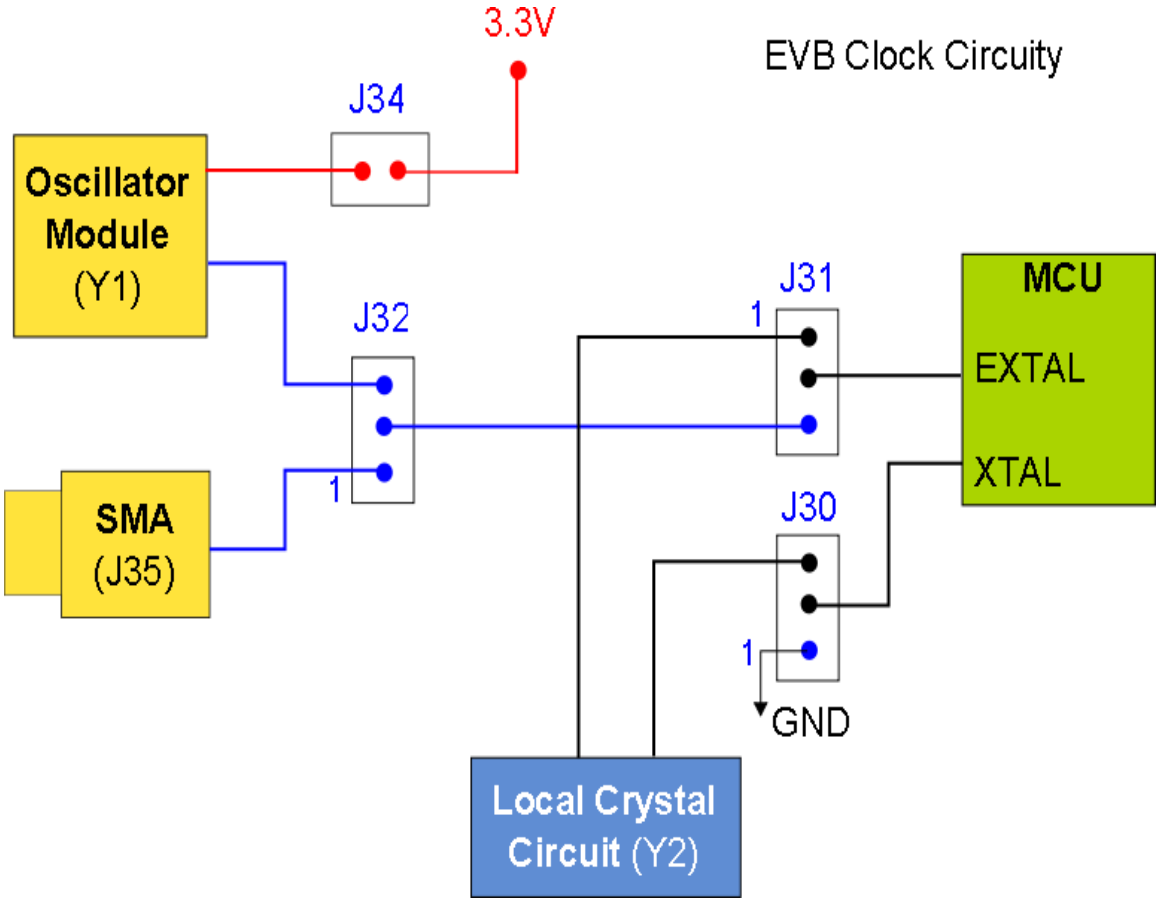


Figure 6. EVB Clock Selection

Table 3. Table Clock source jumper selection (J30, J31, J32, J34)

Jumper	Position	PCB Legend	Description
J34 (Y1 PWR)	**FITTED (D)** REMOVED		EVB oscillator module Y1 is powered EVB oscillator module Y1 is not powered
J32 (OSC SEL)	1-2 **2-3 (D)**	EXTAL-SMA OSC-MOD	SMA external square wave input 8 MHz Oscillator is routed from Y1
J30 Must Match J31	1-2 **2-3 (D)**	Y2 GND	MCU clock is Y2 XTALIN GND
J31 Must Match J30	**1-2 (D)** 2-3	EVB-EXTAL Y2	MCU clock is selected by J68 MCU clock is Y2 XTALOUT

NOTE

The MPC5604E clock circuity is 3.3 V based. Any external clock signal driven into the SMA connector must have a maximum voltage of 3.3 V.

4.8 Reset Boot Configuration (J44, J46, J47)

The MPC5604E has 3 boot configuration jumpers (BOOTCFG) that determine the boot location of the MCU based at POR (Power On Reset). This is shown in the Table 4:

Table 4. BOOTCFG Control

J47 (FAB)	J44 (ABS0)	J46 (ABS2)	Boot ID	Boot Mode
1-2	2-3	2-3	—	Serial Boot LinFlex without autobaud
1-2	1-2	2-3	—	Serial Boot FlexCAN without autobaud
1-2	2-3	1-2	—	Serial Boot via LinFlex or FlexCAN in autobaud
2-3	—	—	Valid	SC (Single Chip)
2-3	—	—	Not Valid	Safe Mode

4.9 NEXUS

The EVB supports a standard JTAG cable with a 14-pin 0.1” walled header footprint.

4.9.1 Debug Connector Pinouts

The EVB is fitted with 14-pin JTAG connector. The following diagram shows the 14-pin JTAG connector pin out (0.1” keyed header).

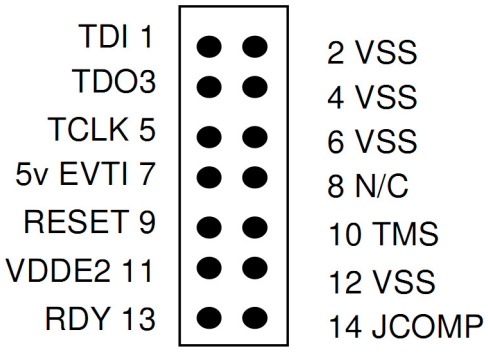


Figure 7. MPC5604E JTAG Connector

NOTE

In order to preserve the ability to accurately measure power consumption of the MCU pins, the JTAG connector reference voltages will be sourced directly from the 3.3 V regulator.

4.10 CAN Configuration (J10, J11, J12, J6, J9)

The EVB has one NXP TJA1041T high speed CAN transceiver on the MCU CAN channel. This can operate with 3.3 V I/O from the MCU. For flexibility, the CAN transceiver I/O is connected to a standard 0.1” connector and DB9 connector at the top edge of the PCB. Connectors P6 and P3 provides the CAN bus level signal interface for CAN-A. The pin out for these connectors is shown below.

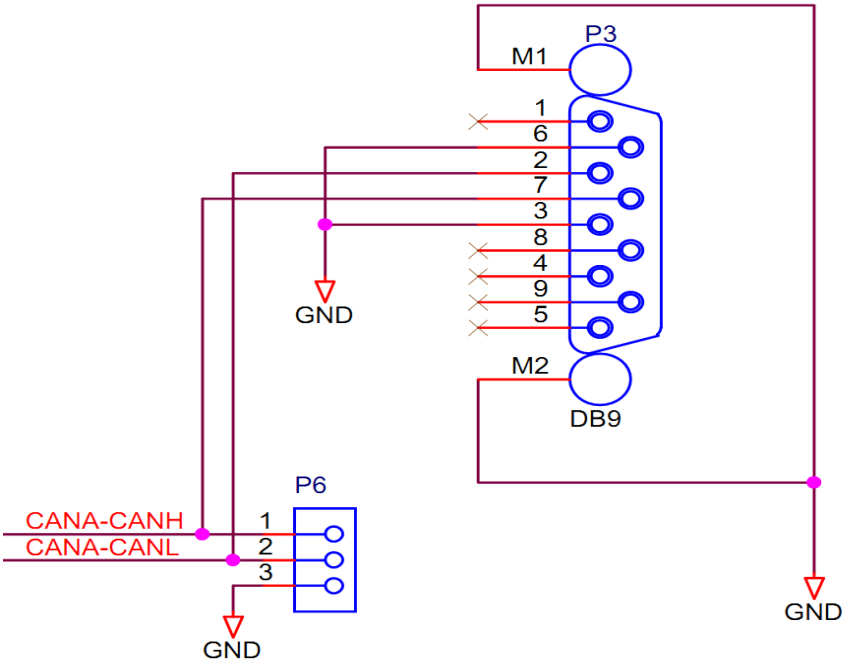


Figure 8. CAN physical interface connector

Table 5. CAN Control Jumpers (J10, J11, J12, J6, J9)

Jumper	Position	PCB Legend	Description
J11	**FITTED (D)** REMOVED		• 5 V is applied to CAN transceiver VCC • No 5 V power is applied to CAN transceiver
J12	**FITTED (D)** REMOVED		• 12 V Power is applied to CAN transceiver VBAT • No 12 V power is applied to CAN transceiver
J6	**FITTED (D)** REMOVED	TX	• MCU CAN_TXD is connected to CAN controller • MCU CAN_TXD is NOT routed to CAN controller.
J10	**FITTED (D)** REMOVED	RX	• MCU CAN_RXD is connected to CAN controller • MCU CAN_RXD is NOT routed to CAN controller.
J9 Position 1-2	**FITTED (D)** REMOVED	WAKE	• CAN Transceiver WAKE is connected to GND • WAKE is not connected and available on Pin 2
J9 Position 3-4	**FITTED (D)** REMOVED	STB	• CAN Transceiver STB is connected to 5 V • STB is not connected and available on Pin 4
J9 Position 5-6	**FITTED (D)** REMOVED	EN	• CAN Transceiver is Enabled • EN is not connected and available on Pin 6

Access to the Error and inhibit signals from the transceivers is provided on J14.

NOTE

You must do the fitting of the jumper headers carefully, as they can easily be fitted in the incorrect orientation.

4.11 RS232 Configuration (J3, J7, J8)

The EVB has a single MAX3223 RS232 transceiver device, providing RS232 signal translation for the MCU LINFlex channel.

The RS232 output from the MAX3223 device is connected to a DB9 connector, allowing a direct RS232 connection to a PC or terminal. Connector P2 provides the RS232 level interface for MCU SCI (LINFlex). The connector pinout is detailed below.

NOTE

The hardware flow control is not supported on this implementation.

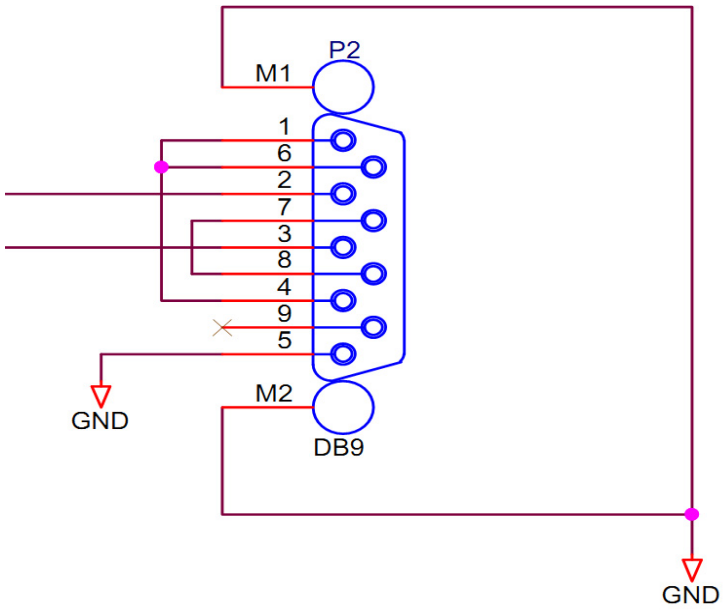


Figure 9. RS232 Physical Notifies Connector

The MPC5604E LINFlex also provides hardware LIN master capability which is supported on the EVB via LIN transceiver. Jumpers J7 and J8 are provided to isolate the MCU LINFlex signals from the RS232 interface as described below. There is also a global power jumper (J3) controlling the power to the RS232 transceiver.

Table 6. RS232 Control Jumpers

Jumper	Position	Description
J3 (SCI-PWR)	**FITTED (D)** REMOVED	• Power is applied to the MAX3223 transceiver • No power is applied to the MAX3223 transceiver
J7	2-3 **(D)** REMOVED	• MCU TXD is routed to MAX3223 • MCU TXD signal is disconnected from RS232/LIN
J8	2-3 **(D)** REMOVED	• MCU RXD is routed to MAX3223 • MCU RXD signal is disconnected from RS232/LIN

The default configuration enables SCI. RS232 compliant interfaces (with no hardware flow control) are available at DB9 connector P2. If the MCU is configured such that SCI is set as a normal I/O port, then

the relevant jumpers must be removed to avoid any conflicts occurring. If required, jumper J3 can be used to completely disable the SCI transceiver.

4.12 LIN Configuration (J2, J5, J7, J8)

The EVB is fitted with one Freescale MCZ33661EF LIN transceiver. The LINFlex module incorporates a UART mode, and as such, the LIN transceiver are connected to the TX and RX signals of SCI via UART.

For flexibility, the LIN transceiver is connected to a standard 0.1” connector (P7) and to one pin molex connector (J1) at the top edge of the PCB as shown in the figure below.

For ease of use, the 12 V EVB supply is fed to pin1 of the P7 header and the LIN transceiver power input to pin 2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of header P7 using a 0.1” jumper shunt.

** Ensure P7 is added before running LIN as it is not the default on the EVB

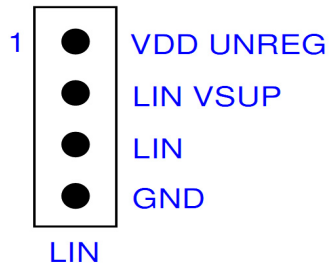


Figure 10. LIN physical Interface Connector P7

Along with the MCU signal routing jumpers (J7 / J8), there is jumper (J5) to enable or disable the LIN transceiver and jumper (J2) which determines if the LIN transceiver is operating in master or slave mode, as defined in the table below.

Table 7.

Jumper	Position	Description
J2	FITTED **REMOVED (D)**	• LIN transceiver is configured for LIN Master mode • LIN transceiver is configured for LIN Slave mode
J5*	**FITTED (D)** REMOVED	• The LIN transceiver is enabled • The LIN transceiver is disabled
J7	**2-3 (D)** 1-2	• MCU LIN_TXD is connected to SCI TX • MCU LIN0_TXD is connected to LIN Physical
J8	**2-3 (D)** 1-2	• MCU LIN_RXD is connected to SCI TX • MCU LIN_RXD is connected to LIN Physical

NOTE

Jumper J5 do not route power to LIN transceivers, they only control an enable line on the LIN device. Power to the LIN transceiver is supplied via connector P7, Pin 2.

The Default LIN configuration is with the module enabled in master mode, LIN slave mode can be enabled by removing jumper J2.

4.13 Ethernet

4.13.1 Ethernet Physical Interface (J22)

The EVB is fitted with a National Semiconductor DP83848C Ethernet physical interface (U10) and a RJ45 connector with integrated activity LEDs and magnetics (J24).

The National Semiconductor DP83848C physical interface is connected to the MII on the MPC5604E. This is a fixed connection with no means of isolation. Pullups are also present on some of these signals. These are detailed in the table below. Please be aware of this when using the related GPIOs.

Table 8. Pull up/Pull down resistors for Ethernet Physical

Port Pin	Pull Direction	Strength
FEC_CRS	Down (GND)	2.2 kΩ
FEC_RX_ER	Down (GND)	2.2 kΩ
FEC_RX_DV	Down (GND)	2.2 kΩ
FEC_RXD0	Down (GND)	2.2 kΩ

Table 8. Pull up/Pull down resistors for Ethernet Physical

Port Pin	Pull Direction	Strength
FEC_RXD1	Down (GND)	2.2 kΩ
FEC_RXD2	Down (GND)	2.2 kΩ
FEC_RXD3	Down (GND)	2.2 kΩ
FEC_TX_EN	Down (GND)	2.2 kΩ
FEC_TXD0	Down (GND)	2.2 kΩ
FEC_TXD1	Down (GND)	2.2 kΩ
FEC_TXD2	Down (GND)	2.2 kΩ
FEC_TXD3	Down (GND)	2.2 kΩ
FEC_MDC_PHY	Up (3.3 V)	1.5 kΩ
FEC_MDIO_PHY	Up (3.3 V)	1.5 kΩ

The voltage domain that is used by the GPIO should be set to 3.3 V when power is applied to the physical interface. Power can be removed from the physical interface via J22.

Table 9. Ethernet Physical Interface Power Supply Enabled (J22)

Jumper	Position	PCB legend	Description
J22 (PHY PWR)	**FITTED (D)** REMOVED	PHY PWR	• The DP83848C Ethernet Physical Interface is powered from the 3.3 V SR. • The DP83848C Ethernet Physical Interface is not powered.

4.13.2 Ethernet MII connector (J49)

An universal 40-pin MII Connector is also provided on the board to provide possibility to connect customer Ethernet Physical Interface to MPC5604E interface signals. Since this connector is normally used by the Ethernet PHY daughter cards of standard PHY vendors, this provides a flexibility of supporting validation with multiple PHY vendors.

Connector pin definition is located in the Section 6.1, “FEC (J33, J49) below.

Following resistors must be populated to enable connection between MPC5604E and MII connector on board:

Table 10. Resistor configuration for MPC5604E MII interface routed to MII connector

Resistor to be populated	Value	Description
R62	0Ω	FEC_TX_CLK routed to FEC_TX_CLK_CONN
R60	0Ω	FEC_TX_EN routed to FEC_TX_EN_CONN
R58	0Ω	FEC_TXD0 routed to FEC_TXD0_CONN
R56	0Ω	FEC_TXD1 routed to FEC_TXD1_CONN
R54	0Ω	FEC_TXD2 routed to FEC_TXD2_CONN
R53	0Ω	FEC_TXD3 routed to FEC_TXD3_CONN
R82	0Ω	FEC_RXD3 routed to FEC_RXD3_CONN
R84	0Ω	FEC_RXD2 routed to FEC_RXD2_CONN
R86	0Ω	FEC_RXD1 routed to FEC_RXD1_CONN
R88	0Ω	FEC_RXD0 routed to FEC_RXD0_CONN
R90	0Ω	FEC_RX_DV routed to FEC_RX_DV_CONN
R92	0Ω	FEC_RX_CLK routed to FEC_RX_CLK_CONN
R94	0Ω	FEC_MDIO routed to FEC_MDIO_CONN

4.14 Video Connector (J45)

EVB has a possibility to connect Camera module to Video connector (J45). Camera signals are then routed to the Video Encoder Wrapper module of MPC5604E. Video connector fits to standard connector used on Omnivision camera evaluation boards.

Connector pin definition is located in the Section 6.4, “VIDEO (J45) below.

Following resistors and capacitors have to be populated to enable connection between MPC5604E and Video connector on board:

Table 11.

Resistor and capacitor to be populated	Value	Description
R33	10Ω	PORT_A0 routed to CON_VID_DATA11
R26	10Ω	PORT_A1 routed to CON_VID_DATA10
R35	10Ω	PORT_A2 routed to CON_VID_DATA9
R28	10Ω	PORT_A3 routed to CON_VID_DATA8
R37	10Ω	PORT_A4 routed to CON_VID_DATA7
L4	75Ω	PORT_A5 routed to CON_VID_CLK
R39	10Ω	PORT_A6 routed to CON_VID_VSYNC
R41	10Ω	PORT_A7 routed to CON_VID_HSYNC
R43	10Ω	PORT_A8 routed to CON_VID_DATA6

Table 11.

Resistor and capacitor to be populated	Value	Description
R31	10Ω	PORT_A9 routed to CON_VID_DATA5
R45	10Ω	PORT_A10 routed to CON_VID_DATA4
R47	10Ω	PORT_A11 routed to CON_VID_DATA3
R49	10Ω	PORT_A12 routed to CON_VID_DATA2
R77	10Ω	PORT_A15 routed to VID_PWDN
L6	75Ω	PORT_C4 routed to MC_RGM_ABS0

Most of the Omnivision camera evaluation boards are configured via I2C interface. For this purpose J27, J28, J39 and J37 should be connected correctly. For pin definitions see Section 6.8, “I2C clock selection (J27, J28, J36, J37, J39, J40).

4.14.1 Audio Connector

EVB has a possibility to connect Sahara SGTL5000 daughter card to Audio connector J48. Audio signals are routed to Serial Audio Interface module of MPC5604E.

Connector pin definition is located in the Section 6.3, “Audio (J48) below.

Following resistors and capacitors have to be populated to enable connection between MPC5604E and Audio connector on board.

Table 12.

Resistor and capacitor to be populated	Value	Description
R64	0Ω	PORT_C3 routed to ETC1
R66	0Ω	PORT_C2 routed to ETC0
R32	0Ω	PORT_A0 routed to SAI0_DATA0
R25	0Ω	PORT_A1 routed to SAI0_DATA1
R34	0Ω	PORT_A2 routed to SAI0_DATA2
R27	0Ω	PORT_A3 routed to SAI0_DATA3
R36	0Ω	PORT_A4 routed to SAI0_SYNC
R29	0Ω	PORT_A5 routed to SAI1_SYNC
R38	0Ω	PORT_A6 routed to SAI2_SYNC
R40	0Ω	PORT_A7 routed to SAI0_BCLK
R42	0Ω	PORT_A8 routed to SAI2_DATA0
R30	0Ω	PORT_A9 routed to SAI2_BCLK
R44	0Ω	PORT_A10 routed to SAI2_MCLK

Table 12.

Resistor and capacitor to be populated	Value	Description
R70	0Ω	PORT_B1 routed to SAI1_DATA0
R72	0Ω	PORT_B0 routed to SAI1_BCLK
R76	0Ω	PORT_A15 routed to SAI1_MCLK
R78	0Ω	PORT_C4 routed to SAI0_MCLK

Sahara SGTL5000 audio daughter card uses I2C interface for configuration. For this purpose J27, J28, J39 and J37 should be connected correctly. For pin definitions see Section 6.8, “I2C clock selection (J27, J28, J36, J37, J39, J40).

5 Default Jumper Summary Table

Table 13. Default Jumper Positions

Jumper Reference	Default Setting	Jump Count	Description
J2	REMOVED	1	Master Mode Pullup disable
J3	1-2	1	Power on SCI is enabled
J4	1-2	1	Power for User switches is disabled
J5	1-2	1	Power on LIN is enabled
J6	1-2	1	CAN TXD is connected to MCU
J7	2-3	1	UART TXD is connected to MCU
J8	2-3	1	UART RXD is connected to MCU
J9	1-2 3-4 5-6	3	CAN control signals are on
J10	1-2	1	CAN RXD is connected to MCU
J11	1-2	1	Power on CAN PHY is enabled
J12	1-2	1	Power on CAN PHY is enabled
J13	2-3	1	1.2 power supply switch is supplied from 12 V
J15	1-2	1	VPP_TEST should be grounded
J16	1-2	1	VDD_HV is enabled
J18	1-2	1	VDD_LV is enabled (external regulation mode)
J19	2-3	1	VDD_BALAST is powered from 1.2 V (external regulation mode)
J20	2-3	1	VDD_BALAST_IN resistor is connected
J21	2-3	1	JTAG_RST is connected to Ethernet PHY

Table 13. Default Jumper Positions

Jumper Reference	Default Setting	Jump Count	Description
J22	1-2	1	Power on Ethernet PHY is enabled
J23	1-2	1	Power on VDD_HV_ADR is enabled
J30	2-3	1	Use on board 8.0 MHz crystal
J31	1-2	1	Use on board 8.0 MHz crystal
J32	2-3	1	Use on board 8.0 MHz crystal
J34	1-2	1	Use on board 8.0 MHz crystal
J41	1-2	1	3.3 V connected to FEC MII connector
J44	2-3	1	MC_RGM_ABS0 is tied to ground
J46	2-3	1	MC_RGM_ABS2 is tied to ground
J47	2-3	1	MC_RGM_FAB is tied to ground

6 User Connector Descriptions

This section details the pinout of the EVB user connectors. The connectors are 0.1 inch pitch turned pin headers and are located at various locations on the EVB. They are grouped by port functionality and the PCB legend shows the respective port number adjacent to each pin.

6.1 FEC (J33, J49)

Table 14. FEC Connector Pinout (J33)

Pin	Function
1	GND
2	GND
3	FEC_TXD3
4	FEC_RXD2
5	FEC_TXD2
6	FEC_RXD3
7	FEC_TXD0
8	FEC_RXD1
9	FEC_TXD1
10	FEC_RXD0
11	FEC_TX_CLK
12	EC_RX_CLK
13	GND
14	GND
15	FEC_TX_EN

Table 14. FEC Connector Pinout (J33)

Pin	Function
16	NC
17	NC
18	NC
19	GND
20	GND
21	FEC_MDC
22	NC
23	FEC_MDIO
24	FEC_RX_DV
25	GND
26	GND

Table 15. MII Connector Pinout (J49)

Pin	Function
1	POWER_MII_CONN
2	MDIO
3	MDC
4	RXD3
5	RXD2
6	RXD1
7	RXD0
8	RXDV
9	RXCLK
10	RXER
11	TXER
12	TXCLK
13	TXEN
14	TXD0
15	TXD1
16	TXD2
17	TXD3
18	COL
19	CRS
20	POWER_MII_CONN
21	POWER_MII_CONN

Table 15. MII Connector Pinout (J49) (continued)

Pin	Function
22	GND
23	GND
24	GND
25	GND
26	GND
27	GND
28	GND
29	GND
30	GND
31	GND
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	POWER_MII_CONN

6.2 ADC(J38)

Table 16. ADC Connector Pinout (J38)

Pin	Function
1	GND
2	GND
3	ADC0_AN[11]
4	ADC0_AN[13]
5	GND
6	GND
7	ADC0_AN[12]
8	ADC0_AN[14]
9	GND
10	GND

6.3 Audio (J48)

Table 17. Audio Connector Pinout (J48)

Pin	Function
1	3.3 V
2	GND
3	SAI0_DATA3
4	GND
5	SAI0_DATA2
6	GND
7	SAI0_DATA1
8	GND
9	SAI0_DATA0
10	GND
11	SAI0_BCLK
12	GND
13	SAI0_SYNC
14	GND
15	SAI0_MCLK
16	GND
17	ETC2/AN14 (ADC signal)
18	GND
19	AUD_IIC1_CLK

Table 17. Audio Connector Pinout (J48) (continued)

Pin	Function
20	GND
21	AUD_IIC1_DATA
22	GND
23	SAI1_D0
24	GND
25	SAI1_BCLK
26	GND
27	ETC1
28	GND
29	SAI1_SYNC
30	GND
31	SAI1_MCLK
32	GND
33	AUD_IIC0_CLK
34	GND
35	AUD_IIC0_DATA
36	GND
37	SAI2_DATA0
38	GND
39	SAI2_BCLK
40	GND
41	SAI2_SYNC
42	GND
43	SAI2_MCLK
44	GND
45	ETC0
46	GND
47	AN13(ADC signal)
48	GND
49	5V
50	GND

6.4 VIDEO (J45)

Table 18. Video Connector Pinout (J45)

Pin	Function
1	CON_VID_DATA4
2	CON_VID_DATA5
3	CON_VID_DATA6
4	CON_VID_DATA7
5	CON_VID_DATA8
6	CON_VID_DATA9
7	CON_VID_DATA10
8	CON_VID_DATA11
9	VID_PWDN
10	NC
11	VID_IIC_DATA
12	NC
13	VID_IIC_CLK
14	CON_VID_HSYNC
15	GND
16	CON_VID_VSYNC
17	GND
18	CON_VID_CLK
19	MC_RGM_ABS0
20	5 V
21	GND
22	5 V
23	CON_VID_DATA2
24	CON_VID_DATA3
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC
31	GND
32	GND

6.5 NMI (J29)

Table 19. NMI Connector Pinout (J29)

Pin	Function
1	GND
2	NMI
3	3.3 V

6.6 LINFLEX (P7)

Table 20. LINFLEX Connector Pinout (P7)

Pin	Function
1	12 V
2	LINC-VSUP
3	LINC-LIN
4	GND

6.7 FlexCAN (P6)

Table 21. FLEXCAN Connector Pinout (P6)

Pin	Function
1	CANH
2	CANL
3	GND

6.8 I2C clock selection (J27, J28, J36, J37, J39, J40)

Table 22. Routing IIC0 to Video Connector – video usecase

Signal description	Jumper Reference	Configuration	Description
IIC 0 clock	J25	2-3	Port_C5 routed to J39 as IIC0_CLK signal
	J39	1-2	IIC0_CLK signal routed to J28
	J28	2-3	IIC0_CLK is selected for Video IIC clock
IIC 0 data	J26	2-3	Port_C6 routed to J40 as IIC0_DATA signal
	J40	1-2	IIC0_DATA signal routed to J37
	J37	2-3	IIC0_DATA is selected for Video IIC data

Table 23. Routing IIC1 to Video Connector – video usecase

Signal description	Jumper Reference	Configuration	Description
IIC 1 clock	J27	1-2	Port_A13 routed to J28
	J28	1-2	IIC1_CLK signal is selected for Video IIC clock
IIC 1 data	J36	1-2	Port_A14 routed to J37
	J37	1-2	IIC1_DATA signal is selected for Video IIC data

Table 24. Routing IIC0 to Audio Connector – audio usecase

Signal description	Jumper Reference	Configuration	Description
IIC 0 clock	J25	2-3	Port_C5 routed to J39 as IIC0_CLK signal
	J39	2-3	IIC0_CLK signal selected for Audio IIC clock
IIC 0 data	J26	2-3	Port_C6 routed to J40 as IIC0_DATA signal
	J40	2-3	IIC0_DATA signal selected for Audio IIC data

Table 25. Routing IIC1 to Video Connector – audio usecase

Signal description	Jumper Reference	Configuration	Description
IIC 0 clock	J27	2-3	IIC1_CLK signal is selected for audio IIC clock
IIC 0 data	J36	2-3	IIC1_DATA signal is selected for audio IIC data

7 Known Bugs List

None

8 Schematic Diagrams

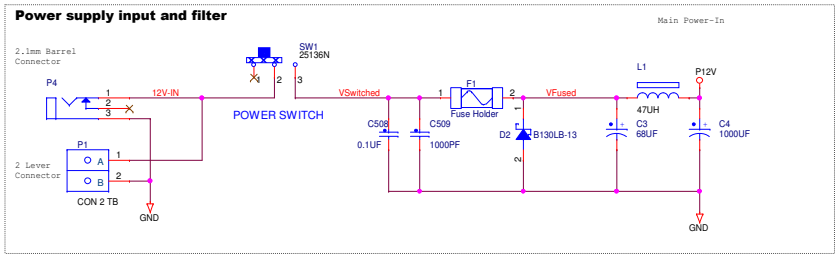
This section shows the schematic diagram of the MPC5604EEVB64.

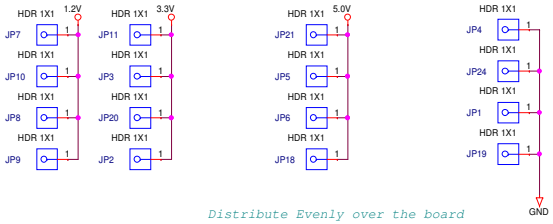
Following are the topics covered in the schematic:

Table 26. Schematic sections

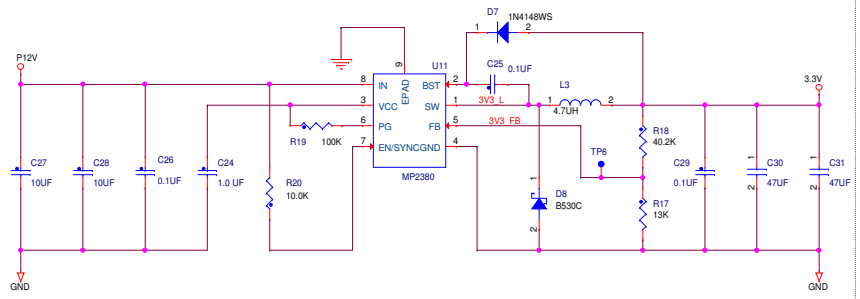
Power section	Sheet 2
Resistor MUX	Sheet 3
Video & Audio section	Sheet 4
MII Connector section	Sheet 5
Debug Interface section	Sheet 6
Reset & Clock section	Sheet 7
Ethernet Physical Interface and RJ45	Sheet 8
CAN Physical Interface	Sheet 9
LIN & SCI Physical Interface	Sheet 10
MPC5604E SoC	Sheet 11
LED & Switch section	Sheet 12
User I/O connectors	Sheet 13

Power supply input and filter

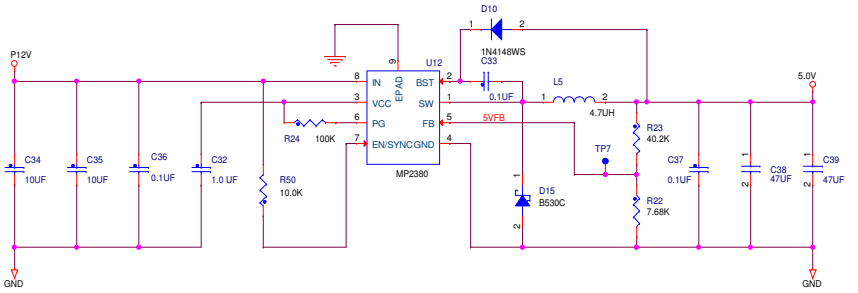


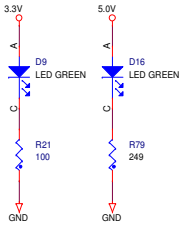


Power Supply 3.3V

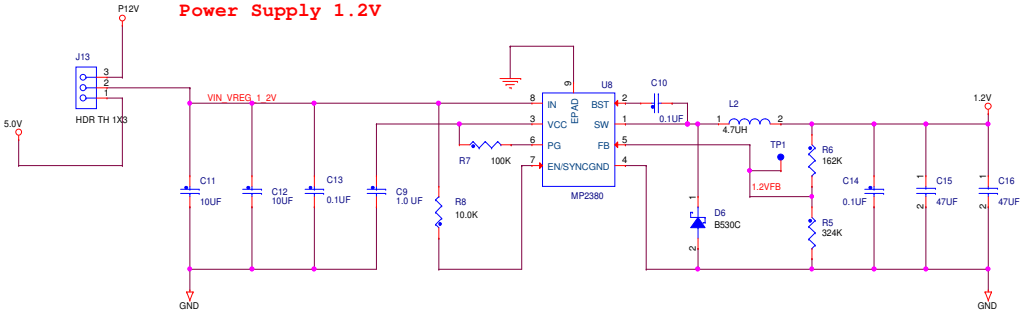


Power Supply 5.0 V





Power Supply 1.2V



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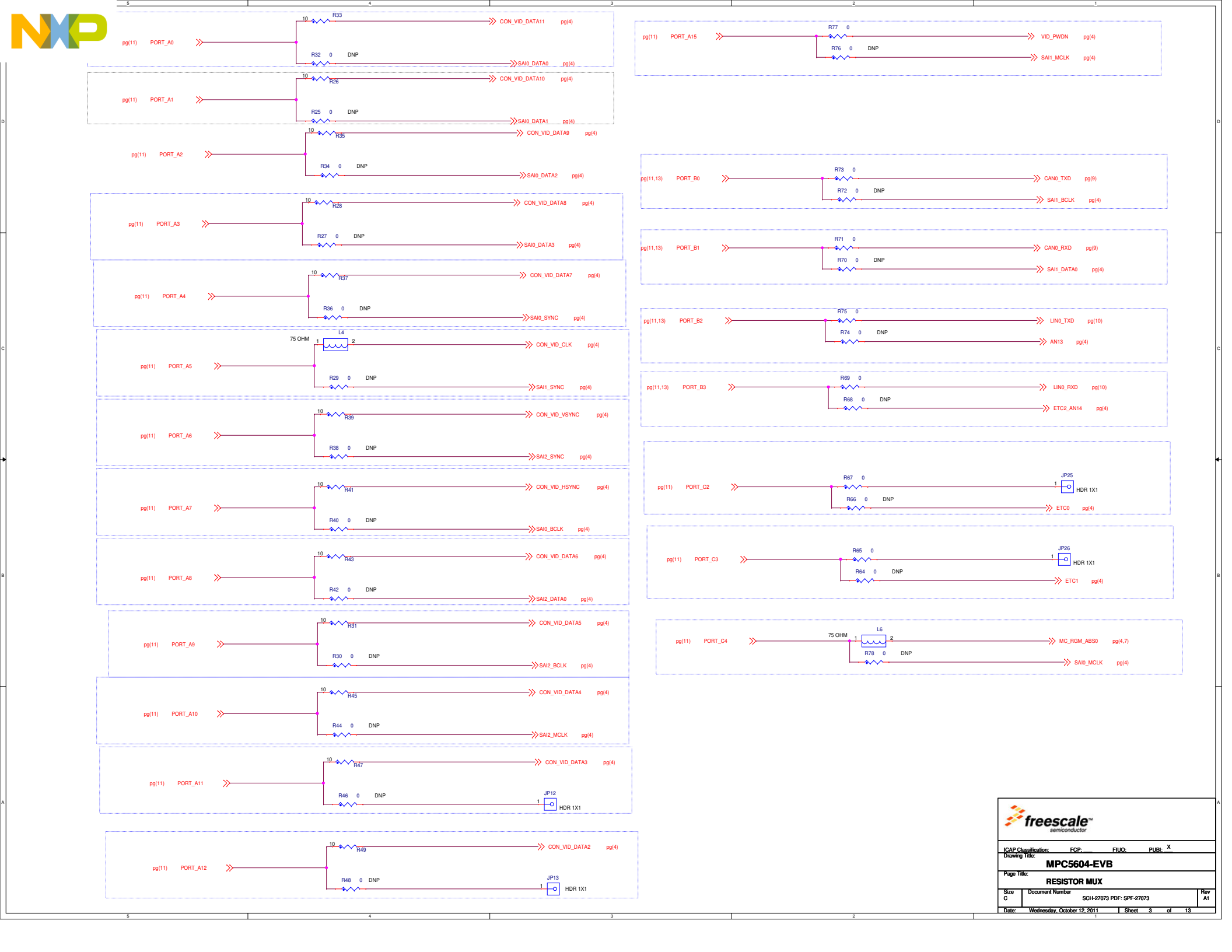
pg(11) PORT_A0
10 R33 CON_VID_DATA11 pg(4)
R32 0 DNP SAI0_DATA0 pg(4)
pg(11) PORT_A1
10 R26 CON_VID_DATA10 pg(4)
R25 0 DNP SAI0_DATA1 pg(4)
pg(11) PORT_A2
10 R35 CON_VID_DATA9 pg(4)
R34 0 DNP SAI0_DATA2 pg(4)
pg(11) PORT_A3
10 R28 CON_VID_DATA8 pg(4)
R27 0 DNP SAI0_DATA3 pg(4)
pg(11) PORT_A4
10 R37 CON_VID_DATA7 pg(4)
R36 0 DNP SAI0_SYNC pg(4)
pg(11) PORT_A5
75 OHM L4 CON_VID_CLK pg(4)
R29 0 DNP SAI1_SYNC pg(4)
pg(11) PORT_A6
10 R39 CON_VID_VSYNC pg(4)
R38 0 DNP SAI2_SYNC pg(4)
pg(11) PORT_A7
10 R41 CON_VID_HSYNC pg(4)
R40 0 DNP SAI0_BCLK pg(4)
pg(11) PORT_A8
10 R43 CON_VID_DATA6 pg(4)
R42 0 DNP SAI2_DATA0 pg(4)
pg(11) PORT_A9
10 R31 CON_VID_DATA5 pg(4)
R30 0 DNP SAI2_BCLK pg(4)
pg(11) PORT_A10
10 R45 CON_VID_DATA4 pg(4)
R44 0 DNP SAI2_MCLK pg(4)
pg(11) PORT_A11
10 R47 CON_VID_DATA3 pg(4)
R46 0 DNP JP12 HDR 1X1
pg(11) PORT_A12
10 R49 CON_VID_DATA2 pg(4)
R48 0 DNP JP13 HDR 1X1
pg(11) PORT_A15
R77 0 VID_PWDN pg(4)
R76 0 DNP SAI1_MCLK pg(4)
pg(11,13) PORT_B0
R73 0 CAN0_TXD pg(9)
R72 0 DNP SAI1_BCLK pg(4)
pg(11,13) PORT_B1
R71 0 CAN0_RXD pg(9)
R70 0 DNP SAI1_DATA0 pg(4)
pg(11,13) PORT_B2
R75 0 LIN0_TXD pg(10)
R74 0 DNP AN13 pg(4)
pg(11,13) PORT_B3
R69 0 LIN0_RXD pg(10)
R68 0 DNP ETC2_AN14 pg(4)
pg(11) PORT_C2
R67 0 JP25 HDR 1X1
R66 0 DNP ETC0 pg(4)
pg(11) PORT_C3
R65 0 JP26 HDR 1X1
R64 0 DNP ETC1 pg(4)
pg(11) PORT_C4
75 OHM L6 MC_RGM_ABS0 pg(4,7)
R78 0 DNP SAI0_MCLK pg(4)
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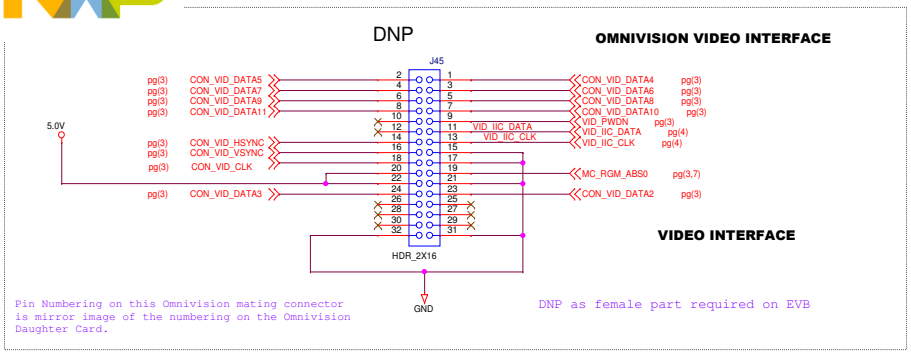

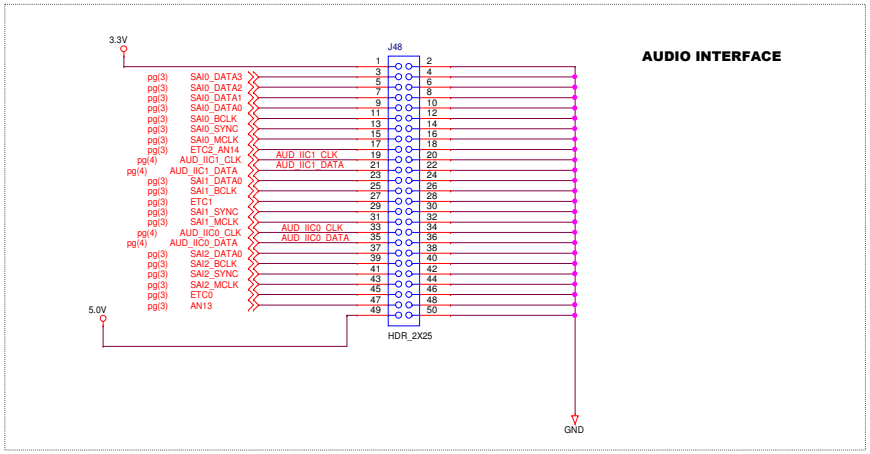

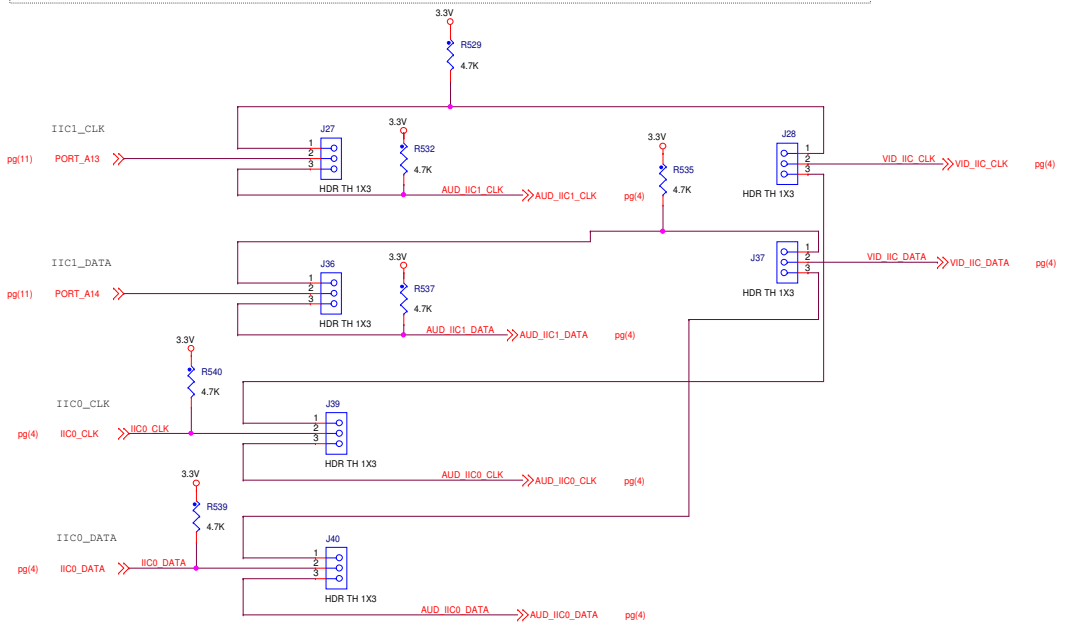

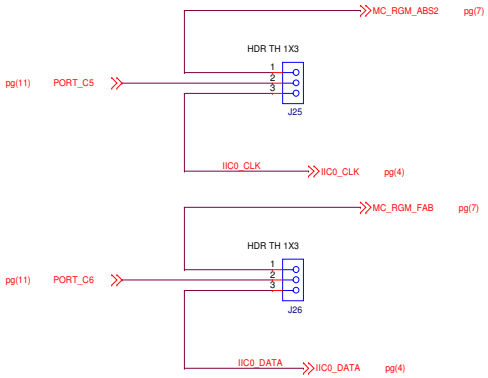

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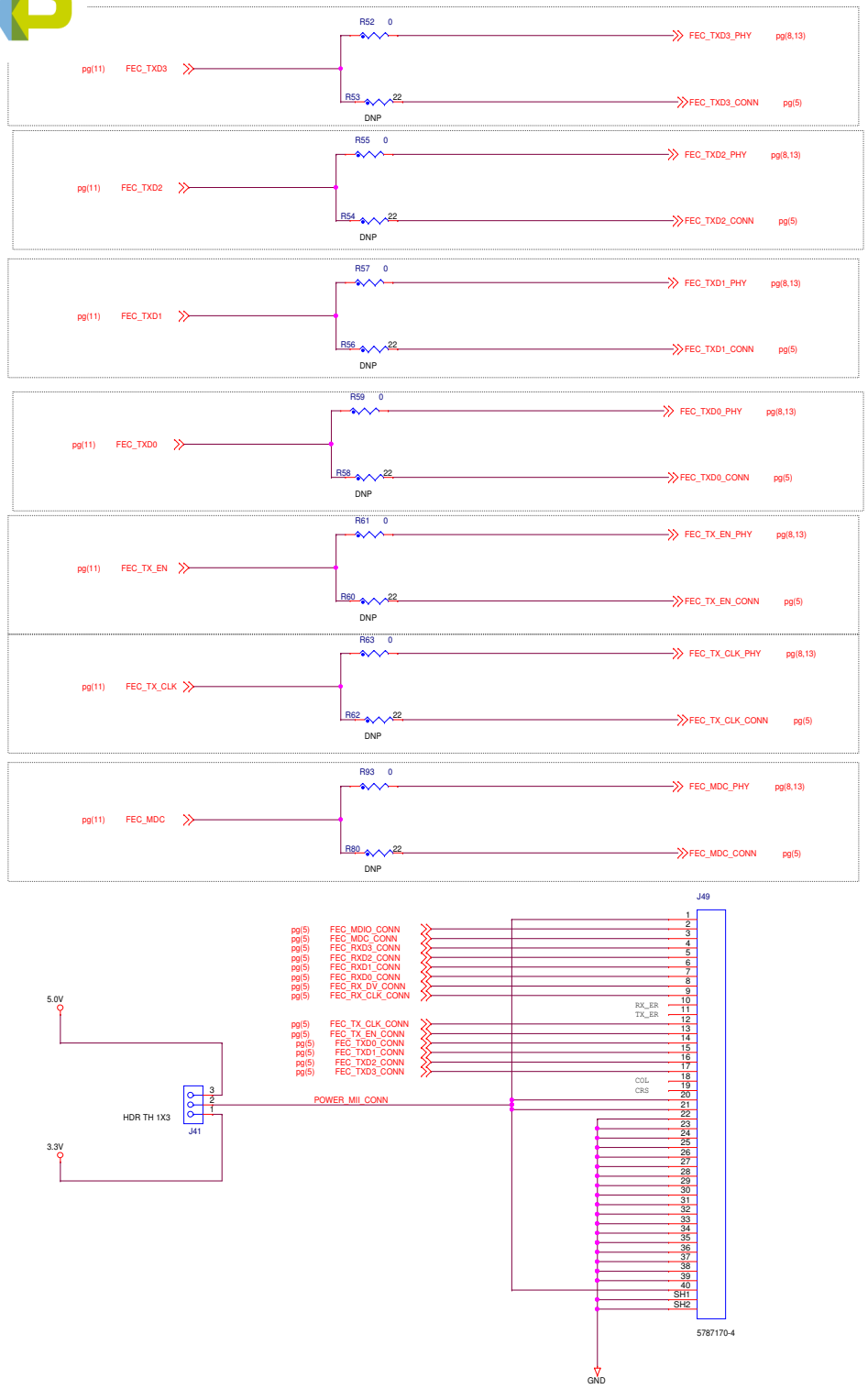

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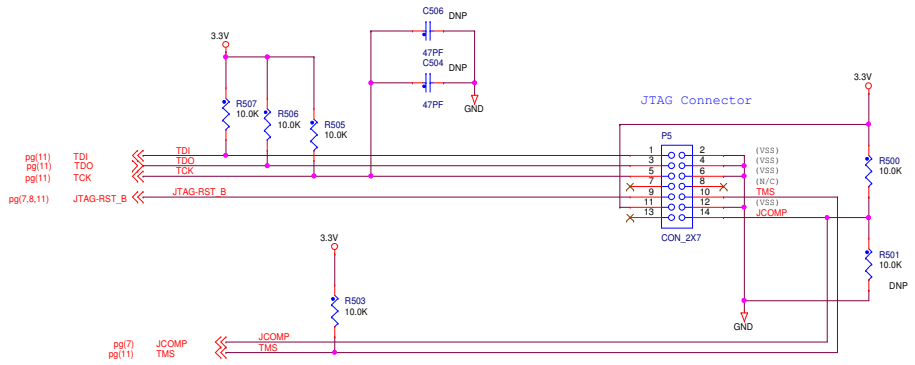
JTAG INTERFACE

Place CAPS as close to connector pins as possible but do NOT fit caps at board assembly.



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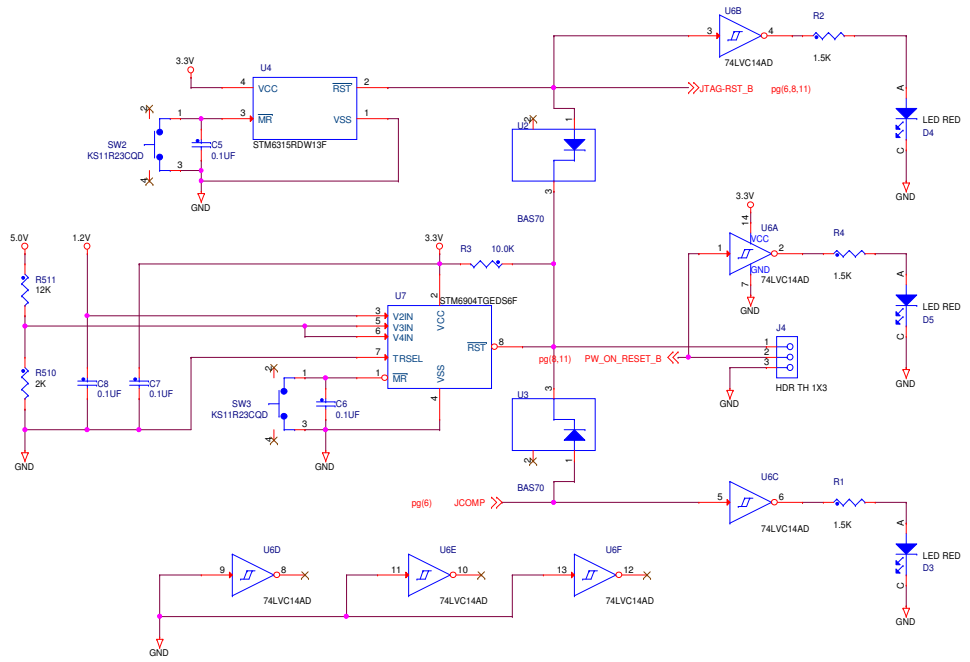
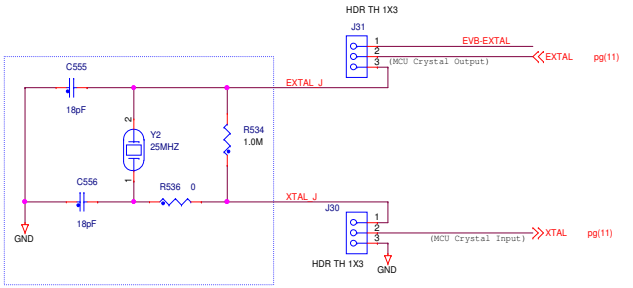
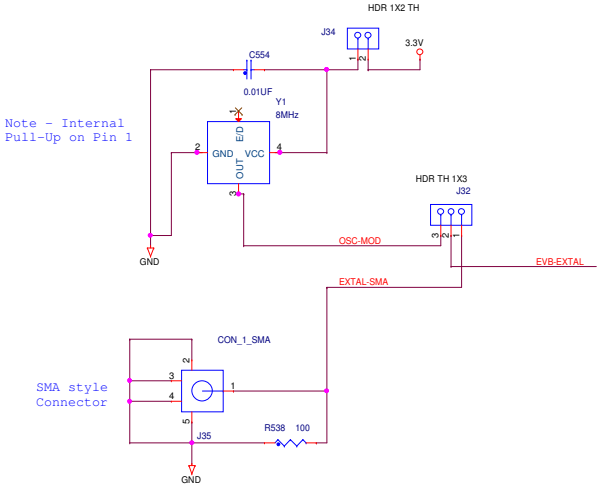
REMOVE XTAL jumper when driving EXTAL from
Oscillator Module or External Source

Power On Reset



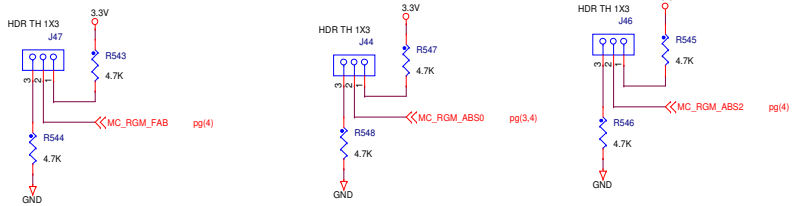
Clock Circuit





STRAIGHT SMA CONNECTOR ,PLACE NEAR TO SOC

Boot Config



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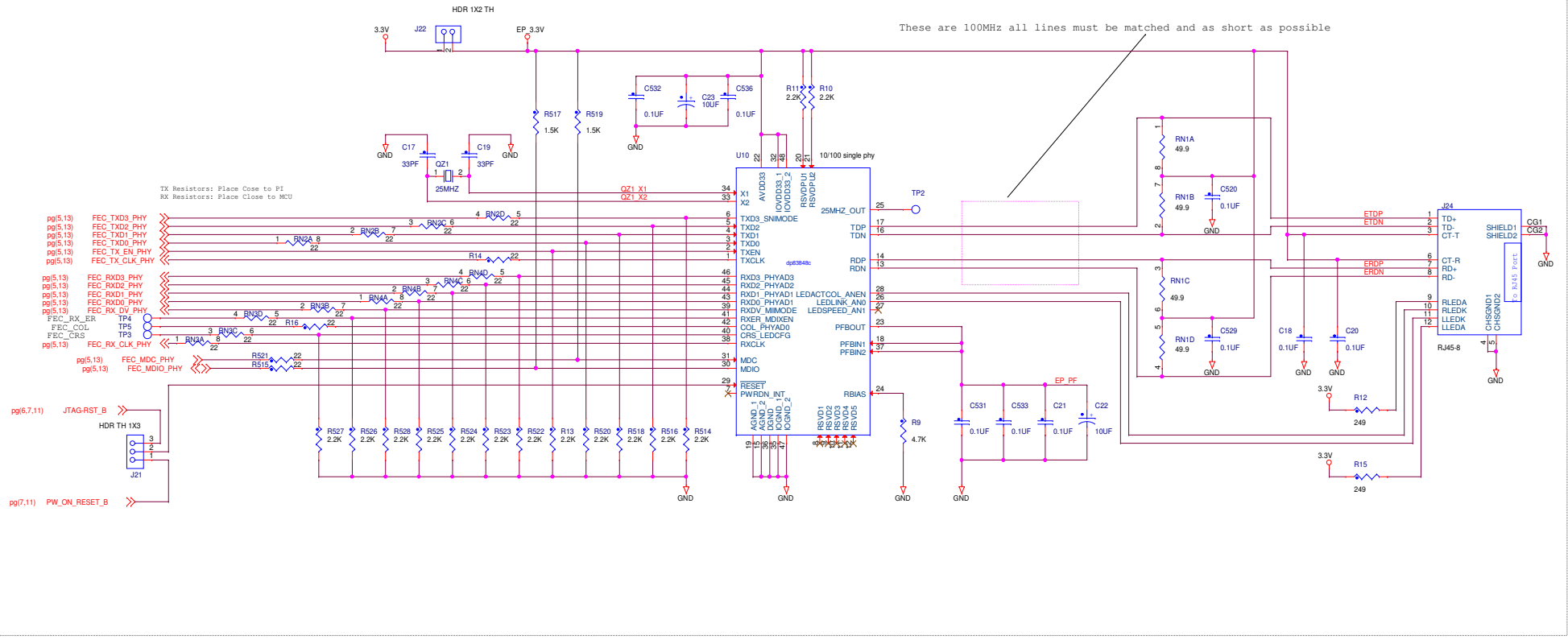
Ethernet Section



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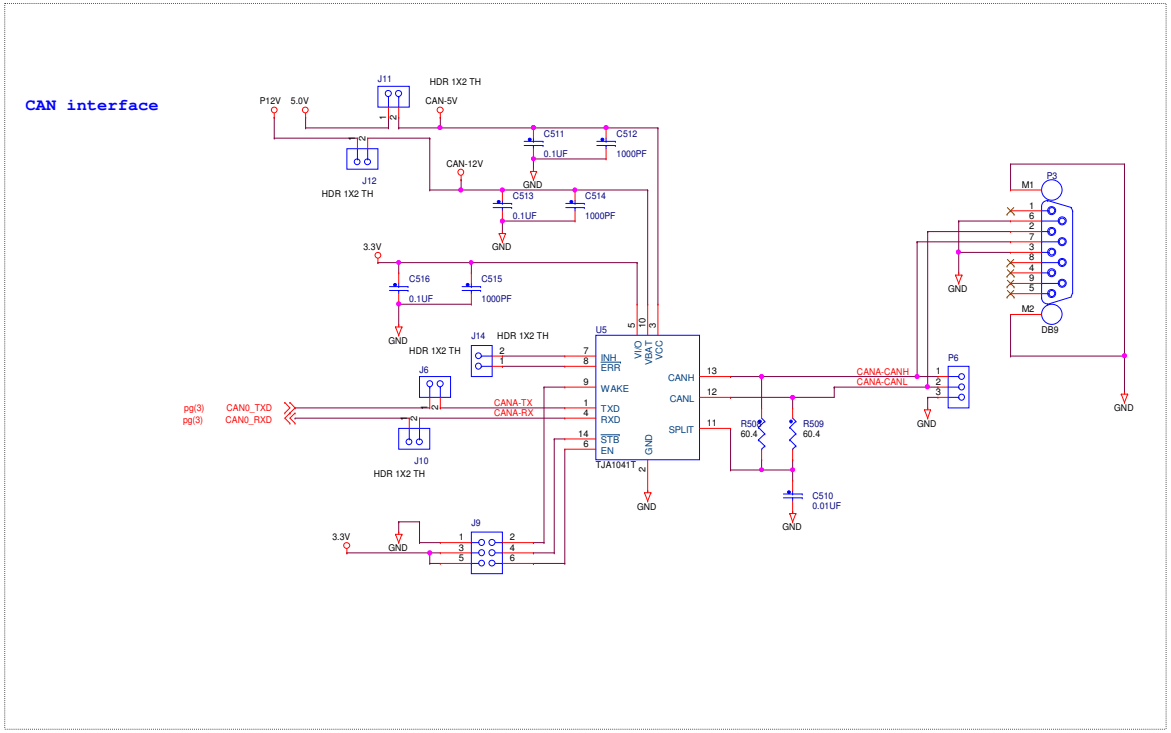
CAN interface



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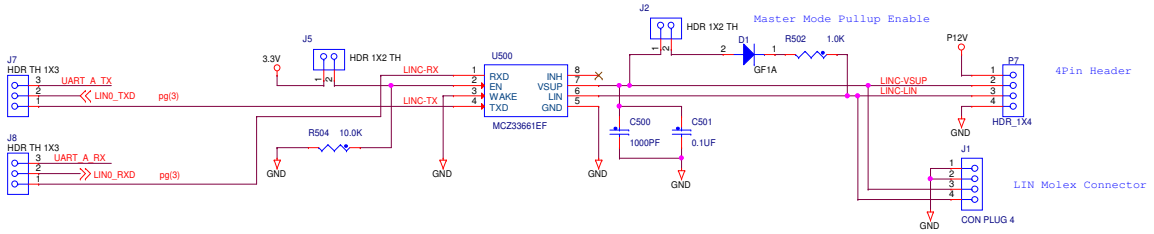
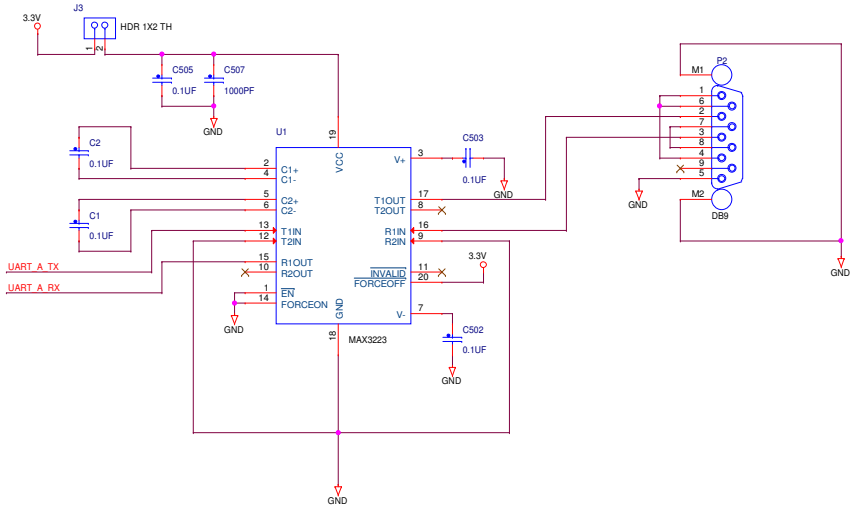
LIN Interface



SCI Interface



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Page Title: **LIN & SCI PHYSICAL INTERFACE**

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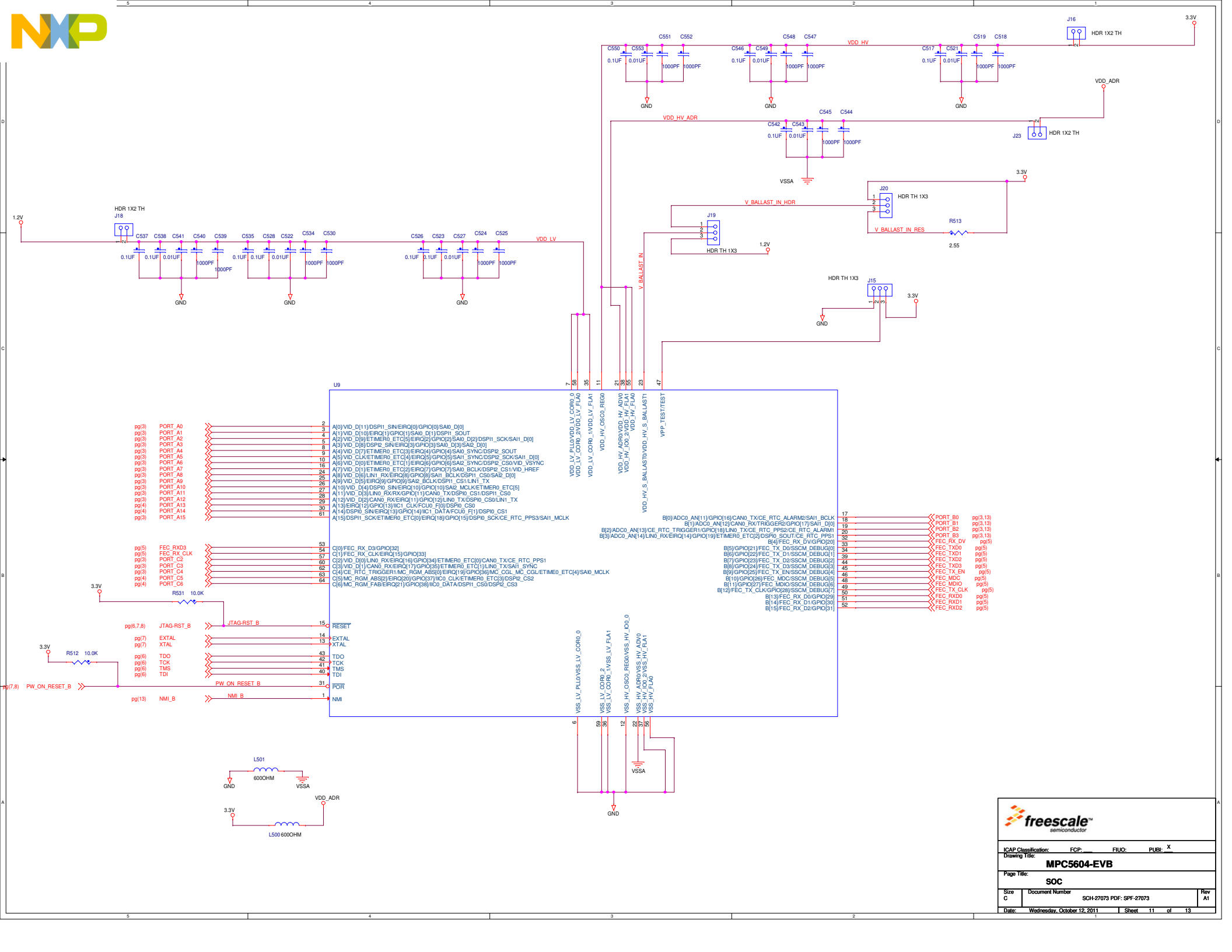

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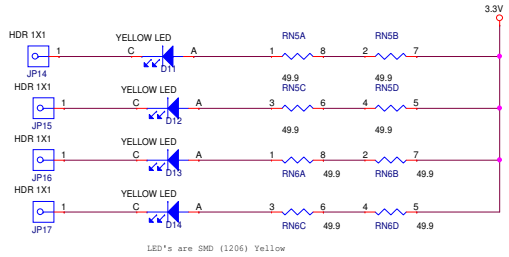
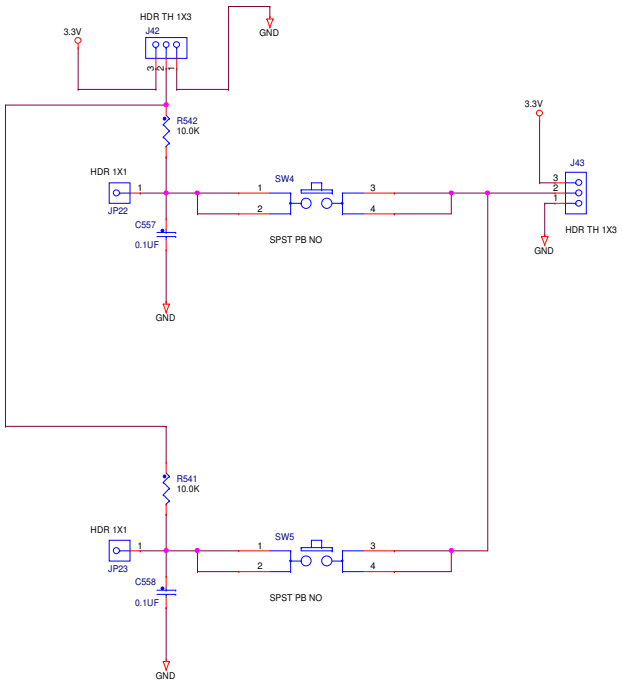
User LED's



User switches



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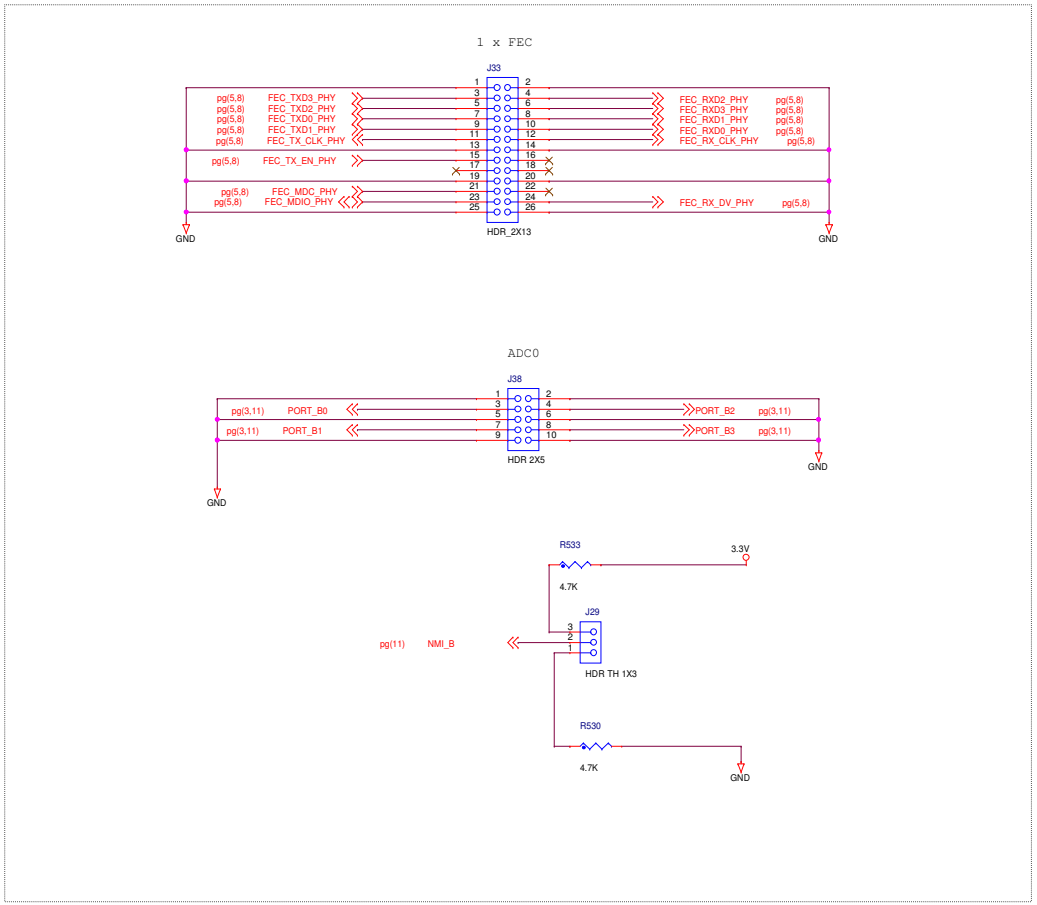

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USER I/O CONNECTORS

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