

Errata to MPC8548E Configurable Development System Reference Manual, Rev. 2

This errata describes corrections to the *MPC8548E Configurable Development System Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.

Changes

2.5, 2-8 In Table 2-1, replace the row for SW3, CCB clock PLL, bits 5, 6, 7, and 8 with the following:

3	5	CCB clock PLL	0	0000 16:1 (default)
	6		0	0010 2:1
	7		0	0011 3:1
	8		0	0100 4:1
				0101 5:1
				0110 6:1
				1000 8:1
				1001 9:1
				1010 10:1
				1100 12:1
				Rest Reserved

2.5, 2-8 Table 2-1, add the following note to the end of the table:

Note: To operate the primary PCI bus at 66 MHz several switch settings are required:
 SW3 on MPC8548CDC card should be set as SW3[5:8] = 1000 (CCB clock: system clock = 8:1) and the Arcadia X3.n should be set as SW3[3:4] = 01.
 If the Arcadia is Rev. X3.0, then SW3[1] must be set as SW3[1] = 1.

2.5, 2-12 In Table 2-3, replace the row for SW3, bit 5 with the following:

3	5	RTK8139 Ethernet enable ENET_DIS*	1	0 RealTek 8139 cannot be accessed 1 RealTek 8139 may be accessed
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4.9, 4-11 Table 4-9, replace the row for CCB Clock PLL[0:3] with the following:

CCB Clock PLL[0:3]	Section 4.9.1	LA[28:31]	Switch/I2C	0x18	4:1	SW3(5:8)	0000 = 16X
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Appendix H, H-7 On page 253, update schematic such that the AVDD for core is connected to an 180-Ω resistor, and the AVDD for platform is connected to a 150-Ω resistor..

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