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WPR1516 Product Brief

Supports all MWPR1516 devices

Contents

1 WPR1516 sub-family introduction

WPR1516 family and reference design extends Freescale's wireless power portfolio to support higher charging power. It satisfies the larger form factor smart phone and tablet like applications for faster charging. It supports 15 W following WPC (wireless power consortium) MPWG (medium power working group) specification, and reserve the capability to support future other standards. With necessary integration, it saves PCB form factor, while leaves the possibility for applications to do thermal design based on application requirement.

WPR1516 is a ARM® Cortex® M0+ core ASSP with Freescale's UHV technology. It includes FSKDT and CNC models which allows easy development for bi-directional communication architecture between transmitter and receiver. PGA (programmable gain amplifier) model handles small signal which ease the solution for FOD (foreign object detection). USB/Adaptor switcher sets the priority between wired and wireless charging. Offering QFN and WLCSP package provides alternative options for both industrial and consumer applications with easy manufacturing or saving PCB space.

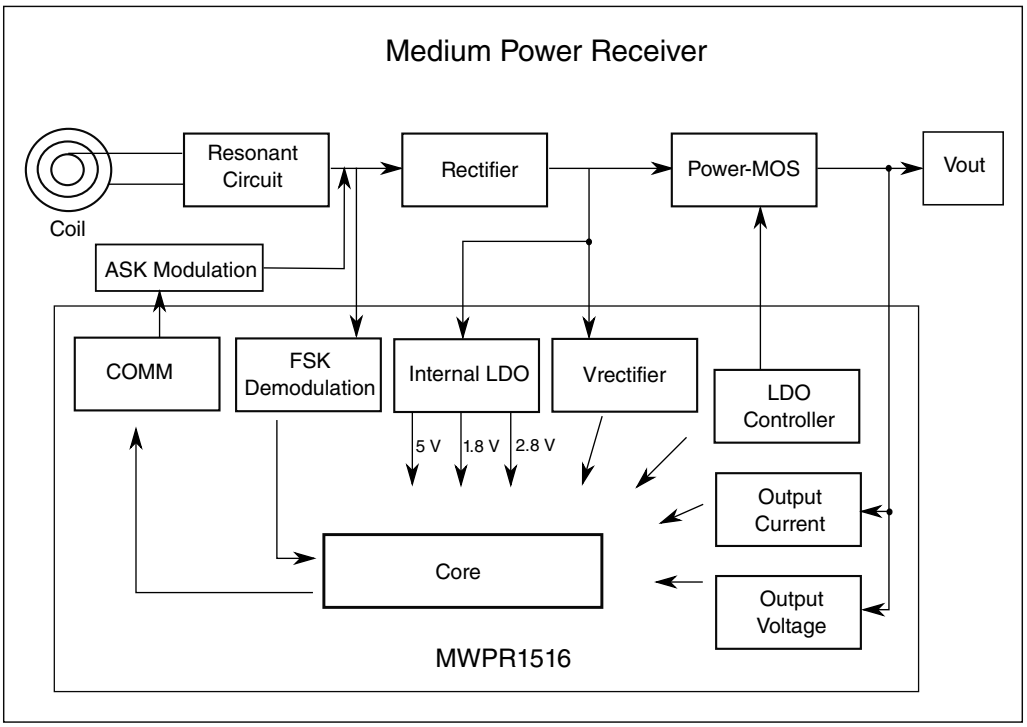

Figure 1. Receive system block diagram

2 WPR1516 sub-family features

WPR1516 sub-family has the following features:

- Operating conditions
  - Voltage range: 3.5 V to 20 V
  - Temperature range: -40 to 85 °C
- Packages
  - 36-pin WLCSP 3.1x3.0 mm 0.6mm pitch
  - 32-pin QFN 5x5mm 0.58 mm pitch
- Core
  - ARM CM0+ at 24 MHz
  - NVIC controller
- Memories
  - 16 KB program flash memory
  - 4 KB SRAM
- Clocks
  - 32 kHz or 4-24 MHz external crystal oscillator
  - 20 kHz internal low power oscillator
- Low power features
  - Run
  - Wait
  - Stop
- System peripherals
  - LDO controller
  - Communication and Clamp Controller (CNC)
- Analog
  - 1 x 12-bit ADC with total 12 channels

  - Analog comparator with internal 6-bit DAC
  - 1 x programmable gain amplifier (PGA) with differential input and output
- Communication interfaces
  - One UART
  - One I2C
- Timers
  - 2 x 2-channel FTMs with basic TPM function
  - 1 x 2-channel PIT
  - 1 x FSK demodulation timer (FSKDT)
  - 1 x RTC
- Human machine interface
  - Up to 13 GPIOs
- Security and integrity modules
  - 80- bit unique ID per chip

3 Block diagram

The following figure shows the WPR1516 block diagram.

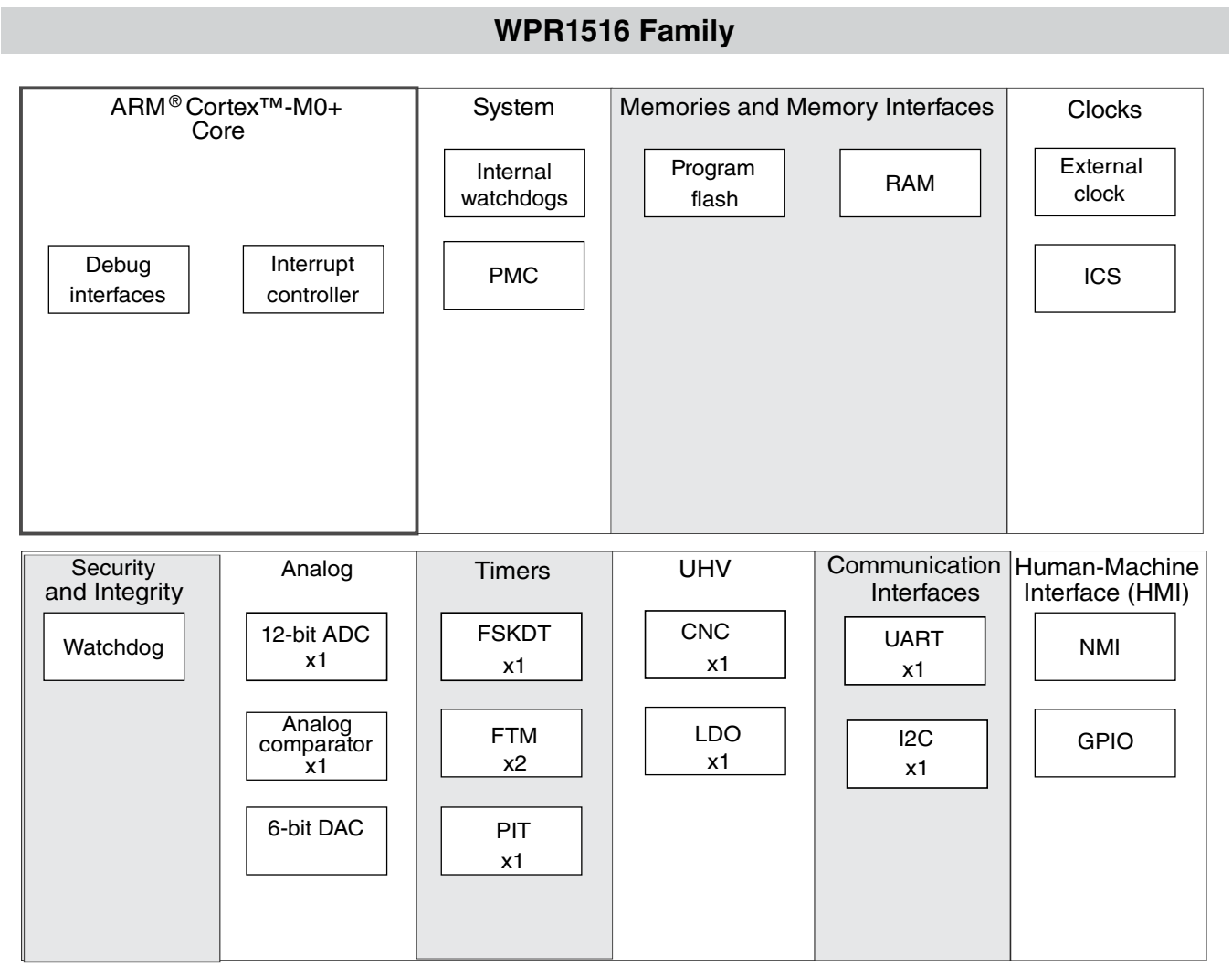

Figure 2. WPR1516 block diagram

4 Features

4.1 High level feature comparison

The following table shows the high level feature of WPR1516.

Table 1. WPR1516 high level features

Sub-family	WPR1516
CPU frequency	24 MHz
Flash memory	16 KB
SRAM	4 KB
PGA	Yes
ADC	12-bit
CNC	Yes
FSKDT	Yes

4.2 Common feature

Table 2. WPR1516 common features

Core/System modules			Timers Modules	
Core	CM0+		FSKDT	1
CPU Frequency	24 MHz		FTM	2x2-ch
DMA	–		PIT	1
Bit Manipulation Engine	–		Communication interface	
Debug	SWD		Low Power UART	–
Trace	–		UART	1
Memories			8-bit SPI	–
Flash	16 KB		I2C	1
SRAM	4 KB		I2S	–
ROM	–		USB Slave FS	–
Regfile	–		USB Vreg	–
Clock Modules			Human Machine Interface	
External clock	DC to 24 MHz		Segment LCD	–
ICS	31.25 - 39.063 kHz		NMI	Yes
RTC	–		Total GPIOs	13
Embedded USB Clock Generator	–		GPIOs w/ Interrupt	–
Security and Integrity			High Current GPIOs	–

Table continues on the next page...

Table 2. WPR1516 common features (continued)

Watchdog	Yes		Operating Characteristics	
Analog Modules			Voltage Range	3.5 V - 20 V
ADC	1x12-bit ADC		Flash Write Voltage	3.5 V
Analog Comparator	1		Temperature range	-40 to 85 ˚C

4.3 Features difference per package

Table 3. Features difference per package

Package	32-pin QFN	36-pin WLCSP
Flash	16 KB	16 KB
SRAM	4 KB	4 KB
CNC	Yes	Yes
Total GPIOs	13	13

4.4 Power modes

The following table shows the power modes of WPR1516.

Table 4. WPR1516 power modes

Power mode	Description	Core mode	Recovery
Run	Allows maximum performance of chip. Default mode out of reset; on-chip voltage regulator is on.	Run	–
Wait	Allows peripherals to function while the core is in Sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Stop	Places chip in static state. Lowest power mode that retains all registers. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Deep sleep	Reset/Interrupt

4.5 Module-by-module feature list

4.5.1 Core modules

4.5.1.1 ARM Cortex M0+ Core

- Up to 24 MHz core frequency from 3.5 V to 20 V across temperature range of –40 °C to 85 °C
- Support up to 32 interrupt request sources

- 2-stage pipeline micro-architecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiply

4.5.1.2 Nested Vectored Interrupt Controller (NVIC)

Following are the features of the NVIC module.

- Up to 32 interrupt sources
- Includes a single non-maskable interrupt

4.5.1.3 Wake-up Interrupt Controller (WIC)

The features of the WIC module are given below.

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

4.5.1.4 Debug controller

- 2-pin serial wire debug (SWD) provides external debugger interface

4.6 System module

4.6.1 Power management controller (PMC)

Features of PMC module include:

- Four integrated voltage regulators: $VREG_{VDDX}$, $VREG_{VDDF}$, $VREG_{VDD}$ and $VREG_{VREFH}$
  - 5 volt ($VREG_{VDDX}$ for analog modules)
  - 2.8 volt ($VREG_{VDDF}$ for flash memory and oscillator)
  - 1.8 volt ($VREG_{VDD}$ for digital logics)
  - 3.7~4.9 volt output with 6-bit trim ($VREG_{VREFH}$ for ADC voltage reference)
  - Output supply decoupling capacitors of 4.7~10 µF for $VREG_{VDDX}$ and 10 µF for $VREG_{VREFH}$ required
  - No output supply decoupling capacitors for $VREG_{VDDF}$ and $VREG_{VDD}$ required
  - Reduced performance mode (RPM), full performance mode (FPM), and wake-up from the RPM state via external input
- Integrated power-on reset (POR)
- Low voltage detection system
  - Integrated low voltage reset (LVR) with reset capability in $VREG_{VDDX}$, $VREG_{VDDF}$ and $VREG_{VDD}$
  - Integrated low voltage warning (LVW) indicator in $VREG_{VDDX}$
  - Programmable LVW indicator for VREFH in $VREG_{VREFH}$
- Buffered high-accuracy reference voltage output
  - Factory programmed trim for high-accuracy reference

- 20 kHz low-power oscillator (LPO) clock source
- Integrated temperature sensor allowing both internal and external monitoring

4.6.2 Watchdog timer (WDOG)

Features of the WDOG module include:

- Configurable clock source inputs independent from the:
    - bus clock
    - Internal 32 kHz RC oscillator
    - Internal 20 kHz RC oscillator
    - External clock source
- Programmable timeout period
    - Programmable 16-bit timeout value
    - Optional fixed 256 clock prescaler when longer timeout periods are needed
- Robust write sequence for counter refresh
    - Refresh sequence of writing 0x02A6 and then 0x80B4 within 16 bus clocks
- Window mode option for the refresh mechanism
    - Programmable 16-bit window value
    - Provides robust check that program flow is faster than expected
    - Early refresh attempts trigger a reset.
- Optional timeout interrupt to allow post-processing diagnostics
    - Interrupt request to CPU with interrupt vector for an interrupt service routine (ISR)
    - Forced reset occurs 128 bus clocks after the interrupt vector fetch.
- Configuration bits are write-once-after-reset to ensure watchdog configuration cannot be mistakenly altered.
- Robust write sequence for unlocking write-once configuration bits
    - Unlock sequence of writing 0x20C5 and then 0x28D9 within 16 bus clocks for allowing updates to write-once configuration bits
    - Software must make updates within 128 bus clocks after unlocking and before WDOG closing unlock window.

4.6.3 System clocks

The following clock sources can be used as system clocks.

- External crystal oscillator or resonator
    - Low range: 31.25–39.0625 kHz
    - High range: 4–24 MHz
- Internal clock references
    - 31.25 to 39.0625 kHz oscillator
    - 20 kHz LPO oscillator
- External square wave input clock
- Frequency-locked loop (FLL) range: 40–50 MHz

4.7 Memories and memory interfaces

4.7.1 On-chip memory

24 MHz performance devices

- Up to 16 KB flash memory
- Up to 4 KB SRAM

4.8 Analog

4.8.1 Analog-to-digital converter (ADC)

Features of ADC module include:

- Programmer's model with list based architecture for conversion command and result value organization
- Selectable resolution of 8-bit, 10-bit, or 12-bit
- Channel select control for n external analog input channels
- Provides up to eight device internal channels
- Programmable sample time
- A sample buffer amplifier for channel sampling (improved performance in view to influence of channel input path resistance versus conversion accuracy)
- Left/right justified result data
- Individual selectable VRH_0/1 and VRL_0/1 inputs on a conversion command basis
- Special conversions for selected VRH_0/1, VRL_0/1, (VRL_0/1 + VRH_0/1) / 2
- 15 conversion interrupts with flexible interrupt organization per conversion result
- One dedicated interrupt for "End Of List" type commands
- Command sequence list (CSL) with a maximum number of 64 command entries
- Provides conversion sequence abort
- Restart from top of active command sequence list (CSL)
- The command sequence list and result value list are implemented in double buffered manner (two lists in parallel for each function)
- Conversion command (CSL) loading possible from system RAM or NVM
- Single conversion flow control register with software selectable access path
- Two conversion flow control modes optimized to different application use cases

4.8.2 Analog comparator (ACMP)

Features of ACMP module include:

- Operational over the whole supply range of 2.7 V to 5.5 V
- On-chip 6-bit resolution DAC with selectable reference voltage from V_{DD} or internal VREFH
- Configurable hysteresis
- Selectable interrupt on rising edge, falling edge, or both rising or falling edges of comparator output
- Selectable inversion on comparator output
- Up to four selectable comparator inputs

4.8.3 Programmable gain amplifier (PGA)

Features of PGA module include:

- Programmable gain: ×8, ×10, ×15 or ×20
- Differential inputs from two inputs across the external current sensing resistor
- Differential outputs to two ADC input channels
- Input offset voltage can be calibrated by software

4.9 Ultra high voltage

4.9.1 Communication and clamp controller (CNC)

Features of CNC module include:

- A wireless power Tx-to-Rx zero-crossing detection sub-module
  - Wireless power receiver coil voltage frequency detection from the pins AC1 and AC2, supporting up to 500 kHz AC input
  - Low jitter on AC1 and AC2 voltage zero-crossing comparator
  - Programmable glitch rejection
- Supports external wired power (for example, USB adaptor) plug-in
  - Supports 5 V input on the pin AD_IN
  - Switches on/off when valid wired power plugs in/out (could be set as off by default)
  - Over-voltage and low voltage protection on AD_IN
  - Programmable digital filter to make AD_IN status immune to glitches
- Rectified voltage monitor
  - Over-voltage and low voltage detection on VREC
  - Rectifier over-voltage clamp driver
  - Programmable digital filter to make VREC status immune to glitches

4.9.2 Linear low dropout voltage regulator controller (LDO)

Features of LDO module include:

- Input voltage: 4.6 V ~ 20 V(as maximum) from AC-DC rectifier
- Configurable output voltage: 4.2 V ~ 5.2 V
- Configurable loading current: 1 A ~ 3 A(as maximum)
- Configurable overvoltage protection and overcurrent protection
- High-accuracy 9-bit DACs for output voltage and current trimming
- Configurable charge pump voltage and pump voltage monitor

4.10 Timer

4.10.1 Flextimer module (FTM)

Features of FTM module include:

- FTM source clock is selectable
  - Source clock can be the system clock, the fixed frequency clock
  - Fixed frequency clock is an additional clock input to allow the selection of an on chip clock source other than the system clock
  - Selecting external clock connects FTM clock to a chip level input pin therefore allowing to synchronize the FTM counter with an off chip clock source
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- 16-bit counter
  - It can be a free-running counter or a counter with initial and final value
  - The counting can be up or up-down
- Each channel can be configured for input capture, output compare, or edge-aligned PWM mode
- In Input Capture mode:
  - The capture can occur on rising edges, falling edges or both edges
- In Output Compare mode the output signal can be set, cleared, or toggled on match
- All channels can be configured for center-aligned PWM mode
- The generation of an interrupt per channel
- The generation of an interrupt when the counter overflows
- Backwards compatible with TPM
- Testing of input captures for a stuck at zero and one conditions

4.10.2 Real-time counter (RTC)

Features of the RTC module include:

- 16-bit up-counter
  - 16-bit modulo match limit
  - Software controllable periodic interrupt on match
- Software selectable clock sources for input to prescaler with programmable 16 bit prescaler
  - OSC 32.768KHz nominal.
  - LPO (~20 kHz)
  - Bus clock
  - Internal reference clock (32 kHz)

4.10.3 Periodic Interrupt Timer (PIT)

Features of PIT module include:

- Ability of timers to generate trigger pulses
- Ability of timers to generate interrupts
- Maskable interrupts
- Independent timeout periods for each timer

4.10.4 Frequency-shift keying demodulation timer (FSKDT)

Features of FSKDT module include:

- One frequency-shift keyed signal input channel
- 16-bit free-running counter to count the input signal edge-to-edge period
- Three 16-bit phase counters
  - Each phase counter contains the period count accumulation of programmable consequence (4/8/16/32) cycles of the input signal.
  - Interrupt is generated when any individual phase counter is updated or all phase counters are updated.
  - Phase counter 0 is always updated by the latest period count accumulation. Previous period accumulations update phase counter 1 and phase counter 2.
- 16-bit current position number, which contains the input signal cycle number since the module is enabled or reset
- Input signal edge-to-edge period error detection
  - Programmable period-too-short error threshold
  - Programmable period-too-long error threshold
  - Interrupt generation when less than 11 bits (FSKDT_DATA[BM] = 0) or 8 bits (FSKDT_DATA[BM] = 1) are received with FSK parking at F_{op}.
- Module software reset
- Message bit-stream detection
  - Bit value (ZERO or ONE) recognition
  - Interrupt generation
- Message byte packing

4.11 Communication interfaces

4.11.1 Inter-integrated circuit (I2C)

Features of I2C module include:

- Compatible with *The I^2C-Bus Specification*
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection

- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Support for *System Management Bus (SMBus) Specification, version 2*
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support

4.11.2 Universal asynchronous receiver/transmitter (UART)

Features of UART module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable 1-bit or 2-bit stop bits
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

4.12 Human-machine interfaces

4.12.1 General-purpose input/output (GPIO)

Features of the GPIO module include:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register

NOTE

The GPIO module is clocked by system clock.

4.12.2 Interrupt (IRQ)

Features of the IRQ module include:

- A dedicated external interrupt pin IRQ
- IRQ Interrupt Control bits
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Internal pullup device

5 Part Identification

5.1 Format

Part numbers for this device have the following format:

Q WPR## FFF R T PP N

5.2 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
WPR##	WPR family	• WPR15
FFF	Program flash memory size	• 16 = 16 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• C = -40 to 85 °C
PP	Package identifier	• FM=32 QFN (5 mm x 5 mm) • AL=36 WLCSP (3.07 mm x 2.98 mm)
N	Packaging type	• R = Tape and reel • (Blank) = Trays

6 Order information

The following table summarizes the part numbers of the devices covered by this document.

Table 5. Orderable part numbers

MC partnumber	CPU frequency	Pin count	Package	Flash	SRAM
MWPR1516CFM(R)	24 MHz	32	QFN	16 KB	4 KB
MWPR1516CALR	24 MHz	36	WLCSP	16 KB	4 KB

7 Revision history

The following table provides a revision history for this document.

Table 6. Revision history

Rev. No.	Data	Substantial changes
1	12/2014	Initial publish

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