NXP Semiconductors

Product Brief

Document Number: 1

Rev. 2, 05/2022

Contents

1.	Software Product Overview	1
2.	Software Content	3
3.	Supported Targets	4
4.	Quality, Standards Compliance and Testing Approach	5
5.	References	5
6	Document Information	6

Structural Core Self-Test Library

1. Software Product Overview

The SCST (Structural Core Self-Test) Library is the software product used for the runtime detection of permanent HW faults in Arm® Cortex-A53 processor cores. It contains test software (atomic tests) that stimulates the processor core submodules with the predefined test vectors and observes and evaluates the core logic response. It typically achieves 90% DC (Diagnostic Coverage). It targets various MCU core submodules, like:

- Data Path units (ALU, Multiplier, Divider)
- Load/Store unit
- Instruction decoder
- Forwarding logic
- FPU & Neon

The details can be found in the Diagnostic Coverage Estimation document, which is a part of the delivery of each individual SCST product. Faults that are considered as safe (e.g. faults in the debugging logic)

Structural Core Self-Test Library, Product Brief, Rev. 2, 05/2022

are not tested and are excluded from the DC calculation, see Figure 1: NXP's SCST Library content.

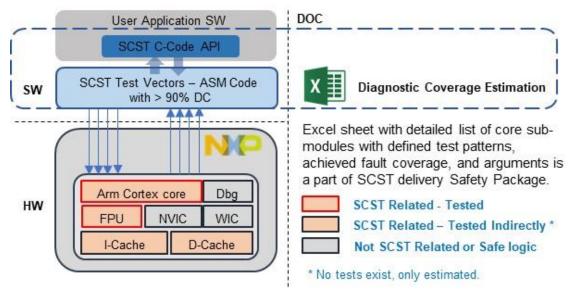


Figure 1. NXP's SCST Library Content Example

The SCST Library can be used to detect single-point faults or latent faults, see [1] for the fault differentiation. In both cases SCST detect permanent faults only and it is primarily intended for processors which do not use HW techniques supporting safety in terms of permanent fault detection, e.g. delayed-lockstep. If SCST is used to detect latent faults, then it is sufficient to run it only during start-up or shut-down. To detect single-point faults, SCST needs to be executed periodically in runtime.

SCST Diagnostic Coverage is estimated analytically. The RTL-code of the core submodules together with Arm[®] Architecture Manual is examined in detail by the developer. An expert individually analyses the core submodules, defines the test patterns, and analytically estimates DC.

SCST is developed as Safety Element out of Context (SEooC) [1]. The highest ASIL assigned to the SCST safety requirements is ASIL B(D) supporting the achievement of safety goals up to ASIL D, however in the case when SCST is used to detect single-point faults, SCST diagnostic coverage is sufficient only for ASIL B. Hence, SCST can be used to support ASIL B(D) requirements and other runtime measures shall be in place to detect the remaining single-point faults to achieve ASIL C and ASIL D metrics.

2. Software Content

The SCST Library is essential in supporting applications to achieve safety. The main components of the SCST Library are as follows:

- SCST Library source code:
 - Is written in assembly language.
 - o Is divided into dedicated atomic tests targeting specific parts of the core.
 - o Provides reaction to a detected fault (destroys test signature).
- Simple API written in C:
 - Provides flexible atomic tests execution.
 - o Signals first detected fault to the user application.
 - Provides support for atomic test fault injection by destroying test signature to allow to the user application testing its own fault reaction mechanisms.
 - o Conforms with MISRA C standard.
- Fault Coverage Estimation document which:
 - o Contains detailed argumentation for the claimed DC estimation.

Supported Targets

3. Supported Targets

The SCST Library described in this product brief is available for NXP S32G device' Arm[®] Cortex-A53 core.

4. Quality, Standards Compliance and Testing Approach

The Cortex-A53 SCST Library software product was developed according to the NXP Software Development Processes that is ISO 26262, Automotive-SPICE, IATF 16949 and ISO 9001 compliant.

5. References

1. ISO 26262-1:2018. Road vehicles - Functional safety - Part 1:Vocabulary, 2018, {ISO 26262-1:2018(E)}.

Document Information

6. Document Information

Table 1. Revision History

Revision number	Date	Substantive changes
1	03/2022	Initial version
2	05/2022	Fixed core and platform description

How to Reach Us:

Home Page:

nxp.com

Web Support: nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C 5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorlQ, QorlQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and µVision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

 $\ensuremath{\mathbb{C}}$ 2022 NXP B.V.

Document Number: 1 Rev. 2

05/2022