56F8123

Target Applications

- > Polyphase metering
- > UPS
- > Electric vehicles
- > Currency validation
- > Industrial control/ networking
- > Home appliances
- > Smart sensors
- > Fire and security systems
- > Medical monitoring

Overview

Freescale Semiconductor's 56F8123 extends the capabilities introduced by the 56F8122 by adding additional analog-to-digital converter (ADC) inputs and timer input/output pins, among other enhancements. This device also features 40 MIPS (at 40 MHz) performance and 40 KB of on-chip Flash memory, and a comprehensive assortment of sophisticated peripherals, all in a 64-pin LQFP package. The 56F8123 is perfectly suited for applications requiring the computational power of a signal processor and the knack for "bit banging" of an embedded controller. The 56F8123 can operate at extended temperatures (up to +105°C) without losing a step. In other words, you now have at your disposal the performance and functionality demanded by an application that may be used in a harsh environment.

COP/Watchdog	Program Memory	Power Management
Relaxation Oscillator	32 KB Flash	
		(2) SPI
PLL	8 KB Boot Flash	(2) SCI
Up to 27 GPIO	56800E Core 40 MIPS 40 MHz 64 LQFP	JTAG/EOnCE
(8) 16-bit Timer		
		8-ch., 12-bit ADC
	Data Memory	
	8 KB RAM	

56800E Core Features

- > Up to 40 MIPS at a guaranteed 40 MHz core frequency
- > DSP and microcontroller (MCU) functionality in a unified, C-efficient architecture
- > JTAG/enhanced on-chip emulation (EOnCE™) for unobtrusive, real-time debugging
- > Four 36-bit accumulators
- > 16- and 32-bit bidirectional barrel shifter
- > Parallel instruction set with unique addressing modes
- > Hardware DO and REP loops available
- > Three internal address buses
- > Four internal data buses
- > Architectural support for 8-, 16- and 32-bit single-cycle data fetches
- > MCU-style software stack support
- > Controller-style addressing modes and instructions
- > Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)
- > Proven to deliver more control functionality with a smaller memory footprint than competing architectures

Benefits

- > Hybrid architecture facilitates implementation of both control and signal processing functions in a single device
- > High-performance, secured Flash memory eliminates the need for external storage devices
- > Extended temperature range up to +105°C allows for operation of nonvolatile memory in industrial applications
- > Flash memory emulation of EEPROM eliminates the need for external nonvolatile memory
- > 32-bit performance with 16-bit code density
- > On-chip voltage regulator and power management reduce overall system cost
- > Internal relaxation oscillator eliminates the need for an external crystal
- > This device boots directly from Flash, providing additional application flexibility
- > ADC modules are tightly coupled to reduce processing overhead
- > Low-voltage interrupts (LVIs) protect the system from brownout or power failure
- > Simple in-application Flash memory programming via EOnCE or serial communication





Memory Features

- > Architecture permits as many as three simultaneous accesses to program and data memory
- > On-chip memory includes high-speed volatile and nonvolatile components
 - 32 KB of Program Flash
 - 8 KB of Data RAM
 - 8 KB of Boot Flash
- > All memories operate at 40 MHz (zero wait states) over temperature range (-40°C to +105°C), with no software tricks or hardware accelerators required
- > Flash security feature prevents unauthorized accesses to its content

56F8123 Peripheral Circuit Features

- > Two serial peripheral interfaces (SPIs)
- > Two serial communications interfaces (SCIs)
- > Eight 16-bit timers with input and output compare capability
- > On-chip 3.3V to 2.6V voltage regulator
- > Software-programmable Phase-Lock Loop (PLL)
- > On-chip relaxation oscillator
- > 12-bit ADCs with eight inputs, self-calibration and current injection capability
- > Up to 27 general-purpose input/output (GPIO) pins
- > External reset input pin for hardware reset
- > Computer operating properly (COP)
- > Integrated power-on reset and LVI module
- > I2C communications master mode (emulated)

Product Documentation

56F8300 Peripherals Manual

Detailed peripheral description of the 56F8300 family of devices

Order Number: MC56F8300UM

56F8323/ 56F8123 Technical Data Sheet

Electrical and timing specifications, device-specific peripheral information and package and pin descriptions

Order Number: MC56F8323

56F8123 **Product Brief** Summary description and block diagram of the core, memory, peripherals and interfaces Order Number: MC56F8123PB

DSP56800E Reference Manual

Detailed description of the DSP56800E architecture, 16-bit core processor and the

instruction set Order Number: DSP56800ERM

Award-Winning Development Environment

- > Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- > The CodeWarrior™ Integrated Development Environment is a sophisticated tool for code navigation, compiling and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, CodeWarrior tools and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

Ordering Information

Part MC56F8123 Package Type Low-Profile Quad Flat Pack (LQFP) Pin Count **Temperature Range** -40°C to +105°C **Order Number** MC56F8123VFB

Learn More: For more information about Freescale products, please visit www.freescale.com.

