Signal Controllers

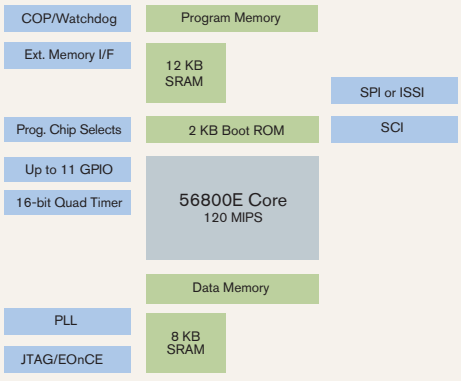
56852

Target Applications

- > Full duplex feature phones
- > Voice-activated toys
- > Voice recognition and command
- > Musical effects equipment
- > Karaoke systems
- > Voice and audio processing
- > General-purpose applications
- > Automotive hands-free

Overview

The first device in the 56800E family, the 56852, sets a new price per performance standard, offering 120 MIPS below US$3 at high volume. The 56852 integrates 12 KB of program SRAM and 8 KB of data SRAM, a quad timer module with two external outputs, a serial peripheral interface (SPI) multiplexed with an improved synchronous serial interface (ISSI) and a serial communications interface (SCI)/universal asynchronous receiver/ transmitter (UART). With 20 KB on-chip SRAM and multiple serial peripherals in an 81-pin MAPBGA package, the 56852 can be integrated easily into a previously designed system where a DSP coprocessor is needed and system board real estate is at a premium. However, with up to 4 MB program or up to 12 MB of data addressing space for off-chip memory, the 56852 is also a powerful stand-alone processor ideal for telephony applications, speech processing and recognition, embedded modems, audio processing—such as 3-D virtualization, and other digital effects, echo cancellation, magnetic and smart card readers and feature phones.



The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and microcontroller (MCU) applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

56800E Core Features	Benefits
> Efficient 16-bit digital signal controller engine with dual Harvard architecture	> 120 MIPs at under US$3 in high volume
> 120 MIPS at 120 MHz core frequency	> Hybrid MCU/DSP architecture removes need for separate MCU in many cases
> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)	> Large linear address spaces, up to 4 MB program and data, supporting complex communications stacks
> Four 36-bit accumulators, including extension bits	> Available in a space saving 81-pin MAPBGA package
> 16-bit bidirectional shifter	> Supported by Metrowerks CodeWarrior™ Integrated Development Environment, allowing rapid application development in C
> Parallel instruction set with unique addressing modes	> Nonintrusive debug via JTAG/on-chip emulation (OnCE™) port
> Hardware DO and REP loops	> Processor Expert™ technology rapid application design (RAD) tool available, including algorithms and drivers
> Three internal address buses and one external address bus	
> Four internal data buses and one external data bus	
> Instruction set supports both DSP and controller functions	
> Four hardware interrupt levels	
> Five software interrupt levels	
> Controller-style addressing modes and instructions for compact code	
> Efficient C compiler and local variable support	
> Software subroutine and interrupt stack with depth limited only by memory	
> JTAG/enhanced on-chip emulation (EOnCE™) debug programming interface	

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Energy Information

> Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs

> Wait and stop modes available

56852 16-bit Digital Signal Processors

> 120 MIPS at 120 MHz

> 12 KB Program SRAM

> 8 KB Data SRAM

> 2 KB Boot ROM

> Access up to 4 MB of program memory or up to 12 MB of data memory

> One SPI or one ISSI

> One SCI

> Interrupt controller

> General-purpose 16-bit quad timer

> JTAG/EOnCE for unobtrusive, real-time debugging

> Computer operating properly (COP)/watchdog timer

> 81-pin MAPBGA package

> Up to 11 general-purpose input/output (GPIO) pins

56852 Memory Features

> Harvard architecture permits as many as three simultaneous accesses to program and data memory

> On-chip memory:

- 12 KB Program SRAM
- 8 KB Data SRAM
- 2 KB Boot ROM

> Off-chip memory expansion

> Access up to 4 MB of program memory or up to 12 MB data memory

> Chip select logic for glueless interface to ROM and SRAM

56852 Peripheral Circuit Features

> General-purpose 16-bit quad timer with two external pins*

> One SCI*

> One SPI or one ISSI module*

> Interrupt controller

> Computer operating properly (COP)/watchdog timer

> JTAG/EOnCE for unobtrusive, real-time debugging

> 81-pin MAPBGA package

> Up to 11 GPIO pins

*Each peripheral I/O can be used alternately as a GPIO.

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

DSP56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit DSP core processor and the instruction set ***Order Number:*** DSP56800ERM
DSP56852 User's Manual	Detailed description of memory, peripherals and interfaces of the 56852 ***Order Number:*** DSP56852UM
DSP56852 Technical Data Sheet	Electrical and timing specifications, pin descriptions and package descriptions ***Order Number:*** DSP56852
DSP56852 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces ***Order Number:*** DSP56852PB

Ordering Information

Part	DSP56852
Supply Voltage	1.8V, 3.3V
Package Type	Mold Array Plastic Ball Grid Array (MBGA)
Pin Count	81
Frequency (MHz)	120
Order Number	DSP56852VF120

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