Mask Set Errata for Mask 0N72D

Introduction

This report applies to mask 0N72D for these products:

- MPC567XK

Errata ID	Errata Title
3866	ADC Self Test algorithm S0 result can be incorrect at low temperature
5008	PMC: Potential stuck in reset condition if certain pins are pulled up too hard during power up.

e3866: ADC Self Test algorithm S0 result can be incorrect at low temperature

Errata type: Errata

Description: The ADC Self Test algorithm S step 0 (S0) measures ADC Vbandgap / VDD_HV_ADR. In the case where the S0 step occurs after the ADC has sampled and converted a value close to VDD_HV_ADR at low temperature (for example -40C) in some process corners the sampling time (specified by INPSAMP_S) of 80h is not long enough to allow the correct ADC sampling capacitor settling. This may lead to an incorrect converted value.

The Band Gap in the above specified condition is slow in discharging the sampling capacitor when the previous sampled voltage is much larger than the Band Gap output voltage (nominally 1.2V). The larger the voltage sampled before S0, the slower is the settling.

This issue can also affect S1 algorithm results since S1 = VDD_HV_ADV / Vbandgap.

Workaround: To eliminate the problem it is mandatory to:

(a) increase the sampling time for S supply self test (INSAMP_S) from 80h to FFh and

(b) insert a sacrificial ADC conversion immediately before the S supply self test.

The user software must insert a single-shot S algorithm Step 0 conversion (also called sacrificial S0 conversion) before the normal S supply self test to achieve accurate sample capacitor settling. The user software must prohibit any other conversions between the sacrificial S0 conversion and normal S0 conversion of the S supply self test.

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e5008: PMC: Potential stuck in reset condition if certain pins are pulled up too hard during power up.

Errata type: Errata

Description: If the below identified pins are pulled high either with a direct short or with too small a resistance during power up, a stuck in reset condition can occur due to a failure to deassert internal LVDs on the 3.3V rail or the 1.2V rail. This affects both internal and external regulation modes of the PMC. There is no issue if the pins are no connects/floating or pulled low with any resistor value.

The pins affected are:

Pin 1: ETIMER1_ETC5/SIUL_GPIO78/SIUL_EIRQ26 (Y15 for 473 BGA, P13 for 257 BGA)

Pin 2: ETIMER1_ETC3/SIUL_GPIO92/CTU1_EXT_IN/MC_RGM_FAB/SIUL_EIRQ30 (Y11 for 473 BGA, P8 for 257 BGA)

Pin 3: ETIMER1_ETC4/SIUL_GPIO93/CTU1_EXT_TGR/SIUL_EIRQ31 (Y16 for 473 BGA, P12 for 257 BGA)

Workaround: 1. If pins 1 or 3 need to be pulled high during power up, a 20 K ohm resistor or greater must be installed between each pin and the voltage source.

2. If the serial boot option is needed :

a) If entering during power up, a 20 K ohm 1% resistor must be installed between Pin 2 (the MC_RGM_FAB pin) and the voltage source and the ambient temperature is between -40C and 80C.

b) If entering after reset deassertion, the following sequence can be used from -40C to 125C.

i. Power up device with Pin 2 (MC_RGM_FAB pin) low.

ii. Verify device is out of reset.

iii. Pull FAB pin up to Vih level. This will be achieved with a resistance value less than 18 K ohm.

iv. Assert and deassert RESET_B either through a hardware induced pin toggle or a software induced destructive or functional reset using the ME module.

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