Mask Set Erratafor Mask0M87Y

Introduction

This report applies to mask 0M87Y for these products:

- MPC5644B
- MPC5644C
- MPC5645B
- MPC5645C
- MPC5646B
- MPC5646C

Prior ID	Current ID	Erratum Title
	e4168	ADC: "Abort switch" aborts the ongoing injected channel as well as the upcoming normal channel
	e4186	ADC: triggering an ABORT or ABORTCHAIN before the conversion starts
e10594	e3441	CGM : Default clock source for PLL is FIRC
e10128	e3462	CSE : Serial boot mode is non operational when CSE is used in sequential mode
e9984	e3446	CTU : The CTU (Cross Trigger Unit) CLR_FLAG in EVTCFGR register does not function as expected
e9998	e3439	DEBUG : Incorrect Pin PL[12] behavior when debugger is connected.
e10128	e3463	DEBUG : The debugger cannot connect to the device under certain circumstances when the CSE is used in sequential mode.
	e3449	DEBUG: Device may hang due to external or 'functional' reset while using debug handshaking mechanism
	e3556	DMA_MUX : Low Power Entry may not be completed when peripherals run on divided clock with DMA enabled mode
	e3697	e200z: Exceptions generated on speculative prefetch
e10637	e3512	ECSM: ECSM_PFEDR displays incorrect endianness
e9494	e3447	FLASH : PAD_3V5V[1:0] polarity and bit position in NVUSR0 register is incorrect.
	e3452	FLASH: Programming just after reading a location of Data Flash with double ECC error can trigger a functional reset.
e10521	e3444	FlexCAN : CAN1RXD not available on PA[0]

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Prior ID	Current ID	Erratum Title
e33503	e2421	FLEXRAY : Message Buffer can not be disabled in POC state INTEGRATION_LISTEN
	e4340	LINFlexD: Buffer overrun can not be detected in UART Rx FIFO mode
e10107	e3466	LINFlexD: Register bus aborts are not generated on illegal accesses to reserved addresses within the register address space of LINFlexD
	e4758	LPM: High VDD STOP Mode Current
e10616	e3450	MC_ME : Checkstop Exception occurs during short reset assertion if Flash is Powered Down in current mode.
	e3570	MC_ME: Possibility of Machine Check on Low-Power Mode Exit
e10491	e3574	MC_RGM: A non-monotonic ramp on the VDD_HV/BV supply can cause the RGM module to clear all flags in the DES register
e9040	e3476	MC_RGM: Clearing a flag at RGM_DES or RGM_FES register may be prevented by a reset
e10256	e3438	Nexus Debug : Simultaneous Nexus trace on both e200z0 and e200z4 cores is not possible when the e200z0 core is running at half the e200z4 clock frequency
e10128	e3464	STCU : Software Watchdog Timer (SWT) can assert a reset before CSE sequential boot process completes.
e10336	e3465	STCU SSCM : CER Bit set in SSCM when MBIST is disabled, but has valid MBIST configuration in Test/Shadow
	e4146	When an ADC conversion is injected, the aborted channel is not restored under certain conditions
e10777	e3448	WKPU : NLOCK and NDSS bit value in NCR register in wakeup unit reverts to reset state at STANDBY exit.
e9044	e3440	WKPU : PB[8],PB[9],PB[10],PD[0],PD[1] pins configuration during standby
e10565	e3469	XBAR : Instruction Performance Degradation
e10566	e3470	XBAR : Performance Degradation in 1:1 mode

Revision	Changes
25AUG2011	Initial revision

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Revision	Changes
13JUN2012	The following errata were removed. • e3407 • e2656 • e3442 • e3436 • e3469 • e3470 The following errata were added. • e4168 • e4186 • e4146 • e4758 • e4340 • e3323 The following errata were revised. • e3697 • e3570 • e3512 • e3441
2	The following errata were removed. • e3323 The following errata were added. • e3469 • e3470

e4186: ADC: triggering an ABORT or ABORTCHAIN before the conversion starts

Description: When ABORTCHAIN is programmed and an injected chain conversion is programmed afterwards, the injected chain is aborted, but neither JECH is set, nor ABORTCHAIN is reset. In case a CTU conversion is demanded, the CTU conversion is aborted by the ADC digital logic but the CTU awaits ADC analogue acknowledgement that never arrives, stopping all CTU operation until next reset.

When ABORT is programmed and normal/injected chain conversion comes afterwards, the ABORT bit is reset and chain conversion runs without a channel abort.

If ABORT, or ABORTCHAIN, feature is programmed after the start of the chain conversion, it works properly.

Workaround: Do not program ABORT/ABORTCHAIN before starting the execution of the chain conversion.

If the CTU is being used in trigger mode, there will always be a small vulnerable window preventing reliably reading the ADC status and using ADC.MCR[ABORT] or ADC.MCR[ABORTCHAIN]. If these functions are required, disable all CTU triggers to that ADC first and do not start the CTU if the ABORT or ABORTCHAIN flags have been set whilst the ADC was IDLE. If the CTU cannot be disabled, an optimised ABORT should be implemented in software that de-configures further channel conversions using the ADC.NMCRx registers before waiting for ADC.MSR[NSTART] == 0. At this point, the ADC should be IDLE and the NMCRx registers can be reinstated for next use.

e3441: CGM : Default clock source for PLL is FIRC

Description: In the reference manual, the configuration for the SELCTL field within the CGM_AC0_SC register is detailed as follows:

0x0000 = FXOSC (default)

0x0001 = FIRC

On cut1 devices, this is reversed such that:

0x0000 = FIRC (default)

0x0001 = FXOSC

This is of particular importance when migrating between Cut1 and Cut2 silicon as a code change will be required to ensure the correct clock source is selected.

Workaround: Ensure that the correct PLL clock source is selected by programming the SELCTL fields as above.

e3462: CSE : Serial boot mode is non operational when CSE is used in sequential mode

Description: Serial boot mode (Force Alternate Boot mode = 1) will not function and the debugger will not be able to connect to the device when all of the conditions below are met:

1. CSE_RUN_MODE has been selected to be sequential (i.e. a valid DCF record exists in shadow flash to make CSE_RUN_MODE be sequential)

2. The Software Watchdog Timer (SWT) is enabled out of reset (via NVUSRO WATCHDOG_EN bit)

Reset will be asserted each SWT period. This state is recoverable by setting FAB=0.

Workaround: Do not use the serial boot mode when CSE_RUN_MODE is sequential.

e3446: CTU : The CTU (Cross Trigger Unit) CLR_FLAG in EVTCFGR register does not function as expected

Description: If the CTU CLR_FLG is set and the CTU is idle, a PIT triggered request to the CTU does not result in the correct ADC channel number being latched. The previous ADC channel number is latched instead of the requested channel number.

Workaround: There is no software workaround to allow the CLR_FLAG functionality to operate correctly. Do not program the CLR_FLAG bit to ‘1’.

e3439: DEBUG : Incorrect Pin PL[12] behavior when debugger is connected.

Description: When a debugger is connected (JTAG or Nexus), GPIO functionality is not available on pin PL[12]. Instead, PL[12] is assigned to EVTO functionality.

Workaround: Do not attempt to use PL[12] when a debugger is connected.

e3463: DEBUG : The debugger cannot connect to the device under certain circumstances when the CSE is used in sequential mode.

Description: It will be impossible for the debugger to connect to the device if all of the following conditions are met:

1. CSE_RUN_MODE has been selected to be sequential (i.e. a valid DCF record exists in shadow flash to make CSE_RUN_MODE= sequential)

2. The Software Watchdog Timer (SWT) is enabled out of reset (via NVUSRO WATCHDOG_EN bit)

3. The code flash is erased (i.e. no start address and length values are present for the CSE Secure Boot Process)

In this situation, the device will be permanently and irrevocably stuck in an infinite loop with reset being asserted each SWT period.

Workaround: 1. Set NVUSRO WATCHDOG_EN bit=0.

or

2. Don’t use Sequential mode; use Parallel mode instead (this is the default unless a valid DCF record is programmed).

Note: Users of sequential mode should be aware that this condition can be reached in development cycles where the flash is being erased. To avoid this condition developers must change the DCF record so that CSE_RUN_MODE is parallel prior to any flash erase/reset event. After flashing and a reset, the DCF record can be changed back to sequential mode, thus avoiding any issue.

e3449: DEBUG: Device may hang due to external or 'functional' reset while using debug handshaking mechanism

Description: If the low-power mode debug handshake has been enabled and an external reset or a ‘functional’ reset occurs while the device is in a low-power mode, the device will not exit reset.

Workaround: The NPC_PCR[LP_DBG_EN] bit must be cleared to ensure the correct reset sequence.

e3556: DMA_MUX : Low Power Entry may not be completed when peripherals run on divided clock with DMA enabled mode

Description: System may not enter into Low Power Mode (HALT/STOP/STANDBY) when all the below conditions are true simultaneously:

1.A Peripheral with DMA capability is programmed to work on divided clock.

2. Above peripheral is programmed to be stopped in Low Power Mode and active in RUN Mode.

3. Above Peripheral is active with DMA transfer while Software requests change to Low Power mode.

Workaround: Software should ensure that all the DMA enabled peripherals have completed their transfer before requesting Low Power mode Entry

e3697: e200z: Exceptions generated on speculative prefetch

Description: The e200z4 core can prefetch up to 2 cache lines (64 bytes total) beyond the current instruction execution point. If a bus error occurs when reading any of these prefetch locations, the machine check exception will be taken. For example, executing code within the last 64 bytes of a memory region such as internal SRAM or FLASH, may cause a bus error when the core prefetches past the end of memory. An ECC exception can occur if the core prefetches locations that are valid, but not yet initialized for ECC.

Workaround: Do not place code to be executed within the last 64 bytes of a memory region. When executing code from internal ECC SRAM, initialize memory beyond the end of the code until the next 32-byte aligned address and then an additional 64 bytes to ensure that prefetches cannot land in uninitialized SRAM.

e3512: ECSM: ECSM_PFEDR displays incorrect endianness

Description: The ECSM_PFEDR register reports ECC data using incorrect endiannes. For example, a flash location that contains the data 0xAABBCCDD would be reported as 0xDDCCBBAA at ECSM_PFEDR.

This 32-bit register contains the data associated with the faulting access of the last, properly-enabled flash ECC event. The register contains the data value taken directly from the data bus.

Workaround: Software must correct endianness.

e3447: FLASH : PAD_3V5V[1:0] polarity and bit position in NVUSR0 register is incorrect.

Description: In the reference manual, the polarity and affected power domain for the NVUSR0 PAD3V5V[0:1] bits do not match the implementation.

For PAD3V5V[0:1] a value of 1 means a 5V I/O supply and value of 0 means a 3.3V I/O supply.

PAD3V5V[0] refers to the VDD_HV_A domain and

PAD3V5V[1] refers to the VDD_HV_B domain.

Workaround: For controlling high voltage enable for I/O domain, program the NVUSR0 register as per description above.

e3452: FLASH: Programming just after reading a location of Data Flash with double ECC error can trigger a functional reset.

Description: If a double-bit ECC error is encountered when reading the data flash, a functional reset will occur if the next data flash access is a program (irrespective of the length of time between the data read causing the ECC error and the program attempt).

If another location in the data flash is read (which does not generate an ECC error) before attempting to program the data flash, the reset does not occur. This only impacts programming operations – an erase after a double-bit ECC error will not generate a reset.

Workaround: If a double-bit ECC error is encountered in the data flash, the application software must read another byte in the data flash without an ECC error prior to performing a program operation on the data flash. There is a read only data flash test flash block at address 0x00C0_2000 and the recommendation is to read data from this location to provide the “non ECC" data read. This procedure could be automated by adding the test block read to the exception handler for a data flash ECC event."

e3444: FlexCAN : CAN1RXD not available on PA[0]

Description: PA[0] does not have CAN1RX functionality on this revision of silicon.

Workaround: None

e2421: FLEXRAY : Message Buffer can not be disabled in POC state INTEGRATION_LISTEN

Description: If the communication controller is started as a non-coldstart node and configured and enabled message buffers in the POS config state for slot 1, then the message buffer can not be disabled in the INTEGRATION_LISTEN state, which is entered when no communication can be established.

Workaround: A Software work-around is available, which is as follows:

Run a freeze command just before running the message buffer disable for slot 1. This should enable the message buffer disable during the Listen States.

e4340: LINFlexD: Buffer overrun can not be detected in UART Rx FIFO mode

Description: When the LINFlexD is configured in UART Receive (Rx) FIFO mode, the Buffer Overrun Flag (BOF) bit of the UART Mode Status Register (UARTSR) register is cleared in the subsequent clock cycle after being asserted.

User software can not poll the BOF to detect an overflow.

The LINFlexD Error Combined Interrupt can still be triggered by the buffer overrun. This interrupt is enabled by setting the Buffer Overrun Error Interrupt Enable (BOIE) bit in the LIN Interrupt enable register (LINIER). However, the BOF bit will be cleared when the interrupt routine is entered, preventing the user from identifying the source of error.

Workaround: Buffer overrun errors in UART FIFO mode can be detected by enabling only the Buffer Overrun Interrupt Enable (BOIE) in the LIN interrupt enable register (LINIER).

e3466: LINFlexD: Register bus aborts are not generated on illegal accesses to reserved addresses within the register address space of LINFlexD

Description: Register bus aborts are not generated on illegal accesses to reserved addresses within the register address space of LINFlexD. This is applicable to LINFlex modules supporting master-only mode.

Workaround: None

e4758: LPM: High VDD STOP Mode Current

Description: The STOP mode current is 5000µA (max, 25C) compared to the targets in the Data Sheet specification of 1200µA for general parts.

Workaround: Lower limit devices with the target current are available as special parts. Please contact a sales representative for details.

e3570: MC_ME: Possibility of Machine Check on Low-Power Mode Exit

Description: When executing from the flash and entering a Low-Power Mode (LPM) where the flash is in low-power or power-down mode, 2-4 clock cycles exist at the beginning of the RUNx to LPM transition during which a wakeup or interrupt will generate a checkstop due to the flash not being available on RUNx mode re-entry. This will cause either a checkstop reset or machine check interrupt.

Workaround: If the application must avoid the reset, two workarounds are suggested:

1) Configure the application to handle the machine check interrupt in RAM dealing with the problem only if it occurs

2) Configure the MCU to avoid the machine check interrupt, executing the transition into low power modes in RAM

There is no absolute requirement to work around the possibility of a checkstop reset if the application can accept the reset, and associated delays, and continue. In this event, the WKPU.WISR will not indicate the channel that triggered the wakeup though the F_CHKSTOP flag will indicate that the reset has occurred. The F_CHKSTOP flag could still be caused by other error conditions so the startup strategy from this condition should be considered alongside any pre-existing strategy for recovering from an F_CHKSTOP condition.

e3574: MC_RGM: A non-monotonic ramp on the VDD_HV/BV supply can cause the RGM module to clear all flags in the DES register

Description: During power up, if there is non-monotonicity in power supply ramp with a voltage drop > 100mV due to external factors, such as battery cranking or weak board regulators, the SoC may show a no flag condition (F_POR==LVD12==LVD27==0).

Under these situations, it is recommended that customers use a workaround to detect a POR.

In all cases, initialization of the device will complete normally.

Workaround: The software workaround need only be applied when neither the F_POR, LVD27 nor LVD12 flag is set and involves checking SRAM contents and monitoring for ECC errors during this process. In all cases, an ECC error is assumed to signify a power-on reset (POR).

Three suggestions are made for software workarounds. In each case, if POR is detected all RAM should be initialized otherwise no power-on condition is detected and it is possible to initialize only needed parts of RAM while preserving required information.

Software workaround #1 :

An area of RAM can be reserved by the compiler into which a KEY, such as 0x3EC1_9678, is written. This area can be checked at boot and if the KEY is incorrect or an ECC error occurs, POR can be assumed and the KEY should be set. Use of a KEY increases detection rate to 31 bits(=<10e-9) or 23bits (= <5.10e-6) instead of 7-bit linked to ECC (=<10e-2)

Software workaround #2 :

When runtime data should be retained and RAM only fully re-initialized in the case of POR, a checksum should be calculated on the runtime data area after each data write. In the event of a reset where no flags are set, the checksum should be read and compared with one calculated across the data area. If reading the checksum and the runtime data area succeeds without an ECC error, and the checksums match, it is assumed than no POR occurred. The checksum could be a CRC, a CMAC or any other suitable hash.

Software workaround #3 :

Perform a read of memory space that is expected to be retained across an LVD reset. If there are no ECC errors, it can be assumed that an LVD reset occurred rather than a POR.

e3476: MC_RGM: Clearing a flag at RGM_DES or RGM_FES register may be prevented by a reset

Description: Clearing a flag at RGM_DES and RGM_FES registers requires two clock cycles because of a synchronization mechanism. As a consequence if a reset occurs while clearing is on-going the reset may interrupt the clearing mechanism leaving the flag set.

Note that this failed clearing has no impact on further flag clearing requests.

Workaround: No workaround for all reset sources except SW reset.

Note that in case the application requests a SW reset immediately after clearing a flag in RGM_xES the same issue may occur. To avoid this effect the application must ensure that flag clearing has completed by reading the RGM_xES register before the SW reset is requested.

e3438: Nexus Debug : Simultaneous Nexus trace on both e200z0 and e200z4 cores is not possible when the e200z0 core is running at half the e200z4 clock frequency

Description: Nexus Trace messages are not transmitted correctly when the e200z0 is working at half of the e200z4 frequency (CGM_Z0_DCR[DIV] bit is set)

Workaround: Do not configure the Nexus trace for the e200z0 when the CGM_Z0_DCR[DIV] bit is set.

e3464: STCU : Software Watchdog Timer (SWT) can assert a reset before CSE sequential boot process completes.

Description: The device will be stuck in a continual reset loop and debug cannot be established with the device if all of the following conditions are met:

1. CSE_RUN_MODE has been selected to be sequential (i.e. a valid DCF record exists in shadow flash to make CSE_RUN_MODE be sequential)

2. The Software Watchdog Timer (SWT) is enabled out of reset (via NVUSRO WATCHDOG_EN bit)

3. More than 16Kbytes have been selected to be authenticated by the CSE's Secure Boot Process.

Workaround: There are 3 possible workarounds that can be applied:

1. Set NVUSRO WATCHDOG_EN bit=0 to disable the SWT out of reset. The application code can then enable the SWT.

or

2. Authenticate less than 16Kbytes via the Secure Boot Process.

or

3. Don't use Sequential mode; use Parallel mode instead (this is the default unless a valid DCF record is programmed).

e3465: STCU SSCM : CER Bit set in SSCM when MBIST is disabled, but has valid MBIST configuration in Test/Shadow

Description: If the MBIST is disabled (NVUSRO.STCU_EN=1) and there is valid MBIST configuration information programmed into the shadow / test flash, the configuration error bit (CER) in the SSCM.STATUS register will be set.

Workaround: None

e4146: When an ADC conversion is injected, the aborted channel is not restored under certain conditions

Description: When triggered conversions interrupt the ADC, it is possible that the aborted conversion does not get restored to the ADC and is not converted during the chain. Vulnerable configurations are:

- Injected chain over a normal chain
- CTU trigger over a normal chain
- CTU trigger over an injected chain

When any of these triggers arrive whilst the ADC is in the conversion stage of the sample and conversion, the sample is discarded and is not restored. This means that the channel data register will not show the channel as being valid and the CEOCFRx field will not indicate a pending conversion. The sample that was aborted is lost.

When the trigger arrives during the final channel in a normal or injected chain, the same failure mode can cause two ECH/JECH interrupts to be raised.

If the trigger arrives during the sampling phase of the last channel in the chain, an ECH is triggered immediately, the trigger is processed and the channel is restored and after sampling/ conversion, a second ECH interrupt occurs.

In scan mode, the second ECH does not occur if the trigger arrives during the conversion phase. In one-shot mode, the trigger arriving during the conversion phase of the last channel restarts the whole conversion chain and the next ECH occurs at completion of that chain.

Workaround: It is suggested that the application check for valid data using the CDR status bits or the CEOCFRx registers to ensure all expected channels have converted. This can be tested by running a bitwise AND and an XOR with either the JCMRx or NCMRx registers and the CEOCFRx registers during the ECH of JECH handler. Any non-zero value for (xCMRx & (xCMRx $\oplus$ CEOCFRx)) indicates that a channel has been missed and conversion should be requested again.

Spurious ECH/JECH interrupts can be detected by checking the NSTART/JSTART flags in the ADC Module Status Registers – if the flag remains set during an ECH/JECH interrupt then another interrupt will follow after the restored channel or chain has been sampled and converted.

e3448: WKPU : NLOCK and NDSS bit value in NCR register in wakeup unit reverts to reset state at STANDBY exit.

Description: At STANDBY exit, NLOCK bit is reset to 0 and NDSS is reset to 2'b11.

This means that if the NMI configuration has previously been locked by setting the NLOCK bit, after STANDBY exit the configuration is returned to unlocked. The NMI source reverts to the default state of reserved

Workaround: Reprogram NLOCK and NDSS bits to required value at STANDBY exit.

e3440: WKPU : PB[8],PB[9],PB[10],PD[0],PD[1] pins configuration during standby

Description: Pins PB[8], PB[9], PB[10], PD[0] and PD[1] have both wake-up and analog functions on the pin.

As with all wakeup pins, to avoid excessive current consumption during STANDBY mode, these pins must be pulled either high or low (using the internal pull resistors or otherwise).

Workaround: When these pins are being used as an analogue input, you must ensure that during STANDBY, the analogue level applied on these pins is either lower than 0.2*VDD_HV or higher than 0.8*VDD_HV to prevent excessive current consumption.

e3469: XBAR : Instruction Performance Degradation

Description: The e200z0 core is connected to the crossbar via an interface gasket to convert between the 32-bit core and 64-bit crossbar busses. This gasket also contains a buffer to increase performance of sequential instruction fetches. This buffer is non functional resulting in non optimal performance.

The actual performance impact will vary with number of sequential accesses as well as the configuration of flash wait states and operating speed.

Workaround: None

e3470: XBAR : Performance Degradation in 1:1 mode

Description: The e200z0 core is connected to the crossbar via an interface gasket to convert between the 32-bit core and 64-bit crossbar busses. If the e200z0 operating frequency equals the system clock frequency (e200z0 clock divider in divide by 1 configuration), there is an additional 2 clock delay for every access.

Workaround: None

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Document Number: MPC5646B_0M87Y
Rev. 2