Mask Set Errata for Mask REVA

Introduction

This report applies to mask REVA for these products:

- MPC551X

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e4082: 32KOSC: 32 KHz Oscillator and PK1/AN15

Errata type: Errata

Description: Characterization of the 32 KHz OSC has revealed that it is not robust enough for the Automotive enviroment.

The 32 KHz OSC may not operate properly if the DC level on the EXTAL32 pin is pulled by leakage (either internal or external) in the positive direction. Note: putting a standard oscilloscope probe on this pin causes a negative leakage which can hide this issue.

Workaround: The 32 KHz OSC is only needed if an accurate Time of Day functionality is required in the application when using the RTC. The RTC can alternatively be clocked from the internal 32 KHz IRC or from the internal 16 MHz IRC. Do not use the 32 KHz OSC. There are no

functional or reliability issues if the 32 KHz OSC is not used. The 32 KHz OSC was intended to provide a clock source for the RTC and Low Power mode wake up input filtering. The RTC and wake up input filtering should be clocked from the internal 32 KHz IRC or from the 16 MHz IRC.

e1722: BAM: Serial download unavailable to last 16 bytes (4 words) of System RAM

Errata type: Information

Description: When using the BAM Serial boot download feature, the BAM initializes an additional 4 32-bit words after the end of the downloaded records. This is done to insure that if the core fetches the last instruction of the downloaded code from the internal SRAM while executing the code, it will not prefetch instructions from memory locations that have not been initialized.

Note: if the download image has the exact same size as the internal SRAM, the 20 bytes at the beginning of the SRAM will be written with zero value due to incomplete memory decoding.

Workaround: When using the Serial download feature of the BAM, make sure that the maximum address of the downloaded code does not exceed the end address of the SRAM minus 16 bytes or the last address of the Memory Management Unit (MMU) entry minus 16 bytes (for devices with MMU and the SRAM MMU setting less than the full SRAM size), whichever is smaller.

e1282: CRP: Spurious Pin Wakeup in Run Mode

Errata type: Errata

Description: During RUN mode, a CRP_PSCR[PWKSRCF] flag may be unintentionally set instead of the intention of only setting the wakeup flags during Sleep mode. The pin wakeup flags work fine during Sleep mode. There is not an issue when the pin wakeup flags are disabled. The flag may be set during flag configuration of CRP_WKSE[WKCLKSEL], CRP_WKPINSEL[WKPSELn], and CRP_WKSE[WKPDETn]. The flag may also be set if there is a change in the wakeup pin at the same time as the internal system clock or the internal pin wakeup clock. Note that if the pin toggles then the flag may be set regardless of whether the pin is selected as posedge or negedge.

Workaround: Workaround for unintentional flag setting during configuration, would be to first complete the pin wakeup configuration (i.e. select pin wakeup clock, select pin muxing, and configure pin enable/edge detect via the CRP registers CRP_WKSE[WKCLKSEL], CRP_WKPINSEL[WKPSELn], and CRP_WKSE[WKPDETn]). Then poll the CRP_PSCR[PWKSCRF] pin wakeup flag and if set write one to clear and then recheck. May take one pin wakeup clock cycle to clear.

Workaround for unintentional flag setting during pin change is to have the SLEEPF and STOPF flags in CRP_PSCR checked in the CRP interrupt service routine and if neither of them is set then clear all flags in CRP_PSCR[PWKSRCF].

e575: DSPI: Changing CTARs between frames in continuous PCS mode causes error

Errata type: Errata

Description: Erroneous data could be transmitted if multiple Clock and Transfer Attribute Registers (CTAR) are used while using the Continuous Peripheral Chip Select mode (DSPIx_PUSHR[CONT=1]). The conditions that can generate an error are:

1) If DSPIx_CTARn[CPHA]=1 and DSPIx_MCR[CONT_SCKE = 0] and DSPIx_CTARn[CPOL, CPHA, PCSSCK or PBR] change between frames.

2) If DSPIx_CTARn[CPHA]=0 or DSPIx_MCR[CONT_SCKE = 1] and any bit field of DSPIx_CTARn changes between frames except DSPIx_CTARn[PBR].

Workaround: When generating DSPI bit frames in continuous PCS mode, adhere to the aforementioned conditions when changing DSPIx_CTARn bit fields between frames.

e1103: DSPI: PCS Continuous Selection Format limitation

Errata type: Errata

Description: When the DSPI module has more than one entry in the TX FIFO and only one entry is written and that entry has the CONT bit set, and continuous SCK clock selected the PCS levels may change between transfer complete and write of the next data to the DSPI_PUSHR register.

For example:

If the CONT bit is set with the first PUSHR write, the PCS de-asserts after the transfer because the configuration data for the next frame has already been fetched from the next (empty) fifo entry. This behavior continues till the buffer is filled once and all CONT bits are one.

Workaround: To insure PCS stability during data transmission in Continious Selection Format and Continious SCK clock enabled make sure that the data with reset CONT bit is written to DSPI_PUSHR register before previous data sub-frame (with CONT bit set) transfer is over.

e1082: DSPI: set up enough ASC time when MTFE=1 and CPHA=1

Errata type: Information

Description: When the DSPI is being used in the Modified Transfer Format mode (DSPI_MCR[MTFE]=1) with the clock phase set for Data changing on the leading edge of the clock and captured on the following edge in the DSPI Clock and Transfer Attributes Register (DSPI_CTARn[CPHA]=1), if the After SCK delay scaler (ASC) time is set to less than 1/2 SCK clock period the DSPI may not complete the transaction - the TCF flag will not be set, serial data will not received, and last transmitted bit can be truncated.

Workaround: If the Modified Transfer Format mode is required DSPI_MCR[MTFE]=1 with the clock phase set for serial data changing on the leading edge of the clock and captured on the following edge in the SCK clock (Transfer Attributes Register (DSPI_CTARn[CPHA]=1) make sure that the ASC time is set to be longer than half SCK clock period.

e237: EBI: ALE timing specification is not met under all conditions

Errata type: Errata

Description: The External Bus Interface Address Latch Enable (ALE) signal's Falling Edge to Address/Data (AD) Invalid (Talead) timing specification does not meet the 2 ns minimum in the Data Sheet across the full operating range (voltage and temperature range) and may not provide enough margin when interfacing to external logic.

Workaround: In order to increase the ALE falling edge to AD Invalid (Talead) timing margin, Slew Rate Control bits in the Pin Control Register for the AD signals should be configured for medium slew rate (SIU_PCRn[SRC]=0b01). The control signals (ALE, WE/BE, CS, R/W, OE, etc) must

be set to maximum slew rate (SIU_PCRn[SRC]=0b11. This configuration will provide a guaranteed Talead of at least 4ns. Note that since this configuration may delay the Output Delay (Tcov) for the AD pins to a maximum of 35ns, additional EBI wait states may be required.

e1741: EQADC : 25% calibration channel sampling requires at least 64 sampling cycles

Errata type: Information

Description: The 25%*(VRH-VRL) calibration channel (ADC channel 44) will not convert to specification with an ADC sample time less than 64 cycles.

Workaround: For accurate calibration, the 25% calibration channel should be converted using the Long Sample Time (LST) setting for either 64 or 128 ADC sample cycles in the ADC Conversion Command Message (LST = 0b10 or 0b11).

e652: EQADC: 50% reference channels reads 20 mv low

Errata type: Information

Description: The equation given for the definition of the 50% reference channel (channel 42) of the Enhanced Queued Analog to Digital Converter (eQADC) is not correct. The 50% reference point will actually return approximately 20mV (after calibration) lower than the expected 50% of difference between the High Reference Voltage (VRH) and the Low Reference Voltage (VRL).

Workaround: Do not use the 50% point to calibrate the ADC. Only use the 25% and 75% points for calibration.

After calibration, software should expect that the 50% Reference will read 20 mV low.

e2075: FLASH: Large blocks limited to 1,000 Program/erase cycles

Errata type: Errata

Description: The electrical specification for Program/Erase cycling on large Flash blocks (all 128K blocks - Middle Address Space [MAS] blocks M0 and M1, plus High Address Space [HAS] blocks H0 to H3/H7/H11/H19 [depending on total flash size]) has been changed to 1,000 PE cycles minimum. The small blocks (16K, 48K, and 64K - Low Address Space [LAS] blocks L0-L5) are still specified as 100,000 PE cycles minimum.

The data retention specification all blocks is still 20 years for blocks cycled less than 1000 times and 5 years for blocks cycled 1001 to 100,000 cycles (1,000 for large blocks).

Workaround: Only use the small blocks for EEPROM emulation (LAS L0-L5). Do not use blocks MAS M0/M1 or HAS H0 to H3/H7/H11/H19 (depending on total flash size) for EEPROM emulation requiring greater than 1,000 Program/Erase cycles. Refer to the latest device electrical specifications (Data Sheet) dated July 2007 or later.

e605: FLASH: Minimum Programming Frequency is 25 MHz

Errata type: Information

Description: Programming and erase operations of the internal flash could fail if the clock to the flash (usually the system clock) is less than 25 MHz.

Workaround: Do not program or erase the flash when the system operating frequency is below 25Mhz.

e1178: FLASH: Possible Flash Read Corruption if Prefetch Enabled

Errata type: Errata

Description: Enabling flash prefetching may during flash read accesses cause incorrect code execution. Both flash ports 0 and 1 as configured using the PFCRP0 and PFCRP1 registers are affected. All masters as enabled by PFCRPx[MnPFE] are affected. Data and Instruction prefetch as enabled by PRCRPx[DPFEN] and PRCRPx[IPFEN]are affected.

Workaround: Do not enable flash prefetching. Prefetch is disabled when all PRCRPx[MnPFE] bits are cleared or if both PRCRPx[DPFEN] and PRCRPx[IPFEN] bits are cleared for both flash ports. Flash prefetching will also be disabled if PRCRPx[BFEN] is cleared or if PRCRPx[PFLIM] is cleared for both flash ports. With flash prefetching disabled, the line read buffers may still be utilized if PRCRPx[BFEN] is set.

e169: FLASH: SIZE indicates 1.5M regardless of flash size

Errata type: Information

Description: The size identifier in the FLASH Module Configuration Register (MCR[SIZE]) is 0x0101 indicating 1.5M of flash regardless of the actual flash size.

Workaround: Use only the size of flash indicated in the device definition (shown below for reference).

MPC5514 512K

MPC5515 768K

MPC5516 1M

MPC5517 1.5M

e2083: FLASH: The ADR register may get loaded with a flash address even through no ECC error has occurred

Errata type: Information

Description: The Flash Address Register (FLASH_AR) may be loaded with a flash address when no Error Correction Code (ECC) has occurred. When an ECC does occur, the FLASH_AR is properly set.

Workaround: Check the Flash Module Control Register ECC Event Error (FLASH_MCR[EER]=1) to check for an ECC error before examining the ADR register. If an error has occurred then the ADR register data is valid. If an error has not occurred then the FLASH_AR data could change on any flash access.

e1111: FMPLL: LOLF can be set on MFD change

Errata type: Errata

Description: Normally, the Loss of Lock Flag (FMPLL_SYNCR[LOLF]) would not be set if the loss of lock occurred due to changing of the Multiplication Factor Divider bits or PREDIV bits (FMPLL_SYNCR[MFD] or [PREDIV]) or enabling of Frequency Modulation (FMPLL_SYNCR[Depth]>0b00). However, if LOLF has been set previously (due to an unexpected loss of lock condition) and then cleared (by writing a 1), a change of the MFD, PREDIV or DEPTH fields can cause the LOLF to be set again which can trigger an interrupt request if LOLIRQ bit is set.

In addition, changing the RATE bit will also set the LOLF regardless of previous conditions.

Workaround: The Loss of Lock Interrupt Request enable in the Synthesizer Control Register (FMPLL_SYNCR[LOLIRQ]) should be cleared before any change to the multiplication factor (MFD), PREDIV, modulation depth (DEPTH), or modulation rate (RATE) to avoid unintentional interrupt requests. After the PLL has locked (LOCK=1), LOLF should be cleared (by writing a 1) and LOLIRQ may be set again if required.

e4195: FMPLL: Loss of SCM Clock

Errata type: Errata

Description: If the Self Clock Mode (SCM) is enabled and the Phase Lock Loop (PLL) experiences a loss of clock, sometimes the PLL output clock can stop when in SCM mode.

Workaround: Do not use SCM mode. If enabling the Loss of Clock (LOCEN in the ESYNCR2 register), also set the Loss of Clock Reset Enable bit (LOCRE=1 in the ESYNCR2 register) and then the SoC which will force the system clock source back to the internal 16MIRC instead of the SCM PLL output clock which is the safest clock to be using. Note, the Loss of Lock is not affected by this erratum.

e2656: FlexCAN: Abort request blocks the CODE field

Errata type: Errata

Description: An Abort request to a transmit Message Buffer (TxMB) can block any write operation into its CODE field. Therefore, the TxMB cannot be aborted or deactivated until it completes a valid transmission (by winning the CAN bus arbitration and transmitting the contents of the TxMB).

Workaround: Instead of aborting the transmission, use deactivation instead.

Note that there is a chance that the deactivated TxMB can be transmitted without setting IFLAG and updating the CODE field if it is deactivated.

e3407: FlexCAN: CAN Transmitter Stall in case of no Remote Frame in response to Tx packet with RTR=1

Errata type: Errata

Description: FlexCAN does not transmit an expected message when the same node detects an incoming Remote Request message asking for any remote answer.

The issue happens when two specific conditions occur:

1) The Message Buffer (MB) configured for remote answer (with code "a") is the last MB. The last MB is specified by Maximum MB field in the Module Configuration Register (MCR[MAXMB]).

2) The incoming Remote Request message does not match its ID against the last MB ID.

While an incoming Remote Request message is being received, the FlexCAN also scans the transmit (Tx) MBs to select the one with the higher priority for the next bus arbitration. It is expected that by the Intermission field it ends up with a selected candidate (winner). The coincidence of conditions (1) and (2) above creates an internal corner case that cancels the Tx winner and therefore no message will be selected for transmission in the next frame. This gives the appearance that the FlexCAN transmitter is stalled or "stops transmitting".

The problem can be detectable only if the message traffic ceases and the CAN bus enters into Idle state after the described sequence of events.

There is NO ISSUE if any of the conditions below holds:

a) The incoming message matches the remote answer MB with code "a".

b) The MB configured as remote answer with code "a" is not the last one.

c) Any MB (despite of being Tx or Rx) is reconfigured (by writing its CS field) just after the Intermission field.

d) A new incoming message sent by any external node starts just after the Intermission field.

Workaround: Do not configure the last MB as a Remote Answer (with code "a").

e2360: FlexCAN: Global Masks misalignment

Errata type: Errata
Description: Convention: MSB=0.

During CAN messages reception by FlexCAN, the RXGMASK (Rx Global Mask) is used as acceptance mask for most of the Rx Message Buffers (MB). When the FIFO Enable bit in the FlexCAN Module Configuration Register (CANx_MCR[FEN], bit 2) is set, the RXGMASK also applies to most of the elements of the ID filter table. However there is a misalignment between the position of the ID field in the Rx MB and in RXIDA, RXIDB and RXIDC fields of the ID Tables. In fact RXIDA filter in the ID Tables is shifted one bit to the left from Rx MBs ID position as shown below:

Rx MB ID = bits 3-31 of ID word corresponding to message ID bits 0-28

RXIDA = bits 2-30 of ID Table corresponding to message ID bits 0-28

Note that the mask bits one-to-one correspondence occurs with the filters bits, not with the incoming message ID bits.

This leads the RXGMASK to affect Rx MB and Rx FIFO filtering in different ways.

For example, if the user intends to mask out the bit 24 of the ID filter of Message Buffers then the RXGMASK will be configured as 0xffff_ffef. As result, bit 24 of the ID field of the incoming message will be ignored during filtering process for Message Buffers. This very same configuration of RXGMASK would lead bit 24 of RXIDA to be "don't care" and thus bit 25 of the ID field of the incoming message would be ignored during filtering process for Rx FIFO.

Similarly, both RXIDB and RXIDC filters have multiple misalignments with regards to position of ID field in Rx MBs, which can lead to erroneous masking during filtering process for either Rx FIFO or MBs.

RX14MASK (Rx 14 Mask) and RX15MASK (Rx 15 Mask) have the same structure as the RXGMASK. This includes the misalignment problem between the position of the ID field in the Rx MBs and in RXIDA, RXIDB and RXIDC fields of the ID Tables.

Workaround: Therefore it is recommended that one of the following actions be taken to avoid problems:

*) Do not enable the RxFIFO. If CANx_MCR[FEN]=0 then the Rx FIFO is disabled and thus the masks RXGMASK, RX14MASK and RX15MASK do not affect it.

*) Enable Rx Individual Mask Registers. If the Backwards Compatibility Configuration bit in the FlexCAN Module Configuration Register (CANx_MCR[BCC], bit 15) is set then the Rx Individual Mask Registers (RXIMR0-63) are enabled and thus the masks RXGMASK, RX14MASK and RX15MASK are not used.

*) Do not use masks RXGMASK, RX14MASK and RX15MASK (i.e. let them in reset value which is 0xffff_ffff) when CANx_MCR[FEN]=1 and CANx_MCR[BCC]=0. In this case, filtering processes for both Rx MBs and Rx FIFO are not affected by those masks.

*) Do not configure any MB as Rx (i.e. let all MBs as either Tx or inactive) when CANx_MCR[FEN]=1 and CANx_MCR[BCC]=0. In this case, the masks RXGMASK, RX14MASK and RX15MASK can be used to affect ID Tables without affecting filtering process for Rx MBs.

e2685: FlexCAN: Module Disable Mode functionality not described correctly

Errata type: Errata

Description: Module Disable Mode functionality is described as the FlexCAN block is directly responsible for shutting down the clocks for both CAN Protocol Interface (CPI) and Message Buffer Management (MBM) sub-modules. In fact, FlexCAN requests this action to an external logic.

Workaround: In FlexCAN documentation chapter:

Section "Modes of Operation", bullet "Module Disable Mode":

Where is written:

"This low power mode is entered when the MDIS bit in the MCR Register is asserted. When disabled, the module shuts down the clocks to the CAN Protocol Interface and Message Buffer Management sub-modules.."

The correct description is:

"This low power mode is entered when the MDIS bit in the MCR Register is asserted by the CPU. When disabled, the module requests to disable the clocks to the CAN Protocol Interface and Message Buffer Management sub-modules."

Section "Modes of Operation Details", Sub-section "Module Disable Mode":

Where is written:

"This low power mode is entered when the MDIS bit in the MCR Register is asserted. If the module is disabled during Freeze Mode, it shuts down the clocks to the CPI and MBM sub-modules, sets the LPM_ACK bit and negates the FRZ_ACK bit.."

The correct description is:

"This low power mode is entered when the MDIS bit in the MCR Register is asserted. If the module is disabled during Freeze Mode, it requests to disable the clocks to the CAN Protocol Interface (CPI) and Message Buffer Management (MBM) sub-modules, sets the LPM_ACK bit and negates the FRZ_ACK bit."

e1388: FlexRay: Incomplete Transmission of Message Frame in Key Slot

Errata type: Errata

Description: The FlexRay module will transmit an incomplete message in the key slot under the following circumstances:

1.) The transmit message buffer n assigned to the key slot is located in the message buffer segment 2, i.e. FR_MBSSUTR[MB_LAST_SEG1] < n, and

2.) the data size of the message buffer segment 1 is smaller than the static payload length, i.e. FR_MBDSR[MBSEG1DS] < PCR19[payload_length_static].

In this case, the FlexRay module will transmit only FR_MBDSR[MBSEG1DS] payload words from message buffer n. The remaining words are padded with 0's.

Workaround: The transmit message buffer assigned to key slot must be located in message buffer segment 1.

e2302: FlexRay: Message Buffer can not be disabled and not locked after CHI command FREEZE

Errata type: Errata

Description: If a complete message was transmitted from a transmit message buffer or received into a message buffer and the controller host interface (CHI) command FREEZE is issued by the application before the end of the current slot, then this message buffer can not be disabled and locked until the module has entered the protocol state normal active.

Consequently, this message buffer can not be disabled and locked by the application in the protocol config state, which prevents the application from clearing the commit bit CMT and the module from clearing the status bits. The configuration bits in the Message Buffer Configuration, Control, Status Registers (MBCCSRn) and the message buffer configuration registers MBCCFRn, MBFIDRn, and MBIDXRn are not affected.

At most one message buffer per channel is affected.

Workaround: There are two types of workaround.

1) The application should not send the CHI command FREEZE and use the CHI command HALT instead.

2) Before sending the CHI command FREEZE the application should repeatedly try to disable all message buffers until all message buffers are disabled. This maximum duration of this task is three static or three dynamic slots.

e2388: IRC: 32K/16M IRC Trim Data Swapped

Errata type: Errata

Description: 32K and 16M IRC trim values (8 bits each) stored in the flash shadow row starting at location 0x00FF_FDE6 are stored opposite than what is stated in the Reference Manual. The order that they are now stored in the shadow row is the 16M trim value followed by the 32K trim value.

Workaround: For the 16M IRC trim value (TRIMIRC), read the shadow row location 0xFF_FDE6 and write to Clock Reset Power module clock source register (CRP_CLKSRC).

For the 32K IRC trim value (TRIM32IRC), read the shadow row location 0xFF_FDE7 and write to Clock Reset Power module clock source register (CRP_CLKSRC).

e164: JTAGC: SAMPLE instruction does not sample input data during board boundary scan testing.

Errata type: Errata

Description: Executing the SAMPLE instruction should take a snapshot of the input and output signals present at the pins, without interfering with the normal operation of the chip.

For pins configured as inputs, executing the SAMPLE instruction will result in the internally set, off value, of the pad being sampled and not the actual input value of the pin.

Workaround: Do not expect to sample input pin values when executing the SAMPLE or SAMPLE/PRELOAD instructions when using JTAG. Use the EXTEST and PRELOAD instructions to test connections between devices during boundary scan testing of boards.

e1004: MPC5516: SIU_MIDR[PARTNUM] is 5516, [MASKNUM] is 0x10, DID[PIN]=0x116

Errata type: Information

Description: The part number field in the MCU Identification Register (SIU_MIDR[PARTNUM]) is 0x5516. The mask revision number (SIU_MIDR[MASKNUM]) is 0x10. The Part Identification Number field in both the Nexus Port Controller Device Identification Register (NPC_DID[PIN]) and JTAGC Identification Register (JTAGC_DID[PIN]) is 0x116. The Part Revision Number field in both the Nexus Port Controller Device Identification Register (NPC_DID[PRN]) and JTAGC Identification Register (JTAGC_DID[PRN]) is 0x1.

Workaround: Software should be aware that the SIU_MIDR[MASKNUM], NPC_DID[PRN], and JTAGC_DID[PRN] fields may change in the future.

e2161: NPC: Automatic clock gating does not work for MCKO_DIV = 8

Errata type: Errata

Description: If the Nexus clock divider (NPC_PCR[MCKO_DIV]) in the Nexus Port Controller Port Configuration Register is set to 8 and the Nexus clock gating control (NPC_PCR[MCKO_GT]) is enabled, the nexus clock (MCKO) will be disabled prior to the completion of transmission of the Nexus message data.

Workaround: Do not enable the automatic clock gating mode when the Nexus clock divider is set to 8. If Nexus clock gating is required, use a divide value of 1, 2 or 4 (set NPC_PCR[MCKO_GT]=0b1 and NPC_PCR[MCKO_DIV]=0b000, 0b001, or 0b011). However, MCKO must be kept below the maximum Nexus clock rate as defined in the device data sheet. If divide by 8 clock divider is required, then do not enable clock gating (set NPC_PCR[MCKO_GT]=0b0 and NPC_PCR[MCKO_DIV]=0b111).

e3116: NPC: TCK frequency must be lower than system frequency in low power modes for communication

Errata type: n/a

Description: The JTAG Clock (TCK) typically operates at a frequency well below the system clock frequency, as specified in the electrical data sheets. In some cases, however, such as low power mode (if the device supports low power modes), the system clock frequency may be lowered significantly from the normal operating range. If the system clock frequency is reduced below the frequency of TCK it will no longer be possible to communicate with the Nexus Port Controller Port Configuration Register (NPC_PCR). Therefore, if the tool needs to update the NPC_PCR Low Power Debug Enable (NPC[PCR[LP_DBG]) or Low Power Synchronization bits (NPC[PCR[LP1_SYN] and NPC[PCR[LP2_SYN]), the clock frequency must be lowered.

Workaround: Insure that the frequency of TCK does not exceed the system clock frequency during normal operation and during low power operation.

e3377: Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge

Errata type: Errata

Description: The Nexus Output pins (Message Data outputs 0:15 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance driver (when used as a general purpose input [GPI] in the application).

Workaround: 1. Do not tie the Nexus output pins directly to ground or a power supply.

2. If these pins are used as GPI, limit the current to the ability of the regulator supply to guarantee correct start up of the power supply. Each pin may draw upwards of 150mA.

If not used, the pins may be left unconnected.

e1136: eDMA: BWC setting may be ignored between 1st and 2nd transfers and after the last write of each minor loop.

Errata type: Errata

Description: The eDMA Transfer Control Descriptor Bandwidth Control field setting may be ignored between 1st and 2nd transfers and after the last write of each minor loop. This will occur if the source and destination sizes are equal. This behavior is a side effect of measures designed to reduce start-up latency. Reference Manuals may fail to mention this behavior.

Workaround: There are 2 possible workarounds:

1) Adjust the Transfer Control Descriptor (TCD) to make the source size not equal to the destination sizes (i.e. ssize = 16 bit, dsize = 32 bit). This delays the write which allows BWC[0:1] arriving from the TCD to be considered in the execution pipeline during start-up.

2) Adjust the TCD so the channel executes a single read/write sequence and then retires. In addition, the channel can be configured to execute a minor loop link to itself which will restart the channel after arbitration and channel start-up latency. The total number of bytes transferred can be controlled by the major loop count.

e1773: eQADC: conversions of muxed digital/analog channels close to the rail

Errata type: Information

Description: If the VDDEH9 and the VDDA power supplies are at different voltage levels, the input clamp diodes on the multiplexed digital and analog signals (AN12, AN13, AN14, and AN15) will clamp to the lower of the two supplies.

If VDDEH9 is lower than the VDDA, conversions on these channels will not obtain full scale readings if voltage is close the the VDDA voltage.

Workaround: When multiplexed digital/analog signals are used as analog inputs, connect VDDEH9 to VDDA and do not use any of the digital functions multiplexed on these pins.

e1013: eSCI : Automatic reset of the LIN state machine cause incorrect transmission

Errata type: Errata

Description: When the LIN FSM of the eSCI module performs an automatic reset due to a bus error condition, it is possible that the application is no longer synchronized to the LIN FSM. As a result, the eSCI may consider the payload data provided by the application via the LIN Transmit Register (eSCI_LTR) as a LIN frame header data and will generate an unexpected LIN frame.

Workaround: The application should disable the automatic LIN FSM reset functionality by setting LDBG bit in the LIN Control Register (eSCI_LCR) to 1.

e1381: eSCI: LIN Wakeup flag set after aborted LIN frame transmission

Errata type: Errata

Description: If the eSCI module is transmitting a LIN frame and the application sets and clears the LIN Finite State Machine Resync bit in the LIN Control Register 1 (eSCI_LCR1[LRES]) to abort the transmission, the LIN Wakeup Receive Flag in the LIN Status Register may be set (LWAKE=1).

Workaround: If the application has triggered LIN Protocol Engine Reset via the eSCI_LCR1[LRES], it should wait for the duration of a frame and clear the eSCI_IFSR2[LWAKE] flag before waiting for a wakeup.

e1221: eSCI: LIN bit error indicated at start of transmission after LIN reset

Errata type: Errata

Description: If the eSCI module is in LIN mode and is transmitting a LIN frame, and the application sets and subsequently clears the LIN reset bit (LRES) in the LIN Control register 1 (ESCI_LCR1), the next LIN frame transmission might incorrectly signal the occurrence of bit errors (ESCI_IFSR1[BERR]) and frame error (ESCI_IFSR1[FE]), and the transmitted frame might be incorrect.

Workaround: There is no generic work around. The implementation of a suitable workaround is highly dependent on the application and a workaround may not be possible for all applications.

e1017: eSCI: LIN fast bit error detection causes incorrect LIN reception

Errata type: Errata

Description: When using the eSCI module in LIN mode, if the fast bit error detection is enabled in the eSCI Control Register 2 (eSCIx_CR2[FBR]) and a bit distortion occurs on the RX line, the eSCI module may process the bit error signal incorrectly. This may cause unexpected transmission and reception behavior of the LIN state machine.

Workaround: The application should disable the fast bit error detection by setting the FBR bit to 0.

e2190: eSCI: LIN slave timeout flag STO not asserted if CRC is received too late

Errata type: Errata

Description: The eSCI module will not assert the Slave-Timeout Flag (STO) in the eSCI LIN Status Register 1 (LINSTAT1) if the checksum field of on RX frame is received later than the time given in the Timeout Value (TO) field of the LIN RX control header.

If the checksum field of on RX frame is not received at all, The STO flag will not be set and the LIN FSM will wait forever.

Workaround: The application should use a timer external to the eSCI module, that is started when a LIN RX frame transmission is started with an expiration time programmed to the expected duration of the reception. The timer is stopped, when the eSCI module signals the end of the LIN frame reception. If this timer expires, the eSCI has ran into the slave timeout condition. In this case, the application should clear the SCICR2[TE] and SCICR2[RE] bits to disable the transmitter and receiver, and should set the LINCTRL1[LRES] bit the reset the eSCI internal LIN slave and master tasks. To resume LIN frame data transmission the application should enable the transmitter and receiver and clear the LINCTRL1[LRES] bit to enable the LIN slave and master tasks.

e1614: eSCI: Low pulse on LIN RX line may prevent assertion of transmit data ready flag ESCI_SR[TXRDY]

Errata type: Errata

Description: If the eSCI module is in LIN mode and receives a low pulse on the RX line while transmitting a frame header or a stop bit, the eSCI internal LIN master and slave tasks may be stopped, and the transmit data ready flag ESCI_SR[TXRDY] will never be asserted again.

Each of the following scenarios of the RX low pulse may provoke this erroneous behavior.

a) The low pulse begins less than 12 bits before the start of the break character, and ends at least 21 bits and at most 30 bits after the start of the break character.

b) The low pulse begins at least 13 bits and at most 14 bits after the start of the break character, and ends at least 22 bits after the start of the break character.

c) The low pulse begins during the stop bit and has duration of at least 2 bits.

Workaround: The application should use a timer external to the eSCI module, that is started when a LIN frame transmission is started with an expiration time programmed to the expected duration of the transmission. The timer is stopped, when the eSCI module signals the end of the LIN frame transmission.

If this timer expires, the eSCI tasks have been stopped internally. In this case, the application should clear the Transmit Enable (SCICR2[TE]) and the Receive Enable (SCICR2[RE] bits to disable the transmitter and receiver, and should set the LIN FSM resync (LINCTRL1[LRES]) bit the reset the eSCI internal LIN slave and master tasks.

To resume LIN frame data transmission the application should enable the transmitter and receiver and clear the LINCTRL1[LRES] bit to enable the LIN slave and master tasks.

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