

MCF52110 Reference Manual Addendum

Devices Supported: MCF52110, MCF52100

by: Microcontroller Solutions Group

This document describes corrections to the *MCF52110 Reference Manual*, order number MCF52110RM. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com/coldfire> for the latest updates.

The current available version of the *MCF52110 Reference Manual* is Revision 2.

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1 Addendum for Revision 2

Table 1. MCF52110RM Rev. 2 Addendum

Location	Description
<p>Chapter "Clock Module"/Section "Block Diagram"/Figure "Clock Module Block Diagram"</p>	<p>Updated the Figure "Clock Module Block Diagram"</p> <ul style="list-style-type: none"> • Changed PPM to PPMRL[17] • Changed PP to PPMRH[11] <p>The diagram illustrates the clock module architecture. It starts with three clock sources: kHz OSCILLATOR (from RTC_EXTAL and RTC_XTAL), MHz OSCILLATOR (from EXTAL and XTAL), and ON-CHIP 8 MHz. These sources feed into a multiplexer controlled by OSCSEL1 and OSCSE. The output goes through a Pre-Divider (controlled by CCHR) to become the Ref Clock. This Ref Clock is then processed by a PLL (controlled by CLKMOD1 and CLKSRC) to produce the System Clock (f_{sys}). A PLL Bypass Clock path is also shown. The System Clock is then distributed to various components: ColdFire V2, BDM, and CLKOUT (via DISCLK). A ÷2 divider feeds into a series of PPMRL registers (PPMRL[1], PPMRL[17], PPMRL[16:13], PPMRL[10], PPMRL[9:8], PPMRL[7:5], PPMRL[4]) which are connected to ColdFire V2, Interrupt Controller, DMA Timers, QSPI, I²Cs, UARTs, and DMA. Another series of PPMRH registers (PPMRH[11], PPMRH[9], PPMRH[8], PPMRH[7], PPMRH[14], PPMRH[4:3], PPMRH[1], PPMRH[0]) are connected to CFM, PWM, GPT, ADC, RTC, PITs, Edge Port, and GPIO / Ports. The Low Power Divider (controlled by LPD[3:0]) provides a STOP MODE clock. The RTC DIV (controlled by RTCGOCNT) provides the RTC_Clk¹. The ON-CHIP 8 MHz source also provides the BWT_Clk¹.</p>

2 Addendum for Revision 1

Table 2. MCF52110RM Rev. 1 Addendum

Location	Description
Throughout	Formatting, layout, spelling, and grammar corrections.
Table 2-1 / Page 2-3	Synchronized the table in the reference manual and the device data sheet.
Table 6-4 / Page 6-6	Corrected the CCHR reset value (was 0x04, is 0x00).
Figure 6-6 / Page 6-12	Added the missing last digit (0) to the CCHR reset value.
Figure 6-12 / Page 6-19	Deleted the RS resistor.
Chapter 8	Deleted references to nonexistent FlexCAN module.
Chapter 11	Added information about the RTC general oscillator count registers, RTCGOCU and RTCGOCL.
Figure 11-13	Corrected the code example for initializing the RTC.
Section 12.5.4 / Page 12-7	Updated the section to reflect the fact that the CWT does not cause a hardware reset.
Table 12-6 / Page 12-8	In the CWCR[CWRI] field description, changed “The interrupt level for the CWT is programmed in the interrupt control register 7 (ICR7)...” to “The interrupt level for the CWT is programmed in the interrupt control register 8 (ICR8)...”.
Table 12-15 / Page 12-18	Deleted reference to nonexistent FlexCAN module.
Section 12.7.3.1 / Page 12-14	<ul style="list-style-type: none"> • Rewrote the introductory text describing the MPR (removing erroneous reference to a fast Ethernet controller). • Corrected the MPR reset value (was 0x11, is 0x1).
Section 14-1 / Page 14-2	Deleted the sentence beginning with “For many peripheral devices...”.
Table 14-2 / Page 14-5	Deleted the entry for the (nonexistent) GSWIACK register.
Section 14.3.8 / Page 14-16	Deleted references to the (nonexistent) GSWIACK register.
Section 16.4 / Page 16-12	Deleted the sentence “BCR _n decrements when an address transfer write completes for a single-address access (DCR _n [SAA] = 0), or when SAA equals 1.”
Figure 23-6 / Page 23-9	Added a note to clarify the UCSR _n reset values.
Figure 23-20 / Page 23-21	<ul style="list-style-type: none"> • Corrected the label of the top signal (was U_nTXD, is U_nRXD). • Corrected the text in the footnote (was TXRTS, is RXRTS).
Figure 23-23 / Page 23-24	Corrected the U _n TXD label (was “Input”, is “Output”).
Figure 23-24 / Page 23-25	<ul style="list-style-type: none"> • Corrected a label on the bottom row (was UMR1_n[PT]=2, is UMR1_n[PT]=1). • Deleted duplicate UMR1_n[PM]=11 label.
Section 23.5.1.2 / Page 23-27	Added example DMA configuration steps.
Section 26.3.2.5.1 / Page 26-18	Corrected the numerical values in the left-aligned example.
Section 26.3.2.6.1 / Page 26-20	Corrected the numerical values in the center-aligned example.
Appendix A	<ul style="list-style-type: none"> • Deleted the entry for the (nonexistent) GSWIACK register. • Added entries for the RTCGOCU and RTCGOCL registers.

3 Revision History

Table 3 provides a revision history for this document.

Table 3. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1	Initial release, incorporating corrections listed in Table 2 .	06/2007
2	Corrected errors in Chapter “Clock Module” listed in Table 1	12/2011

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