Mask Set Errata for Mask 1N16S

This report applies to mask 1N16S for these products:

- MKW41Z512VHT4, MKW41Z256VHT4
- MKW31Z512VHT4, MKW31Z256VHT4
- MKW21Z512VHT4, MKW21Z256VHT4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e8992	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e50117	FAC: Execute-only access control feature has been deprecated
e11368	FLASHLOADER: Kinetis Flashloader Is Not Pre-Programmed in the Flash of MCU Devices
e10527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
e7993	MCG: FLL frequency may be incorrect after changing the FLL reference clock
e7914	PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.
e10224	RSIM: XTAL_OUT_EN signal from the pin is enabled by default

Table 2. Revision History

Revision	Changes
28 SEP 2016	Initial revision
30 MAY 2018	The following errata were revised. • e11368
06 SEP 2018	The following errata were added. • e8992
25 JUL 2019	The following errata were added. • e50117

e8992: AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode

Description: Upon entry into VLPS from VLPR, if NMI is asserted before the VLPS entry completes, then the NMI does not generate a wakeup to the MCU. However, the NMI interrupt will occur after the MCU wakes up by another wake-up event.

Workaround: There are two workarounds:

1) First transition from VLPR mode to RUN mode, and then enter into VLPS mode from RUN mode.

2) Assert NMI signal for longer than 16 bus clock cycles.

e50117: FAC: Execute-only access control feature has been deprecated

Description: The FAC feature is no longer recommended for use.

Workaround: Do not program the XACCn registers to use the FAC feature.

e11368: FLASHLOADER: Kinetis Flashloader Is Not Pre-Programmed in the Flash of MCU Devices

Description: Devices manufactured before work week 29 (WW29) in 2018 do not have the Kinetis flashloader pre-programmed into the flash. The work week and year can be found in the date code on the device's package markings. The date code is embedded in the last line of the package markings and is represented by the YW markings which are characters 4-5 as follows:

xxx YW x

Devices with a date code of KB (work week 28 in 2018) and prior will not have the Kinetis Flashloader pre-programmed. Devices with a date code of KC (work week 29 in 2018) and later will have the Kinetis Flashloader pre-programmed.

Workaround: If devices with the preprogrammed flashloader are required, devices with date code KC or later should be used. Devices with the desired date code can be obtained by ordering directly from NXP after work week 29 of 2018 (July 13, 2018).

e10527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

e7993: MCG: FLL frequency may be incorrect after changing the FLL reference clock

Description: When the FLL reference clock is switched between the internal reference clock and the external reference clock, the FLL may jump momentarily or lock at a higher than configured frequency. The higher FLL frequency can affect any peripheral using the FLL clock as its input clock. If the FLL is being used as the system clock source, FLL Engaged Internal (FEI) or FLL Engaged External (FEE), the maximum system clock frequency may be exceeded and can cause indeterminate behavior.

Only transitions from FLL External reference (FBE, FEE) to FLL Internal reference (FBI, FEI) modes and vice versa are affected. Transitions to and from BLPI, BLPE, or PLL clock modes (if supported) are not affected because they disable the FLL. Transitions between the external reference modes or between the internal reference modes are not affected because the reference clock is not changed.

Workaround: To prevent the occurrence of this jump in frequency either the MCG_C4[DMX32] bit must be inverted or the MCG_C4[DRST_DRS] bits must be modified to a different value immediately before the change in reference clock is made and then restored back to their original value after the MCG_S[IREFST] bit reflects the selected reference clock.

If you want to change the MCG_C4[DMX32] or MCG_C4[DRST_DRS] to new values along with the reference clock, the sequence described above must be performed before setting these values to the new value(s).

e7914: PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

Description: If a write to the PIT module enable bit (PIT_MCR[MDIS]) occurs within two bus clock cycles of enabling the PIT clock gate in the SIM_CG register, the write will be ignored and the PIT will fail to enable.

Workaround: Insert a read of the PIT_MCR register before writing to the PIT_MCR register. This guarantees a minimum delay of two bus clocks to guarantee the write is not ignored.

e10224: RSIM: XTAL_OUT_EN signal from the pin is enabled by default

Description: The XTAL_OUT_EN signal from the default XTAL_OUT_EN pin, PTB0, is enabled out of reset. This will result in the reference oscillator being enabled when this pin is asserted high regardless of the port control multiplexor setting.

Workaround: To prevent the pin from enabling the XTAL out feature unintentionally, set RSIM_RF_OSC_CTRL[RADIO_EXT_OSC_OVRD_EN]=1.

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