ES_LPC111x

Errata sheet LPC1111/12/13/14/15

Rev. 6.1 — 15 January 2024 **Errata**

Document information

Information	Content
Keywords	LPC1111FHN33, LPC1112FHN33, LPC1112FHI33, LPC1113FHN33, LPC1113FBD48, LPC1114FHN33, LPC1114FHI33, LPC1114FBD48, LPC1115FBD48, LPC1115FET48 LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

1 Product identification

The LPC111x devices typically have the following top-side marking:

LPC111xx
/xxx
xxxxxxx
xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC111x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision
'B'	Second device revision
'C'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2 Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	External sync inputs not operational	'A', 'B', 'C'	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	'A', 'B', 'C'	Section 3.2
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'A', 'B', 'C'	Section 3.3
VDD.1[1]	The minimum voltage of the power supply ramp must be 200 mV or below.	'A', 'B', 'C'	Section 3.3
ROM.1	The ROM inadvertently reports IAP busy status for IAP erase and program operations.	'A', 'B', 'C'	Section 3.5

[1] This errata does not apply to the LPC1100XL series (LPC111x/103/203/303/323/333).

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'A', 'B', 'C'	Section 5.1

3 Functional problems detail

3.1 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (this value should be used when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0.	
		0x3	Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0.	
		0x4	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0.	
		0x5	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1.	
		0x6	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0.	
		0x7	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1.	

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0_2 or PIO1_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC111x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.3 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1);         //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:                      // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:                      // data byte in DAT transmitted, ACK received
case 0xC0:                      // (last) data byte transmitted, NACK received
```

```
 case 0xC8:                    // last data byte in DAT transmitted, ACK received
        DataByte = LPC_I2C->DATA_BUFFER;        //
Save data. Data can be process in Main loop
        LPC_I2C-
>DAT = 0xFF;                                        // Pretend to shift out 0xFF
        LPC_I2C-
>CONCLR = 0x08;                                     // clear flag SI
 break;
```

VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below[1]

Introduction:

The datasheet specifies that the power supply (on the V_{DD} pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the V_{DD} pin) needs to be below 400 mV or below before ramping up is 12 us.

Problem:

The device might not always start-up if the power supply (on the V_{DD} pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the V_{DD} pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

Work-around:

None.

3.4 VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below[1]

Introduction:

The datasheet specifies that the power supply (on the VDD pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the V_{DD} pin) needs to be below 400 mV or below before ramping up is 12 us.

Problem:

The device might not always start-up if the power supply (on the V_{DD} pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the V_{DD} pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

Work-around:

None.

1 This errata does not apply to the LPC1100XL series (LPC111x/103/203/303/323/333).

3.5 ROM.1: On the LPC111XL series, the ROM inadvertently reports IAP busy status for IAP erase and program operations

Introduction:

On the LPC111XL series, In-Application Programming (IAP) calls are available to perform erase and write operation on the on-chip flash memory, as directed by the end-user application code. IAP status codes are available for the IAP calls.

Problem:

For IAP erase (sector and page) calls and IAP copy RAM to flash API calls, the ROM inadvertently reports that the flash programming hardware interface is busy (IAP status code 11). This issue affects the LPC1100 XL series devices (8 kB (LPC1111), 16 kB (LPC1112), 24 kB (LPC1113), 32 kB (LPC1114/203/303), 48 kB (LPC1114/323), 56 kB (LPC1114/333), 64 kB (LPC1115)).

Work-around:

The following software workaround can be implemented in the user application code. The example below is for IAP erase operations and utilizes the interrupt status register of the flash IP to ensure that the IAP erase operation is completed successfully:

```
 /* flash controller INT_STATUS register address for the workaround */
 #define     INT_STATUS   ((volatile unsigned *)(0x4003CFE0))
 #define     END_OF_BURN              (1<<1)
 #define     END_OF_ERASE             (1<<0)
__attribute__((section(".iap_ramfunc"))) uint32_t iap_erase_page(uint8_t
 page_start, uint8_t page_end)
        {
        volatile uint32_t dummy = 0;
        uint32_t dummy_pos = 0;
        struct sIAP IAP;
        IAP.cmd = IAP_ERASE_PAGE;                          // Erase Page
        IAP.par[0] = page_start;                          // Start page
        IAP.par[1] = page_end;                                 // End page
        IAP.par[2] = SystemCoreClock / 1000; // CCLK in kHz
        while (((*INT_STATUS) & 0x8) != 0)
        {
                dummy = *(volatile uint32_t *)(0x0 + dummy_pos);
                *INT_CLR_STATUS = 0x8;

                if(((*INT_STATUS) & 0x8) != 0x8)
                {
                        break;
                }
                /* Find a flash location without ECC error */
                dummy_pos += 4;
                /* For LPC1115, the flash size is 0x10000 */
                if (dummy_pos >= 0x10000)
                {
                        return BUSY;
                }
        }
        IAP_Call(&IAP.cmd, &IAP.stat); // Call IAP Command
        if (IAP.stat == BUSY)
        {
                // If it returns BUSY, wait until program/erase is done
```

```
                while ((*INT_STATUS & (END_OF_BURN | END_OF_ERASE)) == 0);
                IAP.stat = 0;
                return (IAP.stat); // Command Failed
        }
        return (0);
}
```

4 AC/DC deviations detail

No known errata.

5 Errata notes

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

6 Revision history

Table 5. Revision history

Rev	Date	Description
6.1	20240115	Replaced workaround in Section 3.5"ROM.1: On the LPC111XL series, the ROM inadvertently reports IAP busy status for IAP erase and program operations".
6	20191001	Describes inadvertent busy status for IAP erase and program operations. See: Section 3.5 "ROM.1: On the LPC111XL series, the ROM inadvertently reports IAP busy status for IAP erase and program operations".
5	20130926	• Added Rev. ‘C’. • Added LPC1115FET48, LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115 JET48.
4.1	20130201	Clarified Section 3.4, does not apply to LPC1100XL series (LPC111x/103/203/303/323/333).
4	20130116	Added Section 3.3 "I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register".
3.3	20120501	Removed LPC1110FD20, LPC1111FDH20, LPC1112FD20, LPC1112FDH20, LPC1112 FDH28, LPC1114FDH28, LPC1114FN28; placed in separate errata ES_LPC1110_11_12_ 14.
3.2	20120117	Added Section 3.2 "ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering".
3.1	20110901	Added Section 5.1 "Note.1".
3	20110301	• Combined LPC1111/12/13/14 errata into one document. • Added Section 3.4 "VDD.1". • Section 3.1: Removed text "For PCLK_ADC = 100 MHz...."
2	20101115	• Added Section 3.1 "ADC.1: External sync inputs not operational". • Added Rev. ‘B’.
1	20100510	Initial version.

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