ES_LPC1102

Errata sheet LPC1102

Rev. 2.2 — 18 January 2012 **Errata sheet**

Document information

Info	Content
Keywords	LPC1102UK errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
2.2	20120118	• Added ADC.2.
2.1	20110901	• Added Note.1.
2	20110301	• Added VDD.1. • Section 3.1: Removed text “For PCLK_ADC = 100 MHz....”
1	20101115	• Initial version

Contact information

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1. Product identification

The LPC1102 devices typically have the following top-side marking:

1102x

xxxxxx

xxxYWW

Field ‘Y’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 1. Functional problems table

Functional problems	Short description	Detailed description
ADC.1	External sync inputs not operational	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	Section 3.2
VDD.1	The minimum voltage of the power supply ramp must be 200 mV or below	Section 3.3

Table 2. AC/DC deviations table

AC/DC deviations	Short description	Detailed description
n/a	n/a	n/a

Table 3. Errata notes

Note	Short description	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	Section 5.1

3. Functional problems detail

3.1 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		0x0	No start (this value should be used when clearing PDN to 0).	
		0x1	Start conversion now.	
		0x2	Start conversion when the edge selected by bit 27 occurs on PIO0_2/SSEL/CT16B0_CAP0.	
		0x3	Start conversion when the edge selected by bit 27 occurs on PIO1_5/DIR/CT32B0_CAP0.	
		0x4	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT0.	
		0x5	Start conversion when the edge selected by bit 27 occurs on CT32B0_MAT1.	
		0x6	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT0.	
		0x7	Start conversion when the edge selected by bit 27 occurs on CT16B0_MAT1.	

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on PIO0_2 or PIO1_5 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC1102, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.3 VDD.1: The minimum voltage of the power supply ramp must be 200 mV or below

Introduction:

The datasheet specifies that the power supply (on the V_{DD} pin) must ramp-up from a minimum voltage of 400 mV or below with a ramp-up time of 500 ms or faster. Also, the minimum time the power supply (on the V_{DD} pin) needs to be below 400 mV or below before ramping up is 12 us.

Problem:

The device might not always start-up if the power supply (on the V_{DD} pin) does not reach 200 mV. The minimum voltage of the power supply ramp (on the V_{DD} pin) must be 200 mV or below with ramp-up time of 500 ms or faster.

Work-around:

None.

4. AC/DC deviations detail

No known errata.

5. Errata notes

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

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