

56F802

Chip Errata

DSP56F802 Digital Signal Controller

This document reports errata information on chip revision A. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.

Note: [Differences Between Errata Sheet Revisions are listed on page 5](#) and errata information for chip revisions prior to revision C have been archived and can be requested from Motorola Sales.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F802 devices. These parts are devices marked as DSP56F802 or as PC56F802 with datecodes of 0152 or later.

Errata Number	Description	Impact and Work Around
1.0	Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses.	Impact: The IP clock rate creates an extra pulse. Work Around: Program n-1 pulses only when operating at Maximum clock rate.
2.0	PWM outputs are not disabled during DEBUG mode.	Impact: Safety considerations if PWM outputs are not disabled prior to entering DEBUG mode. Work Around: Disable PWM outputs prior to entering DEBUG mode. PWM module will continue to operate while in DEBUG mode unless explicitly disabled.
3.0	Program Flash Interface Unit (PFIU) address register read returns wrong value when writing an out-of-row address.	Impact: When verifying the out-of-row write, the PFIU returns the address applied to the Flash pins, which is a concatenation of the ROW register and ADDRESS[4:0] bits. Work Around: None
4.0	Low Analog input voltages to ADC may not be measured properly.	Impact: Inputs < 100mV may yield measurements = 0. Work Around: Bias Analog inputs above 100mV.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F802 devices. These parts are devices marked as DSP56F802 or as PC56F802 with datecodes of 0152 or later.

Errata Number	Description	Impact and Work Around
5.0	Optimal ADC setup.	Impact: Better accuracy Work Around: Recommended values for ADCDIV Register: 4, 9, or 14.
6.0	N register is not available the cycle immediately after it has a value change.	Impact: In the case of an index+ offset move into the N register, N is not available in the cycle immediately following the change in value. Example: move x:(r2+ 3), N lea (R2) +N Work Around: A no-operation (NOP) will need to be inserted between the two statements. As an aid the assembler will be modified to flag this as a problem.
7.0	Timer and GPIO interrupts may be cleared when clearing other interrupts.	Impact: The timer and GPIO modules may have several interrupts cleared by writing to the same register. Unfortunately, clearing one interrupt can unintentionally result in clearing an interrupt that has occurred between the time the status register is read and written back. Work Around: Do not enable multiple interrupts in a single register.
8.0	PLL Stabilization Time	Impact: Maximum PLL stabilization time is 200ms under worst case (-40°C) conditions. Typical PLL stabilization time remains at 10ms (25°C and above). Work Around: Insert a 200ms delay after power up to allow the PLL to settle or verify the Loss of Lock bits (LCK0 and LCK1) in the PLL Status Register (PLLSR) are set to 1 prior to program execution.
9.0	Erroneous data can occur at the output of the ADC while operating in the sequential conversion mode with an analog input at the ground potential level.	Impact: When operating the DSP56F802 ADC in the sequential mode with two or more analog inputs being actively driven, one channel at ground and the following inputs converted at another value, the expected digitized results for the input that follows the grounded input is sometimes corrupted. If analog inputs never come within 250 mV of ground the problem never occurs. Work Around: Restrict the analog input so that it never comes within 250 mV of ground OR apply a 250 mV offset to analog input signals.
10.0	SCI communication limited to 0 to +85 °C.	Impact: SCI communication is limited to a temperature range of 0 to +85 °C. This effect is due to the inherent frequency variation of the internal relaxation oscillator over temperature combined with frequency tolerances required for SCI communication. Work Around: None

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F802 devices. These parts are devices marked as DSP56F802 or as PC56F802 with datecodes of 0152 or later.

Errata Number	Description	Impact and Work Around
11.0	<p>Problem with Automatic Fault Clearing feature of the PWM block is explained below.</p> <p>The fault pins are used to disable any of the PWM output pins. The PWM output pins can be enabled automatically when the fault pin returns to logic zero and a new PWM half cycle begins if the FMODEx control bit is set to logic one.</p> <p>The only issue with this fault protection mechanism is that when the fault pin returns to logic zero, the PWM channel is enabled at the next IP clock cycle instead of the next PWM half cycle.</p> <p>Note that the PWM channel can always be enabled manually after it is disabled if the FMODEx bit is set to logic zero as described in the User's Manual.</p>	<p>Impact: The PWM automatic fault clearing is used for cycle by cycle current limiting. This requires cycle-based fault input control. Due to this issue the fault input continuously changes the voltage thus making it difficult for output devices to respond.</p> <p>Work Around: None</p>
12.2	<p>The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table.</p>	<p>Impact: The user must clear this bit at startup after a COP reset, or any subsequent resets will use the COP reset vector.</p> <p>Work Around: Clear the COP Reset bit in the SIM STATUS register.</p>
13.3	<p>With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.</p>	<p>Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading.</p> <p>Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant.</p> <p>A more in depth FAQ can be found on the Freescale website. freescale.com</p>

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F802 devices. These parts are devices marked as DSP56F802 or as PC56F802 with datecodes of 0152 or later.

Errata Number	Description	Impact and Work Around
14.3	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	<p>Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt.</p> <p>Work Around(s):</p> <ol style="list-style-type: none"> 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at this exact instant.

Differences Between Errata Sheet Revisions

Chip Rev. A <i>Date codes = \geq 0152</i>
Device cannot meet flash data retention specification of 10 years. Corrected
Low voltage V_{DDA} may cause inaccurate ADC measurement. Corrected
Quad Timer, when in Pulse Output Mode, at IP clock rate yields n+1 pluses. <i>See errata item 1 for additional information.</i>
PWM outputs are not disabled during DEBUG mode. <i>See errata item 2 for additional information.</i>
PFIU address register read returns the wrong value when writing an out-of-row address. <i>See errata item 3 for additional information.</i>
Low Analog input voltages to ADC may not be measured properly. <i>See errata item 4 for additional information.</i>
Optimizing ADC setup. <i>See errata item 5 for additional information.</i>
N register is not available the cycle immediately after it has a value change. <i>See errata item 6 for additional information.</i>
Timer and GPIO interrupts may be cleared when clearing other interrupts. <i>See errata item 7 for additional information.</i>
PLL Stabilization Time. <i>See errata item 8 for additional information.</i>
Erroneous data can occur at the output of the ADC while operating in the sequential conversion mode with an analog input at the ground potential level. <i>See errata item 9 for additional information.</i>
SCI communication limited when using the internal relaxation oscillator as chip clock. <i>See errata item 10 for additional information.</i>
PWM automatic fault clearing issue. <i>See errata item 11 for additional information.</i>
The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table. <i>See errata item 12 for additional information.</i>
With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed. <i>See errata item 13 for additional information.</i>
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written. <i>See errata item 14 for additional information.</i>



How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc. 2005. All rights reserved.

DSP56F802E
Rev. 4
12/2005