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MPC5500 Family Overview

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1 Introduction

The MPC5554 microcontroller (MCU) was the first member of the MPC5500 family of next generation microcontrollers based on Power Architecture ™ technology initially designed for next generation automotive powertrain applications. More devices in the family have been introduced, including the MPC5533, MPC5534, MPC5553, MPC5561, MPC5565, MPC5566, and MPC5567 (all included in this document).

The host processor core of the MPC5500 family devices is compatible with the Power Architecture technology. It is 100 percent user-mode compatible (with floating point library) with the PowerPC ISA. This core has instructions beyond the classic PowerPC ISA, including digital signal processing (DSP) instructions.

The MPC553x and MPC556x devices include the variable length encoding (VLE) option for improved code density.

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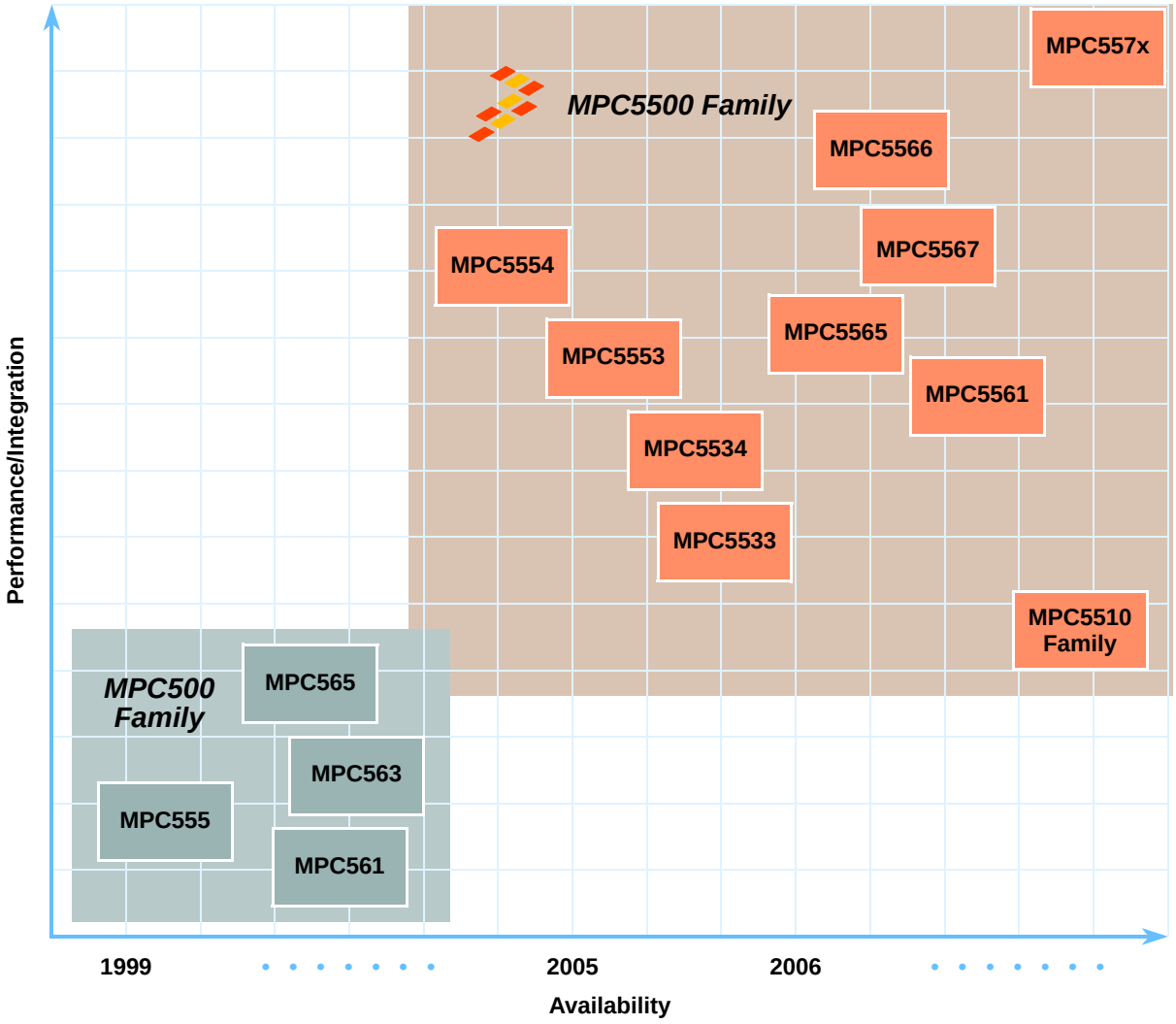
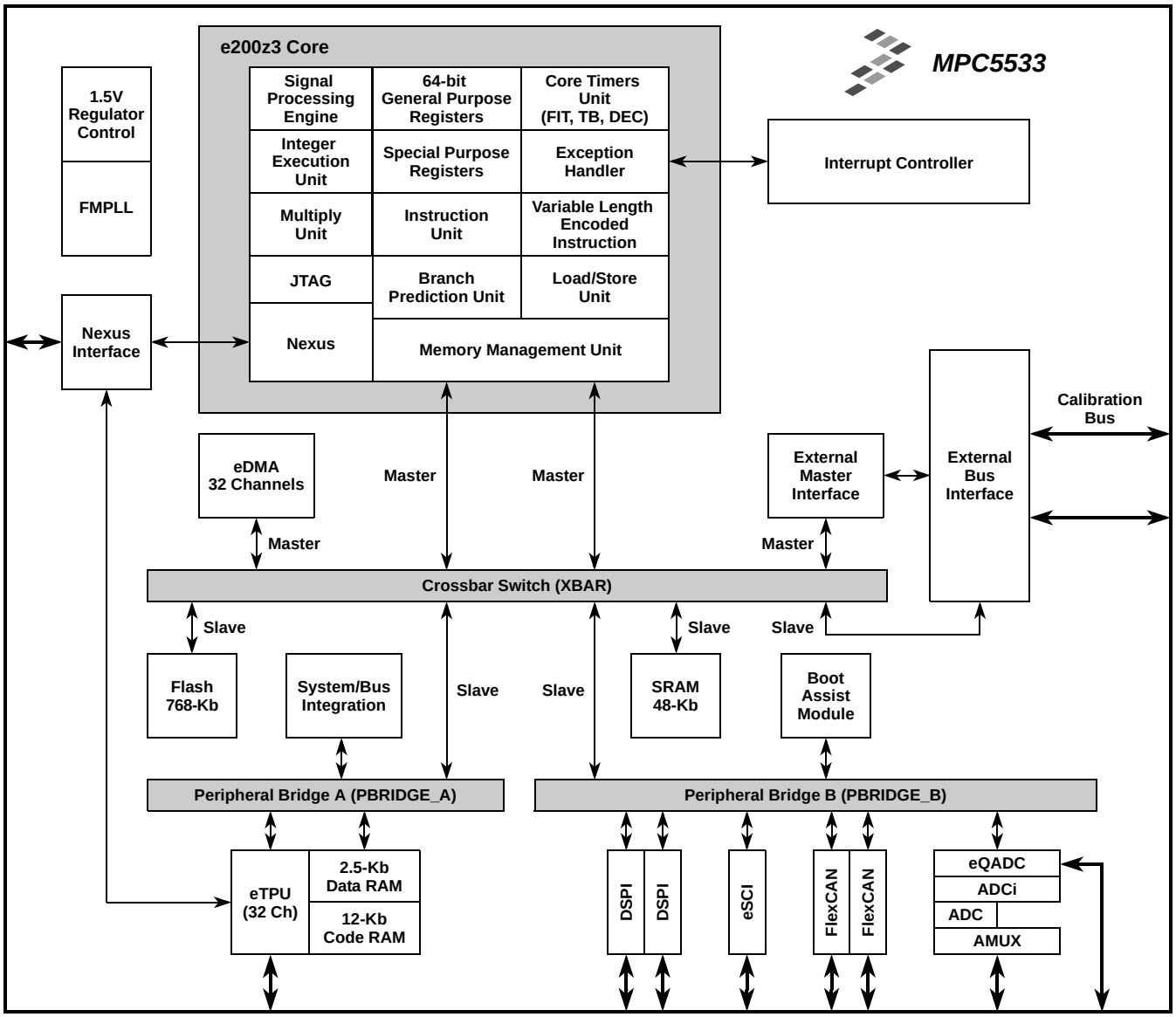


Figure 1. MPC5500 Roadmap



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MPC5500 Device Module Acronyms

CAN – Controller area network (FlexCAN)
DSPI – Deserial/serial peripheral interface
eDMA – Enhanced direct memory access
eQADC – Enhanced queued analog/digital converter
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z3 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 2. MPC5533 Block Diagram

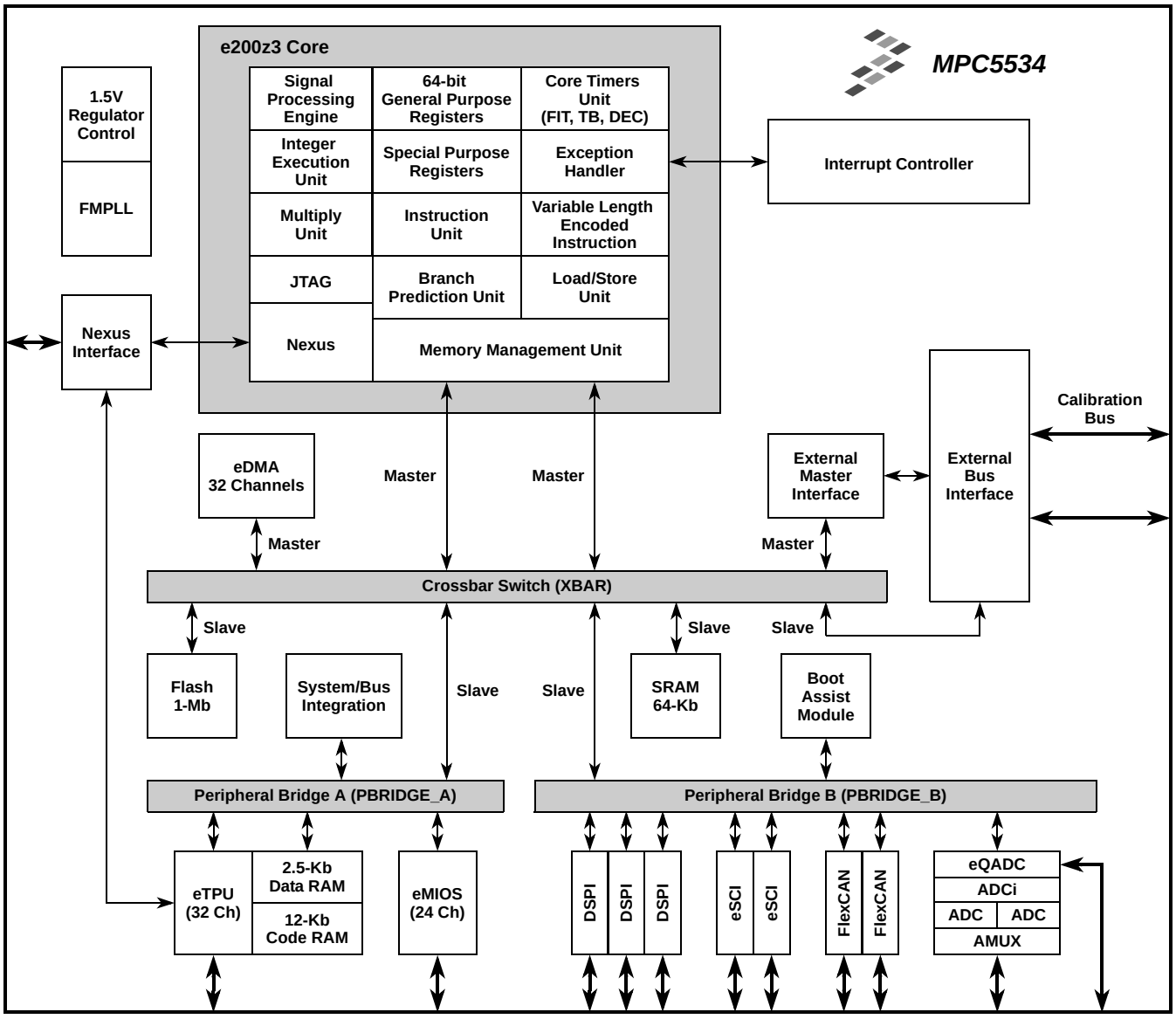

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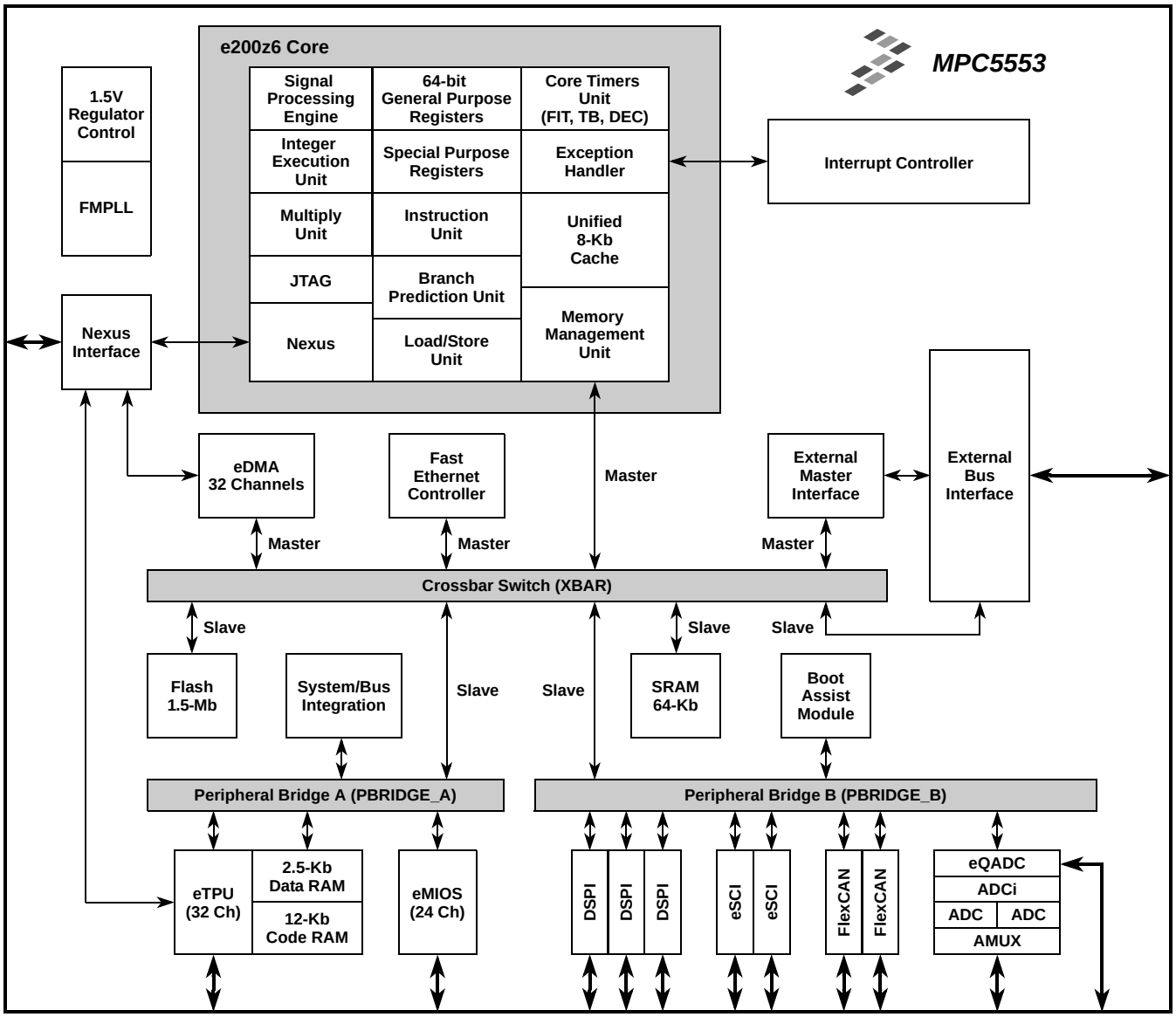
Figure 3. MPC5534 Block Diagram



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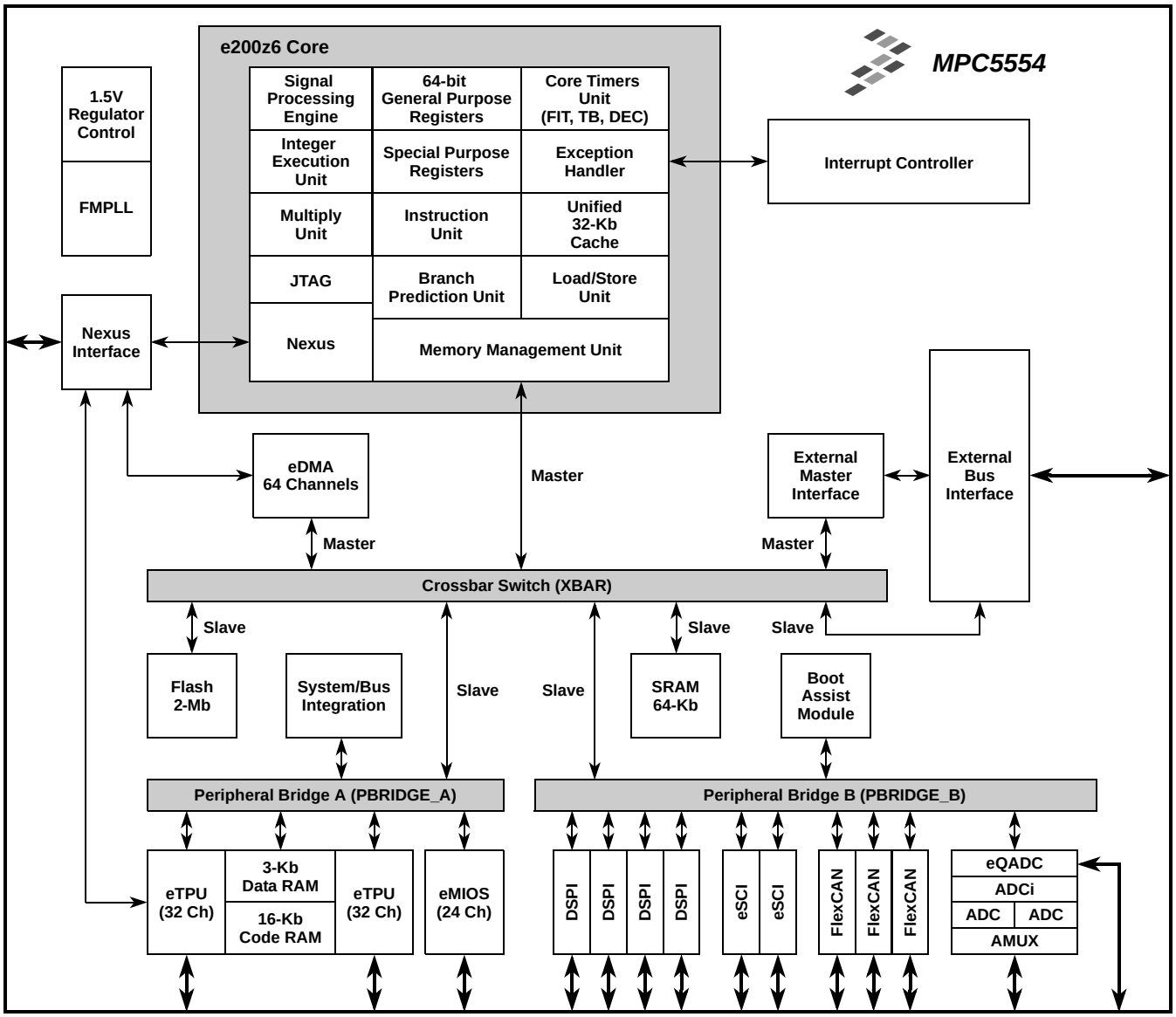
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 4. MPC5553 Block Diagram



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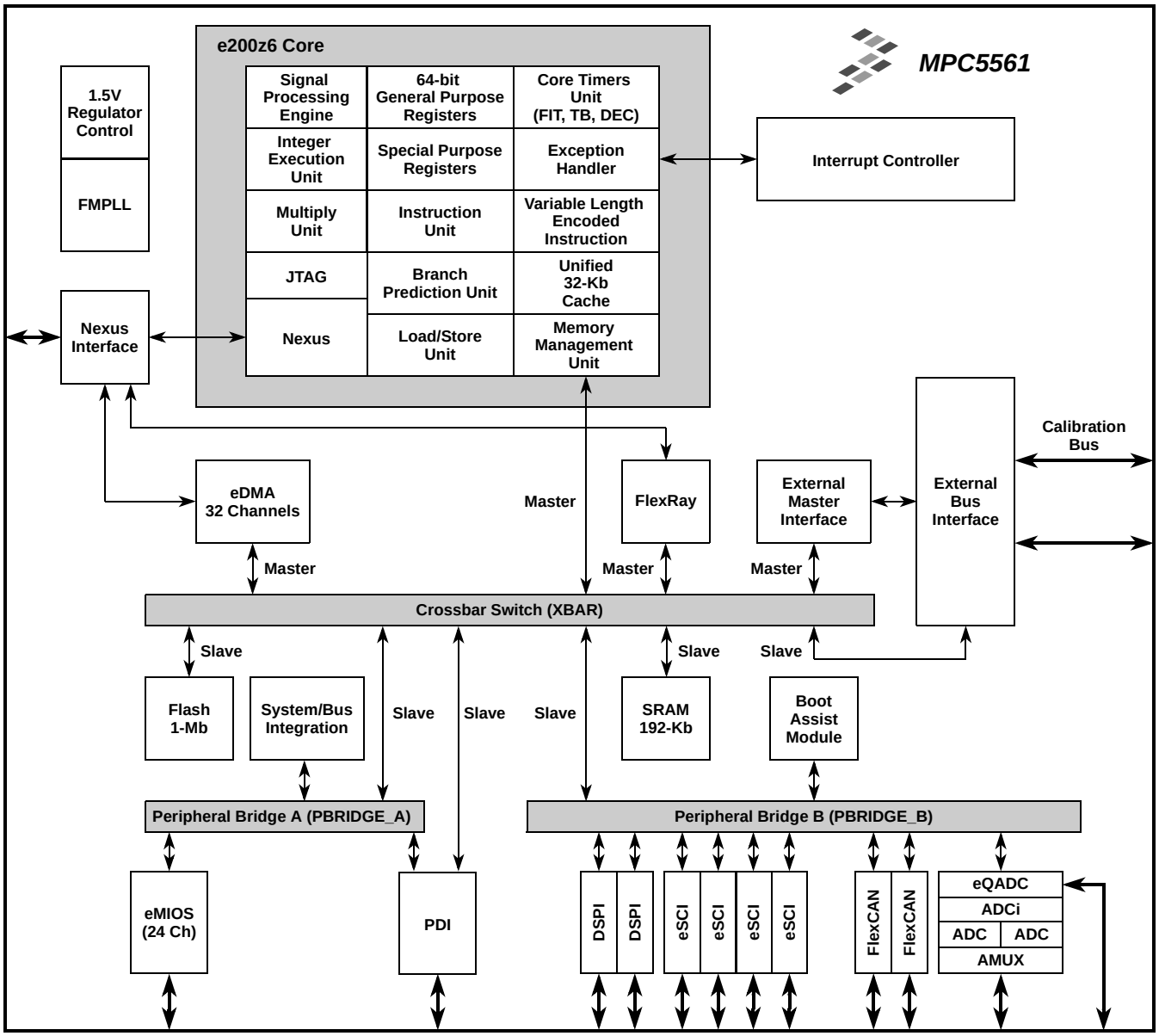
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 5. MPC5554 Block Diagram



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FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
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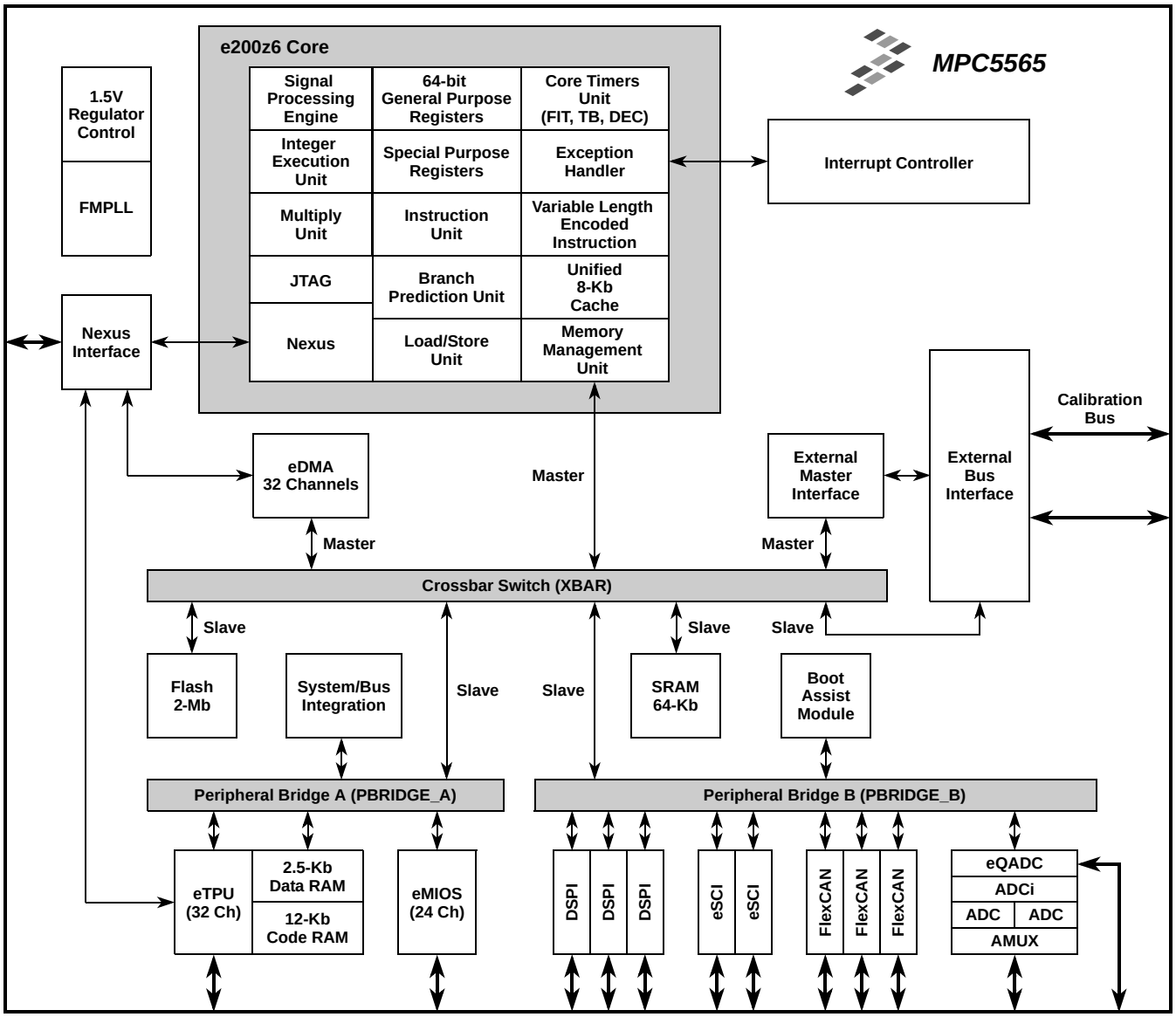
Figure 6. MPC5561 Block Diagram



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MPC5500 Device Module Acronyms

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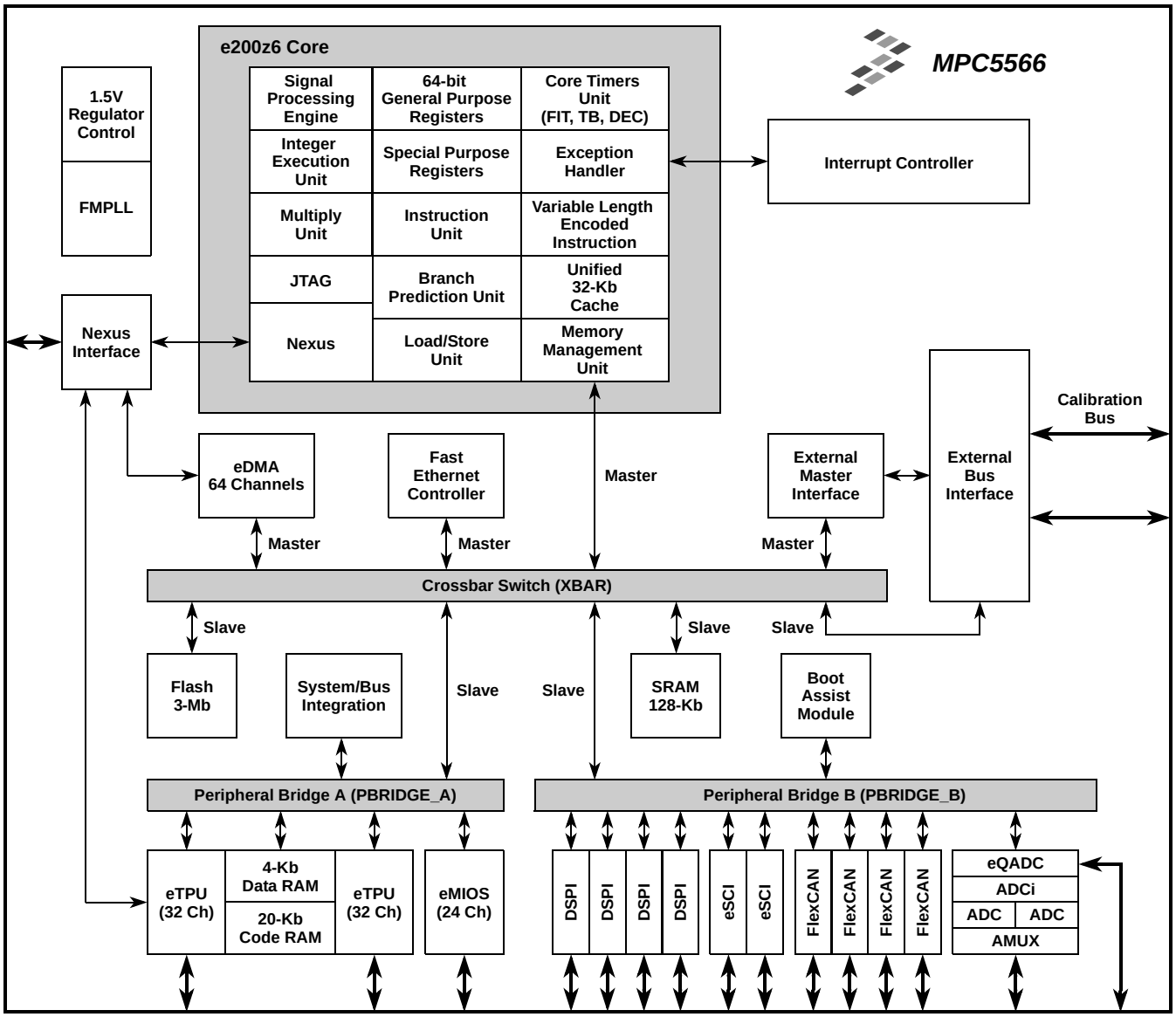
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 7. MPC5565 Block Diagram



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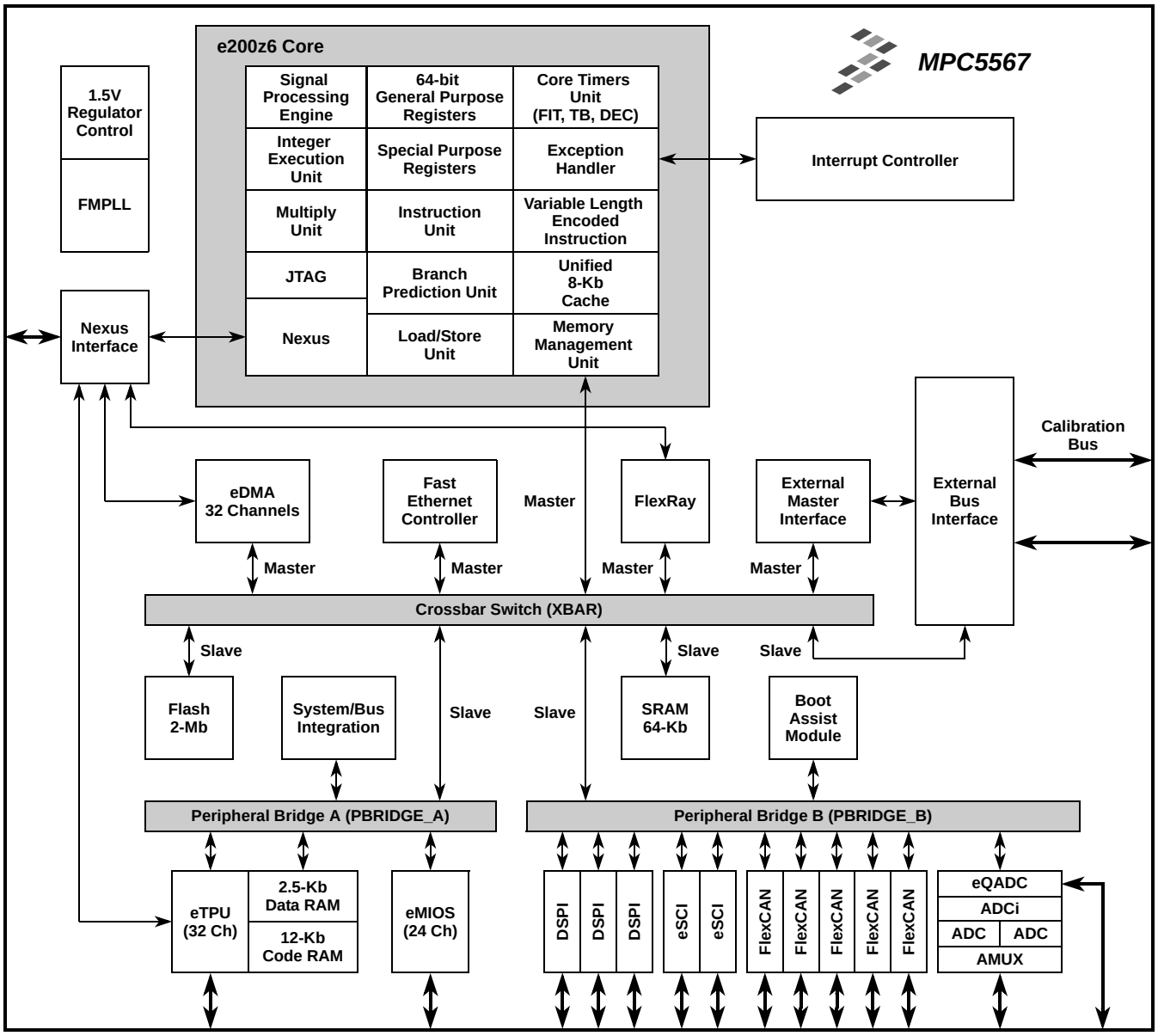
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FMPLL – Frequency modulated phase-locked loop
SRAM – Static RAM

e200z6 Core Component Acronyms

DEC – Decrementer
FIT – Fixed interval timer
TB – Time base
WDT – Watchdog timer

Figure 8. MPC5566 Block Diagram



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MPC5500 Device Module Acronyms

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eTPU	– Enhanced time processing units
FMPLL	– Frequency modulated phase-locked loop
SRAM	– Static RAM

e200z6 Core Component Acronyms

DEC	– Decrementer
FIT	– Fixed interval timer
TB	– Time base
WDT	– Watchdog timer

Figure 9. MPC5567 Block Diagram

2 MPC5500 Family Comparison

Table 1. MPC5500 Family Members

MPC5500 Device		MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
Power Core		e200z3	e200z3	e200z6	e200z6	e200z6	e200z6	e200z6	e200z6
Variable Length Instruction Support		Yes	Yes	No	No	Yes	Yes	Yes	Yes
Cache		None	None	8 Kbyte Unified[1]	32 Kbyte Unified[2]	32 Kbyte Unified[3]	8 Kbyte Unified[1]	32 Kbyte Unified[3]	8 Kbyte Unified[1]
Memory Management Unit (MMU)		16 entry	16 entry	32 entry	32 entry	32 entry	32 entry	32 entry	32 entry
Crossbar		4x5	4x5	4x5	3x5	4x6	3[4]x5	4x5	5x5
Core Nexus		Class 3+ (NZ3C3)	Class 3+ (NZ3C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)	Class 3+ (NZ6C3)
SRAM		48 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	192 Kbyte	64 Kbyte	128 Kbyte	80 Kbyte
Flash	Main Array	768 Kbyte[5]	1 Mbyte[5]	1.5 Mbyte[6]	2 Mbyte[6]	1 Mbyte[6]	2 Mbyte[6]	3 Mbyte[6]	2 Mbyte[6]
	Shadow Block	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte	1 Kbyte
External Bus (EBI)	Data Bus	16-bit[7]	16 bit[7]	32 bit[7]	32 bit[7]	32-bit[7]	32-bit[7]	32-bit[7]	32-bit[7]
	Address Bus	24	24	24	24	26[8]	26[8]	26[8]	26[8]
Calibration Bus		Yes	Yes	Partial	No	Yes	Yes	Yes	Yes
Direct Memory Access (DMA)		32 channel	32 channel	32 channel	64 channel	32 channel	32 channel	64 channel	32 channel
DMA Nexus		None	None	Class 3	Class 3	Class 3	Class 3	Class 3	Class 3
Serial		1	2	2	2	4	2	2	2
	eSCI_A	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_B	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eSCI_C	No	No	No	No	Yes	No	No	No
	eSCI_D	No	No	No	No	Yes	No	No	No
Controller Area Network (CAN)		2	2	2	3	3[9]	3[9]	4[9]	5[9]
	CAN_A	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_B	No	No	No	64 buf	No	64 buf	64 buf	64 buf
	CAN_C	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf	64 buf
	CAN_D	No	No	No	No	No	No	64 buf	64 buf
	CAN_E	No	No	No	No	No	No	No	64 buf
SPI		2	3	3	4	3	3	4	3
	DSPI_A	No	No	No	Yes	No	No	Yes	No
	DSPI_B	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DSPI_D	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
eMIOS		0 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel	24 channel

Table 1. MPC5500 Family Members (continued)

MPC5500 Device	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
eTPU	32 channel	32 channel	32 channel	64 channel	0 channel	32 channel	64 channel	32 channel
eTPU_A	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
eTPU_B	No	No	No	Yes	No	No	Yes	No
Code Memory	12 Kbyte	12 Kbyte	12 Kbyte	16 Kbyte	0 Kbyte	12 Kbyte	20 Kbyte	12 Kbyte
Parameter RAM	2.5 Kbyte	2.5 Kbyte	2.5 Kbyte	3 Kbyte	0 Kbyte	2.5 Kbyte	4 Kbyte	2.5 Kbyte
Nexus	Class 3	Class 3	Class 3	Class 3	No	Class 3	Class 3	Class 3
Interrupt Controller	178 channel	210 channel	210 channel	300 channel	231 channel	231 channel	329 channel	281 channel
Analog to Digital Converter (eQADC)	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel	40 channel
ADC_0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC_1	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast Ethernet Controller (FEC)	No	No	Yes[10]	No	No	No	Yes[10]	Yes[11]
FlexRay	No	No	No	No	Yes	No	No	Yes
FlexRay Nexus	No	No	No	No	Class 3	No	No	Class 3
Phase Lock Loop (PLL)	FM	FM	FM	FM	FM	FM	FM	FM
Maximum System Frequency[12]	80 MHz	80 MHz	132 MHz	132 MHz	132 MHz	132 MHz	132 MHz	132 MHz
Crystal Range	8–20 MHz	8–20 MHz	8–20 MHz	8–20 MHz	8–40 MHz	8–20 MHz	8–20 MHz	8–40 MHz
Voltage Regulator Controller (VRC)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

NOTES:
1 2-way associative
2 8-way associative
3 4-way or 8-way associative
4 The actual crossbar is implemented as a 5x5 crossbar with two unused ports
5 16-byte flash page size for programming
6 32-byte flash page size for programming
7 May not be externally available in some package configurations
8 Either ADDR[8:31] or ADDR[6:29] can be selected.
9 Updated FlexCAN module with optional individual receive filters
10 The FEC signals are shared with data bus pins DATA[16:31]
11 The FEC signals are shared with the calibration bus
12 Initial automotive temperature range qualification

3 MPC5500 Family Memory Map

This section describes the memory map for the MPC5500 devices discussed in this document. All addresses in the device, including those that are reserved, are identified in the tables. The addresses represent the physical addresses assigned to each IP module. Logical addresses are translated by the memory management unit (MMU) into physical addresses.

Under software control of the MMU, the logical addresses allocated to IP blocks may be changed on a minimum of a 4-Kbyte boundary. Peripheral blocks may be redundantly mapped. The customer must use the MMU to prevent corruption.

Table 2 shows a detailed memory map.

Table 2. Detailed MPC5500 Family Memory Map

Address Range[1]	Allocated Size	Used Size	Use	MPC5532	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
0x0000_0000–0x000B_FFFF	768 Kbyte	768 Kbyte	Flash Array	√	√	√	√	√	√	√	√	√
0x000C_0000–0x000F_FFFF	256 Kbyte	256 Kbyte	Flash Array	√		√	√	√	√	√	√	√
0x0010_0000–0x0017_FFFF	512 Kbyte	512 Kbyte	Flash Array				√	√		√	√	√
0x0018_0000–0x001F_FFFF	512 Kbyte	512 Kbyte	Flash Array					√		√	√	√
0x0020_0000–0x002F_FFFF	1 Mbyte	1 Mbyte	Flash Array								√	
0x0030_0000–0x00FF_FBFF	~13 Mbyte	N/A	Reserved									
0x00FF_FC00–0x00FF_FFFF	1024 bytes	1024 bytes	Flash Shadow Block	√	√	√	√	√	√	√	√	√
0x0100_0000–0x1FFF_FFFF	496 Mbyte	2 Mbyte	Emulation Mapping of Flash Array	√	√	√	√	√	√	√	√	√
0x2000_0000–0x3FFF_FFFF	512 Mbyte	N/A	External Memory	√	√	√	√	√	√	√	√	√
0x4000_0000–0x4000_7FFF	32 Kbyte	32 Kbyte	SRAM Array, Standby Powered	√	√	√	√	√	√	√	√	√
0x4000_8000–0x4000_BFFF	16 Kbyte	16 Kbyte	SRAM Array	√	√	√	√	√	√	√	√	√
0x4000_C000–0x4000_FFFF	16 Kbyte	16 Kbyte	SRAM Array			√	√	√	√	√	√	√
0x4001_0000–0x4001_3FFF	16 Kbyte	16 Kbyte	SRAM Array						√		√	√
0x4001_4000–0x4001_FFFF	48 Kbyte	48 Kbyte	SRAM Array						√		√	
0x4002_0000–0x4002_FFFF	64 Kbyte	64 Kbyte	SRAM Array						√			
0x4003_0000–0x9FFF_FFFF	(<15 Gb)	N/A	Reserved									
0xA000_0000–0xBFFF_FFFF	512 Mbyte	256 Mbyte	Parallel Digital Interface						√			
Bridge A Peripherals												
0xC000_0000–0xC3EF_FFFF	63 Mbyte	N/A	Reserved									
0xC3F0_0000–0xC3F0_3FFF	16 kbyte	16 kbyte	Bridge A Registers	√	√	√	√	√	√	√	√	√
0xC3F0_4000–0xC3F7_FFFF	496 Kbyte	N/A	Reserved									
0xC3F8_0000–0xC3F8_3FFF	16 Kbyte	20 kbyte	FMPLL	√	√	√	√	√	√	√	√	√
0xC3F8_4000–0xC3F8_7FFF	16 Kbyte	48 Kbyte	External Bus Interface (EBI) Configuration	√	√	√	√	√	√	√	√	√
0xC3F8_8000–0xC3F8_BFFF	16 Kbyte	28 Kbyte	Flash Configuration	√	√	√	√	√	√	√	√	√
0xC3F8_C000–0xC3F8_FFFF	16 Kbyte	N/A	Reserved									
0xC3F9_0000–0xC3F9_3FFF	16 Kbyte	2.5 Kb	System Integration Unit (SIU)	√	√	√	√	√	√	√	√	√
0xC3F9_4000–0xC3F9_FFFF	48 Kbyte	N/A	Reserved									
0xC3FA_0000–0xC3FA_3FFF	16 Kbyte	1056	Modular Timer System (eMIOS)	√		√	√	√	√	√	√	√
0xC3FA_4000–0xC3FA_7FFF	16 Kbyte	1056	Modular Timer System (eMIOS_B)[3]									
0xC3FA_8000–0xC3FB_FFFF	96 Kbyte	N/A	Reserved									
0xC3FC_0000–0xC3FC_3FFF	16 Kbyte	3 Kbyte	Enhanced Time Processing Unit (eTPU) Registers	√	√	√	√	√		√	√	√
0xC3FC_4000–0xC3FC_7FFF	16 Kbyte	N/A	Reserved									

Table 2. Detailed MPC5500 Family Memory Map (continued)

Address Range[1]	Allocated Size	Used Size	Use	MPC5532	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
0xC3FC_8000–0xC3FC_09FF	16 Kbyte	2.5 Kbyte	eTPU Shared Data Memory (Parameter RAM)	√	√	√	√	√		√	√	√
0xC3FC_8A00–0xC3FC_8BFF		0.5 Kbyte						√			√	
0xC3FC_8C00–0xC3FC_8FFF		1 Kbyte									√	
0xC3FC_9000–0xC3FC_BFFF			eTPU Parameter RAM Reserved									
0xC3FC_C000–0xC3FC_FFFF	16 Kbyte	3 Kbyte	eTPU Shared Data Memory (Parameter RAM) mirror	√	√	√	√	√		√	√	√
0xC3FD_0000–0xC3FD_2FFF	20 Kbyte	12 Kbyte	eTPU Shared Code RAM (12K,16K, or 20K)	√	√	√	√	√		√	√	√
0xC3FD_3000–0xC3FD_3FFF		4 Kbyte						√			√	
0xC3FD_4000–0xC3FD_4FFF		4 Kbyte									√	
0xC3FD_5000–0xC3FF_7FFF	156 Kbyte	N/A	Reserved									
0xC3FF_8000–0xC3FF_BFFF	16 Kbyte	N/A	Reserved									
0xC3FF_C000–0xC3FF_FFFF	16 Kbyte	N/A	Reserved									
0xC400_0000–0xDFFF_FFFF	(448 Mbyte)	N/A	Reserved									
Bridge B Peripherals												
0xE000_0000–0xFBFF_FFFF	(448 Mbyte)	N/A	Reserved									
0xFC00_0000–0xFFEF_FFFF	63 Mbyte	N/A	Reserved									
0xFFF0_0000–0xFFF0_3FFF	16 Kbyte	N/A	Bridge B Registers	√	√	√	√	√	√	√	√	√
0xFFF0_4000–0xFFF0_7FFF	16 Kbyte	N/A	Crossbar (XBAR)	√	√	√	√	√	√	√	√	√
0xFFF0_8000–0xFFF0_FFFF	32 Kbyte	N/A	Reserved									
0xFFF1_0000–0xFFF3_FFFF	192 Kbyte	N/A	Reserved									
0xFFF4_0000–0xFFF4_3FFF	16 Kbyte	N/A	ECSM	√	√	√	√	√	√	√	√	√
0xFFF4_4000–0xFFF4_7FFF	16 Kbyte	N/A	DMA Controller 2 (eDMA)	√	√	√	√	√	√	√	√	√
0xFFF4_8000–0xFFF4_BFFF	16 Kbyte	N/A	Interrupt Controller (INTC)	√	√	√	√	√	√	√	√	√
0xFFF4_C000–0xFFF4_C3FF	1 Kbyte	N/A	Fast Ethernet Controller (FEC)[2]				√				√	√
0xFFF4_C400–0xFFF4_FFFF	15 Kbyte	N/A	Reserved									
0xFFF5_0000–0xFFF7_FFFF	192 Kbyte	N/A	Reserved									
0xFFF8_0000–0xFFF8_3FFF	16 Kbyte	164	Enhanced Queued Analog-to-Digital Converter (eQADC)	√	√	√	√	√	√	√	√	√
0xFFF8_4000–0xFFF8_7FFF	16 Kbyte	164	Enhanced Queued Analog-to-Digital Converter (eQADC_B)[3]									
0xFFF8_8000–0xFFF8_FFFF	32 Kbyte	N/A	Reserved									
0xFFF9_0000–0xFFF9_3FFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_A)					√			√	
0xFFF9_4000–0xFFF9_7FFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_B)			√	√	√	√	√	√	√
0xFFF9_8000–0xFFF9_BFFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_C)	√	√	√	√	√	√	√	√	√
0xFFF9_C000–0xFFF9_FFFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_D)	√	√	√	√	√	√	√	√	√

Table 2. Detailed MPC5500 Family Memory Map (continued)

Address Range[1]	Allocated Size	Used Size	Use	MPC5532	MPC5533	MPC5534	MPC5553	MPC5554	MPC5561	MPC5565	MPC5566	MPC5567
0xFFFA_0000–0xFFFA_3FFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_E)[3]									
0xFFFA_4000–0xFFFA_7FFF	16 Kbyte	200	Deserial Serial Peripheral Interface (DSPI_F)[3]									
0xFFFA_8000–0xFFFA_FFFF	32 Kbyte	N/A	Reserved									
0xFFFB_0000–0xFFFB_3FFF	16 Kbyte	44	Serial Communications Interface (SCI_A)	√	√	√	√	√	√	√	√	√
0xFFFB_4000–0xFFFB_7FFF	16 Kbyte	44	Serial Communications Interface (SCI_B)	√		√	√	√	√	√	√	√
0xFFFB_8000–0xFFFB_BFFF	16 Kbyte	44	Serial Communications Interface (SCI_C)						√			
0xFFFB_C000–0xFFFC_FFFF	16 Kbyte	44	Serial Communications Interface (SCI_D)						√			
0xFFFC_0000–0xFFFC_3FFF	16 Kbyte	1152	Controller Area Network (FlexCAN_A)	√	√	√	√	√	√	√	√	√
0xFFFC_4000–0xFFFC_7FFF	16 Kbyte	1152	Controller Area Network (FlexCAN_B)					√		√	√	√
0xFFFC_8000–0xFFFC_BFFF	16 Kbyte	1152	Controller Area Network (FlexCAN_C)		√	√	√	√	√	√	√	√
0xFFFC_C000–0xFFFC_FFFF	16 Kbyte	1152	Controller Area Network (FlexCAN_D)								√	√
0xFFFD_0000–0xFFFD_3FFF	16 Kbyte	1152	Controller Area Network (FlexCAN_E)									√
0xFFFD_4000–0xFFFD_FFFF	48 Kbyte	N/A	Reserved									
0xFFFE_0000–0xFFFE_3FFF	16 Kbyte	2 kbyte	FlexRay						√			√
0xFFFE4000–0xFFFE_7FFF	16 Kbyte		Reserved									
0xFFFE_8000–0xFFFE_BFFF	16 Kbyte		Parallel Digital Interface						√			
0xFFFF_C000–0xFFFF_FFFF[4]	16 Kbyte	16 Kbyte	Boot Assist Module (BAM)	√	√	√	√	√	√	√	√	√

NOTES:
1 If allocated size is greater than used size, the base address for the module is the lowest address of the listed address range, unless noted otherwise.
2 The fast Ethernet controller (FEC) uses different pins on the MPC5553/MPC5566 and the MPC5567.
3 Reserved for future compatibility. No device is currently defined that uses these regions.
4 BAM address range is configured so that 4 kbytes BAM occupies 0xFFFF_F000-0xFFFF_FFFF.

4 Package Options

The members of the MPC5500 family are all pin-compatible, but the different devices are available in a range of packages. Not all features are available in the smaller packages or on all devices.

Table 3. Device Package Options

Device	208 MAPBGA[1]	324 PBGA	416 PBGA	496 CSP[2]	Calibration Bus
MPC5533	Yes[3,4]	No[7]	No	Yes	Yes
MPC5534	Yes[3,4]	Yes[3]	No	Yes	Yes
MPC5553	Yes[4]	Yes[3]	Yes[5]	Yes	Partial[6]
MPC5554	No	No	Yes[3]	Yes	No
MPC5561	No	Yes	No	No	No
MPC5565	No[7]	Yes[3,4]	No[4,7]	Yes	Yes
MPC5566	No	No	Yes[3]	Yes	Yes
MPC5567	No[7]	Yes[4]	Yes[3,5]	Yes	Yes
Nexus port availability	4-bit MDO Only	4 or 12-bit MDO	4 or 12-bit MDO	4 or 12-bit MDO	
Bus availability	None (OE and CS0 available for GPIO)	16-bit data / 20-bit address 4 chip selects[8]	32-bit data / 24/26-bit address 4 chip selects	32-bit data / 24/26-bit address 4 chip selects	
Calibration bus availability	None	None	None	16-bit data / 21/19-bit address 1/3 chip selects	
Analog channels	34	40	40	40	
Ethernet available[9]	No	No	Yes	—	

NOTES:
1. The 208 MAPBGA package is not available through distribution. If demand warrants, consult factory on availability.
2. The VertiCal CSP package is a 496 ball device mounted on a sub-assembly to fit into the 208, 324, or 416 ball footprint. It is not available as a standalone packaged device.
3. Predominate package. Though all packages may be available, the predominate package is the package in which most of the volume deliveries are expected.
4. Not available to distribution customers.
5. Predominate package for Ethernet use.
6. The MPC5553 lose use of 16 data bus signals in the 416 ball sub-assembly for the calibration data bus. The address bus is shared between the calibration bus and the normal system bus. Note: the fast Ethernet controller (FEC) requires these same 16 data bus signals on this devices. On the MPC5567, the FEC is shared with the calibration bus.
7. Depending on demand, consult factory for availability,
8. Up to 24 bits of address with zero chip selects can optionally be selected.
9. On devices that include Ethernet only.

4.1 416 PBGA Ball Maps

4.1.1 MPC5554/MPC5566

Figure 10 is a pinout for the MPC5554/MPC5566 416 PBGA package, Revision A.

NOTE:

On the MPC5554, Ball J23 is VDDEH6. On the MPC5566, ball J23 is VDDEH10.

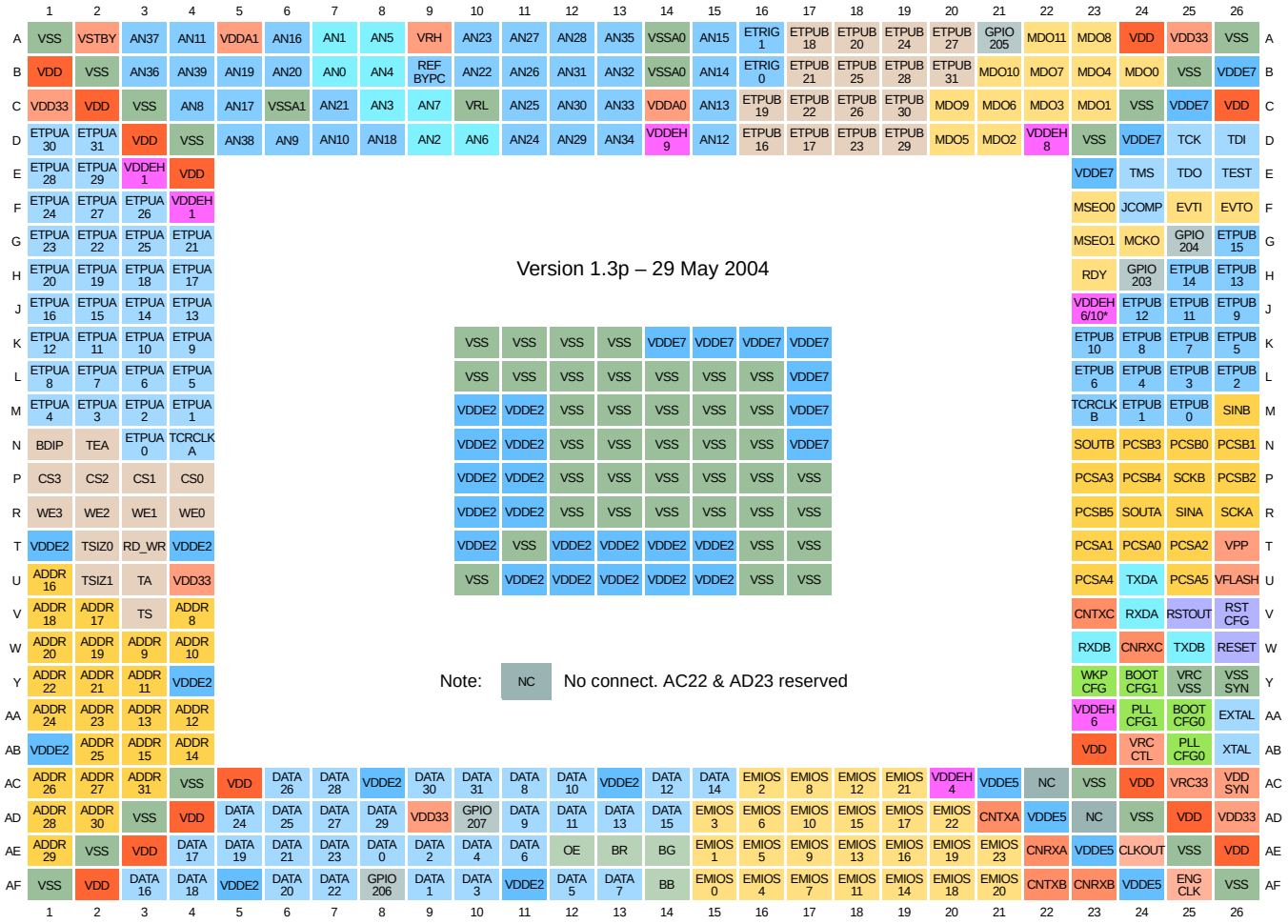

Figure 10. MPC5554/MPC5566 416 PBGA Ball Map Diagram

4.1.2 MPC5553

Figure 11 is a pinout for the MPC5553 416 PBGA package. The MPC5553 and the MPC5554/MPC5565/MPC5566 are pin-compatible; however, the MPC5553 ball map is shown here to highlight the balls not connected to any signal on the MCP5553 (the eTPUB[0:31] and TSIZ[0:1]). The alternate Ethernet signals that are multiplexed with the data bus are not shown for the MPC5553.

NOTE

Some pins have names that include functions unavailable on all family members. For example, ball R25 of the 416 BGA package is named ‘SINA’, but the MPC5553 does not have a DSPI_A module. In this case, the SINA pin can only be used for its alternate functions of GPIO94 or PCSC2. See the specific device reference manual for functions available on each device in the family.

If the MPC5534 were available in the 416 PBGA package, then it would also be missing the following signals: $\overline{WE2}$, $\overline{WE3}$, ADDR[8:11], and $\overline{TEA}$.

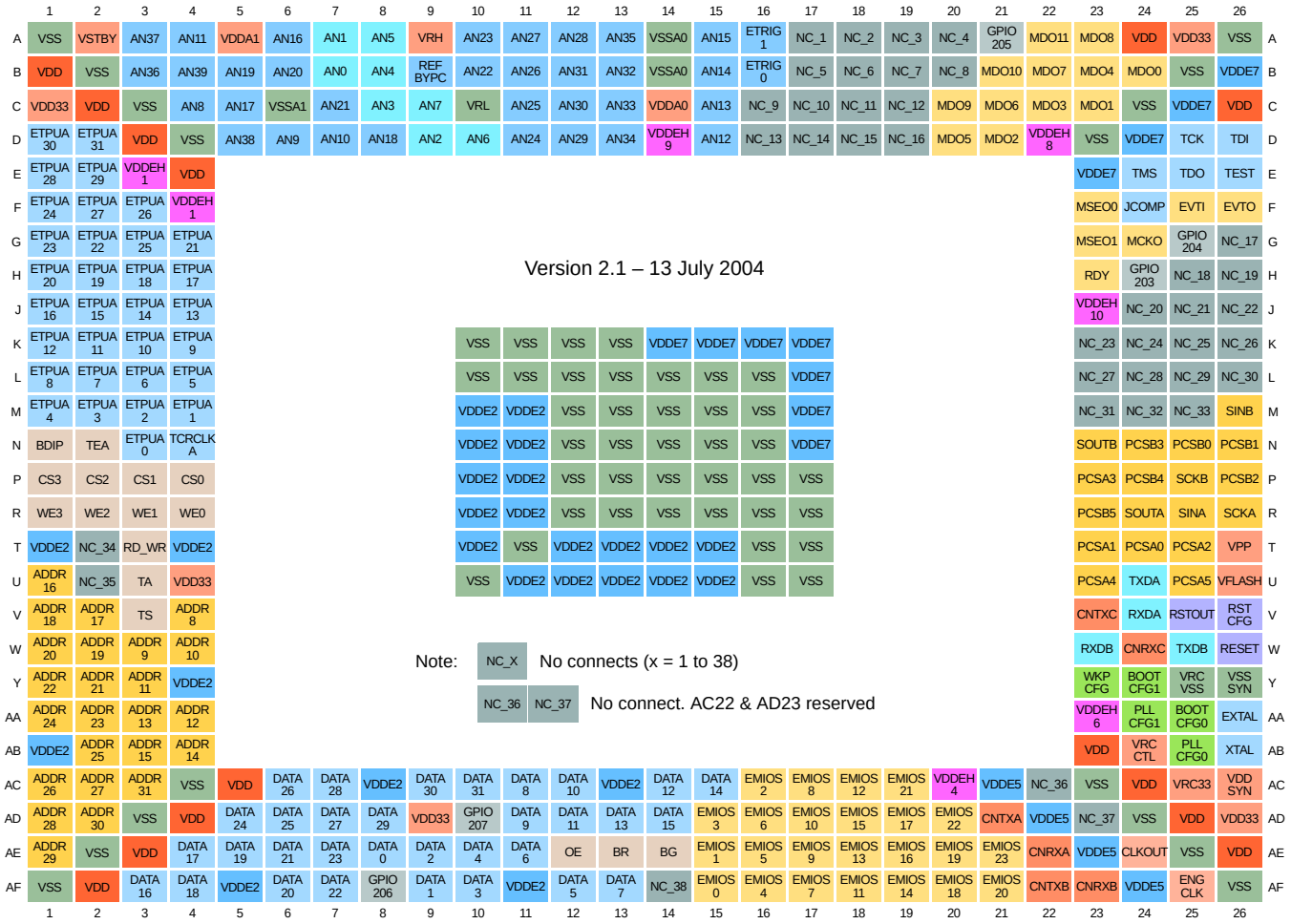

Figure 11. MPC5553 416 PBGA Ball Map Diagram

4.1.3 MPC5567

Figure 11 is a pinout for the MPC5567 416 PBGA package. The MPC5567 and the MPC5553/MPC5554 are pin-compatible; however, the MPC5567 ball map is shown here to highlight the balls not connected to any signals and the balls used for Ethernet.

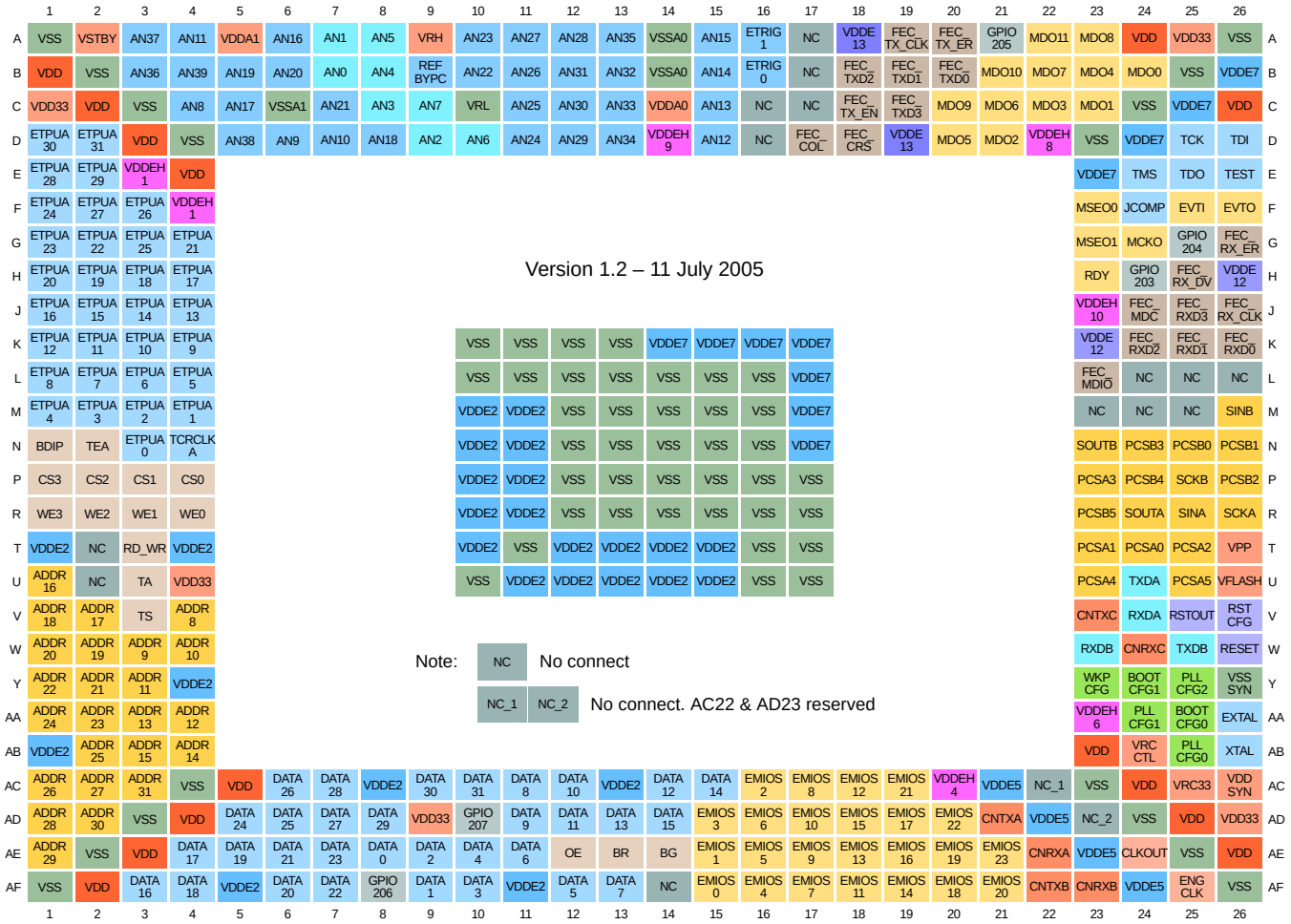

Figure 12. MPC5567 416 PBGA Ball Map Diagram

NOTE

Ball Y25 changes from VRCVSS on all other MPC5500 devices (currently defined) to PLLCFG2 on the MPC5567. PLLCFG2 is required to support a 40-MHz clock option for the FlexRay.

4.2 324 PBGA Ball Maps

4.2.1 MPC5533/MPC5534/MPC5553/MPC5561/MPC5565

Figure 13 is a pinout for the MPC5533/MPC5534/MPC5553/MPC5561/MPC5565 324 PBGA package.

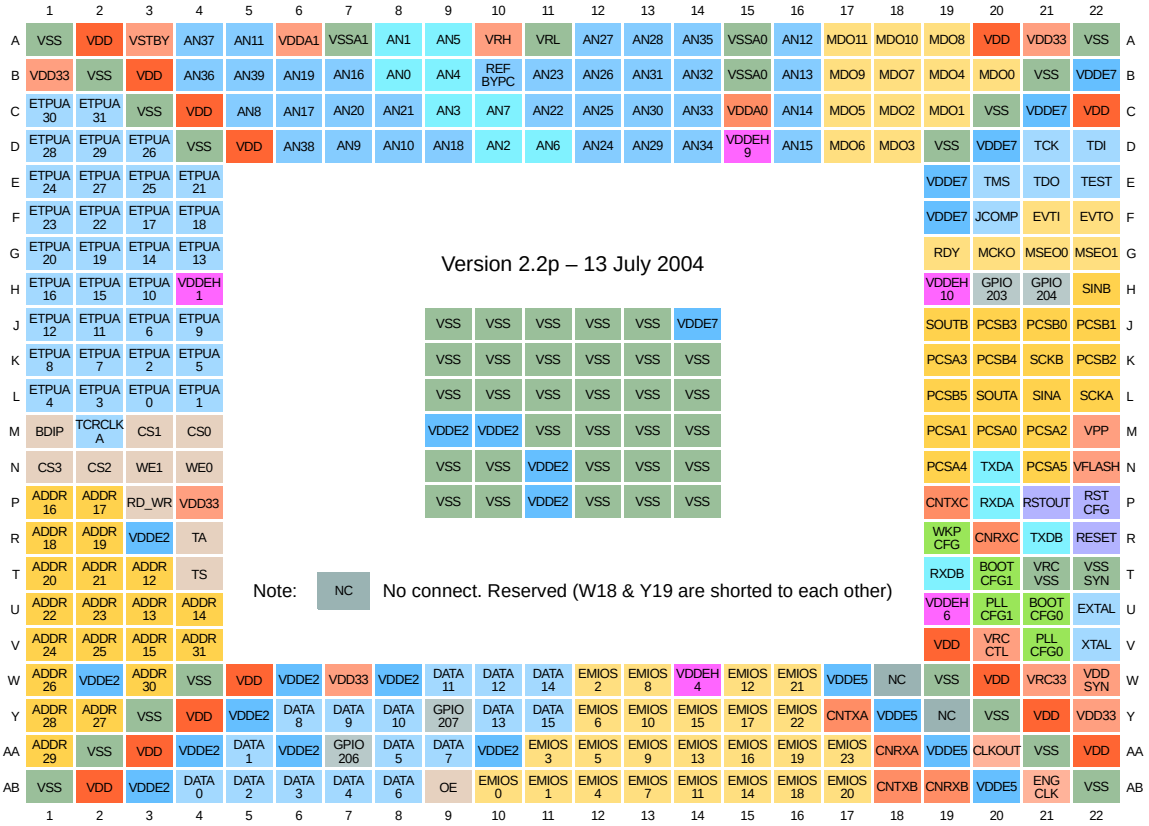

Figure 13. MPC5533/MPC5534/MPC5553/MPC5565 324 PBGA Ball Map Diagram

On the MPC5561 and MPC5567 ball T21 is PLLCFG2 instead of VRCVSS. PLLCFG2 is required to support a 40 MHz clock option for the FlexRay.

4.3 208 MAP BGA Ball Map

4.3.1 MPC5533/MPC5534/MPC5553/MPC5565/MPC5566/MPC5567

Figure 14 is a pinout for the MPC5533/MPC5534/MPC5553/MPC5565/MPC5567 208 MAP PBGA package.

NOTE

VDDEH10 and VDDEH6 are connected internally on the 208-ball package and are listed as VDDEH6.

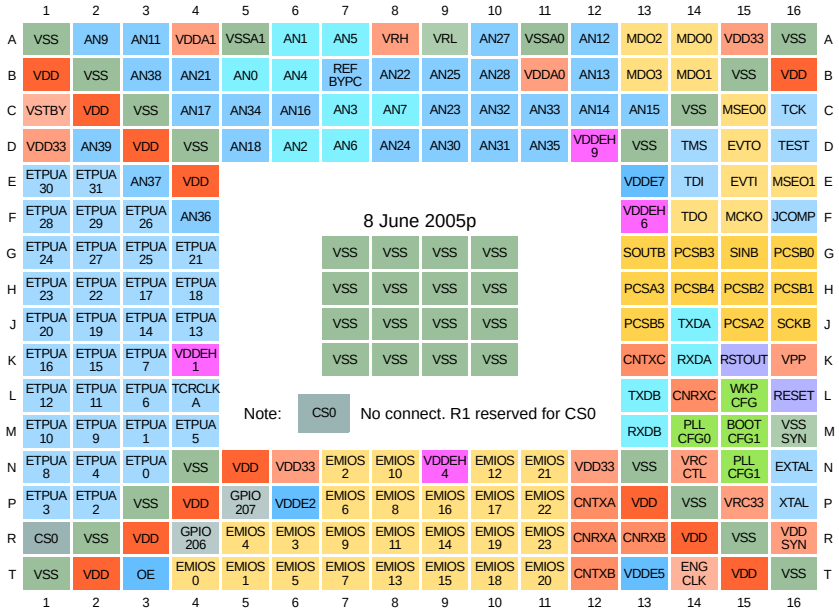

Figure 14. MPC5534/MPC5553/MPC5565/MPC5567 208 PBGA Ball Map Diagram

Appendix A: Revision History

Table 4 is a revision history for this document.

Table 4. Revision History

Revision Number	Substantive Changes
0	Initial release.
A.1	• Added Section 11, "MPC5554 Evaluation Board Availability." (now removed) • Changed TCRCLKB(IRQ6) to TCRCLKA(IRQ) in Table 16.(now removed) • Changed NC to eTPUB24 and NC to TCRCLKB in Table 17.(now removed)
A.4	• First Confidential release for customers.
A.5	• Added MPC5566. Corrected memory map for MPC5565 and MPC5567 showing flash size and eTPU shared RAM size. • Corrected MPC5565 and MPC5567 block diagrams - only 1 eTPU each. • Re-ordered the block diagrams and tables to put into devices into numeric order, instead of introduction order. • Added place holder for MPC557x future devices in the device roadmap. • Added MPC5533 block diagram. • L2 SRAM renamed just SRAM. • Corrected SINA ball number in Section 4.1.2. • Modified ordering of device introduction schedules in Figure 1 MPC5500 roadmap figure. • Added cache associativity to Table 1 • Renamed all pinout diagrams to ball map diagrams for consistency. • Removed eMIOS on MPC5533. Corrected eDMA channels on MPC5533, MPC5534, MPC5565, MPC5567. Corrected number of interrupt channels in Table 1. • Corrected FlexCAN memory map for MPC5533, MPC5534, and MPC5553 in Table 2. • MPC5567 ball map updated for VDDE13. • Cache associativity added to feature table. • Review comment - MPC5566 has 64 eTPU channels. • Updated introduction paragraph to reference all parts covered in this document. • Changed MPC5567 SRAM size to 80K from 64K for revision A of the MPC5567.

Table 4. Revision History (continued)

Revision Number	Substantive Changes
A.6	• Changed MPC5565 416 BPGA package to consult factory—tooling based on forecasted demand. Notes added to 208 MAPBGA and some other configurations that they will not be available through the distribution channel.
A.6.1	• Reviewed by BB, LW, and VG. Editorial and formatting edits by AE. Figures redrawn.
0	• First Public Release
1	• Removed second ADC from MPC5533 block diagram (Figure 2). • Updated package availability for family. On package options that were previously as Yes (available) with the footnotes 4 (Not available to distribution customers) or 7 (Depending on demand, consult factory) changed to “No - consult factory for availability”. • Corrected Ball J23 (VDDEH10) on 416 MPC5553, MPC5566, and MPC5567 Ball Map. • Corrected VDDEH10 on 324 (H19) ball maps. • Corrected eTPUA6 (ball L3) in the 208 MAPBGA (Figure 14). • Added MPC5561 to family comparison (Table 1) and memory map (Table 2). Added MPC5561 block diagram. • Added note on MPC5565 crossbar size in comparison table (Table 1) to indicate that there are 5 ports with 2 unused. • Updated references from PowerPC to Power. • Added reference for PLLCFG2 for the 324 Ball Map for the MPC5567 and MPC5561. • Updated roadmap timing, including the MPC5561 part number, added MPC5510 Family. • Deleted 324 package options for MPC5533. Small editorial and formatting edits by SF.

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