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Introduction

This document describes the differences between the MC68HC08AB16A (HC08AB16A) and the MC68HC908AB32 (HC908AB32), and the requirements/considerations for converting code from the HC08AB16A to the HC908AB32.

Differences Between the Devices

The HC908AB32 is the FLASH version of the HC08AB16A. [Table 1](#) shows the differences between the two parts.

Table 1. Differences Between the Devices

	MC68HC08AB16A	MC68HC908AB32
RAM	512 bytes RAM (\$50 – \$24F)	1024 bytes RAM (\$50 – \$44F)
User memory	16,384 bytes ROM (\$BE00 – \$FDFF)	32, 256 bytes FLASH (\$8000 – \$FDFF)
User vectors	48 bytes ROM (\$FFD0 – \$FFFF)	48 bytes FLASH (\$FFD0 – \$FFFF)
Registers at \$001F and \$003F	Mask Option Registers ⁽¹⁾ \$001F – MORA \$003F – MORB	Configuration registers ⁽²⁾ \$001F – CONFIG1 \$003F – CONFIG2
Bit 4 at \$003F	EEMONSEC bit: Enable EEPROM security in monitor mode	Not used: Bit is reserved

Table 1. Differences Between the Devices (Continued)

	MC68HC08AB16A	MC68HC908AB32
Bit 5 at \$003F	EESEC bit: Enable EEPROM security	Not used: Bit is reserved
Registers at \$FE08 and \$FF7E	Not used: Locations are reserved	FLASH related registers: \$FE08 – FLCR \$FF7E – FLBPR
Registers at \$FE10 and \$FE11	Mask option registers ⁽¹⁾ \$FE10 – EEDIVHMOR \$FE11 – EEDIVLMOR	EEPROM divider nonvolatile registers ⁽³⁾ \$FE10 – EEDIVHNVR \$FE11 – EEDIVLNVR
Monitor ROM	Used for testing only	Used for testing and FLASH programming/erasing

1. The mask options registers are read-only registers. Values in the registers are defined by mask options (hard-wired connections) specified at the same time as the ROM code submission.
2. The configuration registers are write-once after reset. Values in the registers are defined by the user's software.
3. The EEPROM divider nonvolatile registers consist of EEPROM. Values in the registers are defined by the user's programming.

Code Conversion: HC08AB16A to HC908AB32

Due to the aforementioned differences, a few details must be considered with regard to the user's software and setup when the HC08AB16A is replaced with the HC908AB32.

The following sections describe each item required for the conversion.

CONFIG1 and CONFIG2 Registers

The HC08AB16A has mask option registers MORA and MORB. Instead of these mask option registers, the HC908AB32 has configuration registers CONFIG1 and CONFIG2. These registers must be initialized by the user's software. Usually the initialization is performed just after reset. Since the registers are write-once registers, they can not be rewritten until the next reset.

Here is example code that must be added to initialize the CONFIG 1 and CONFIG2 registers:

```

mov    #$02,CONFIG1    ;Enable STOP instruction
bset   EEDIVCLK,CONFIG2 ;Select CPU bus clock as EEPROM timebase
                                ; divider clock
    
```

FLASH Block Protection

The MC68HC908AB32 has the FLASH protection register (FLBPR) located at \$FF7E. This register consists of FLASH and protects the user's code from unintentional programming and erasing. Motorola strongly recommends that the user protect the entire contents of FLASH. The protection register and the user memory can be programmed at the same time.

Here is an example of the recommended FLASH block protect setup code:

```
FlashProtect equ $00
              org FLBPR
              db FlashProtect ;Protect a whole Flash array
```

CAUTION: *The presence of voltage V_{tst} on the \overline{TRQ} pin will bypass the block protection regardless of the value in the FLASH block protect register. Do not apply V_{tst} to the \overline{TRQ} pin unless debugging the device in monitor mode or during initial programming/erasing of the FLASH memory or when reprogramming a protected area of FLASH.*

EEPROM Divider

The EEPROM requires a 35 μ s timebase to program and erase the EEPROM properly. To set the 35 μ s timebase, the user has two options:

- Write a correct divider value to the EEPROM divider registers located at \$FE1A and \$FE1B (EEDIVH and EEDIVL).
- Program a correct divider value to the EEPROM divider nonvolatile registers located at \$FE10 and \$FE11 (EEDIVHNVR and EEDIVLNVR). The programmed divider value is loaded to EEDIV after each reset.

Regarding the HC08AB16A, if the divider was set in the mask option, it must be set using the second option above. Here is an example of the recommended EEPROM divider setup code:

```
EEPROMDiv equ $808C ;In this example, the CGMXCLK is selected
              ; as the EEPROM divider clock and the
              org EEDIVHNMV ; the frequency is 4MHz
              dw EEPROMDiv ;Program a value $80:$8C at
              ; EEDIVHNVM:EEDIVLNVM
```

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