

Motorola Semiconductor Engineering Bulletin

EB367

In-Circuit Programming of FLASH Memory Using the Monitor Mode for the MC68HC908JL/JK

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Introduction

This engineering bulletin describes how to perform in-circuit programming (ICP) of the FLASH memory using monitor mode for the MC68HC908JL/JK.

Two methods are discussed here:

- Using the M68ICS08JLJK in-circuit simulator (ICS) with P&E Microsystems software
- Using P&E Microsystems software with an external communications circuit

ICP is a process where user code is programmed into the device's FLASH memory after the part has been assembled into the application. ICP also allows the original users code to be erased and re-programmed. This method can be used in development, production/manufacturing, and in a field environment.



Using Monitor Mode for FLASH Programming

Motorola's current solution for ICP is the in-circuit simulators and P&E's software.

The software and ICS allow programming of the parts on the simulator or in the target circuit via a MON08 ribbon cable. The software also allows programming of the part, without the ICS, by using an external communications circuit.

All of the programming described here is accomplished by placing the part into monitor mode. In this mode, erasing and programming are done through a single-wire interface with the host computer.

The two ways to enter monitor mode are:

- The ICS provides the entry requirements to enter standard monitor mode. These entry requirements must be implemented on the target board if the ICS is not used.
- A second way to enter monitor mode, that does not require a high voltage on the $\overline{\text{IRQ}}$ pin, is called forced monitor mode. This mode does not need to meet all monitor mode entry conditions of standard monitor mode, but requires the part to be blank (erased).

This engineering bulletin describes how to connect the part, communicate at different baud rates, place it into monitor mode, pass security, and erase and program the part. If the security code is not known, the contents of the FLASH can't be read, but the FLASH can be erased and reprogrammed.

Information on the M68ICS08JL/JK can be found at <http://mcu.motsps.com>. P&E Microsystems software can be downloaded free from that company's Web site.

NOTE: *All the oscillators used in this application note are the 4-pin "powered" or "canned" type oscillators. Discussing all the different vendors of crystals, ceramic oscillators, other required external components, and component layout variables would be too extensive.*

ICP Using the
M68ICS08JLJK's
MON08 Interface

Use this procedure for performing ICP using the ICS's MON08 cable to the target application.

1. Materials required:
 - a. PC with P&E software installed (version 1.33 or higher)
 - b. M68ICS08JL/JK simulator
 - c. Adapter/connector to connect the female end of the MON08 cable to the target application
 - d. Pin assignment diagram (see [Figure 1](#))
 - e. Monitor mode entry requirements (see [Table 1](#))
 - f. Crystal oscillator on the target or from an external clock source with a value from [Table 2](#)
 - g. Target board must have the ability to perform a power-on reset (POR), not just a reset (required to enter monitor mode).
2. Connections (see [Figure 2](#)):
 - a. 9-pin serial cable from PC to the ICS
 - b. 5 volts to the ICS
 - c. MON08 cable (even pins except pin 8) from J3 of the ICS to the target board with these connections:
 - MON08 GND to the V_{SS} pin on the part
 - MON08 RST to the \overline{RST} pin on the part
 - MON08 IRQ to the \overline{IRQ} pin on the part
 - MON08 PTB0 to the PTB0 pin on the part
 - MON08 PTB1 to the PTB1 pin on the part
 - MON08 PTB2 to the PTB2 pin on the part
 - MON08 PTB3 to the PTB3 pin on the part
3. Operation — Standard monitor mode entry:
 - a. Launch the P&E WINIDE in the ICS08JLZ software.
 - b. Open desired file. (Demo file can be used for testing purposes.)
 - c. Assemble/Compile the file (see [Figure 5](#)).

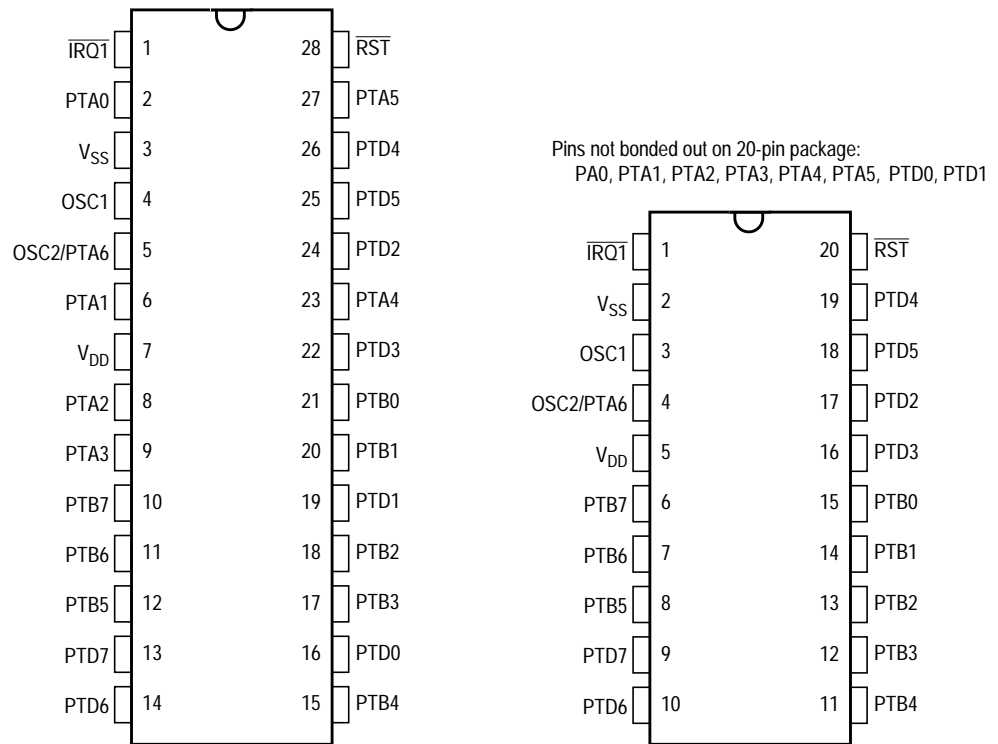
- d. Plug in power to the ICS.
 - e. Turn on power to the target.
 - f. Launch the programmer.
 - g. From “Target Hardware Type,” select “Class II” (see [Figure 6](#)).
 - h. From “PC Serial Port Configuration,” select the PC port you are using and the appropriate baud rate (see [Table 2](#)).
 - i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).
 - j. Select “Contact Target with these Settings...”
 - k. Follow the instructions in the “Power Down/Up Dialog” windows.
 - l. Select appropriate algorithm for the part.
 - m. Double click on “Erase Module” – EM (see [Figure 7](#)).
 - n. Double click on “Program Module” – PM.
 - o. Record security bytes. This information can be seen by quitting and re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, \$FFF6–\$FFFD.
4. Operation — Forced monitor mode entry:
- a. A blank part, 2-wire mode (PTB0 and GND) using the J2 connector, may be used as follows:
 - Remove MON08 RST to $\overline{\text{RESET}}$ connection.
 - Remove MON08 IRQ to $\overline{\text{IRQ}}$ connection.
 - No pullups are required for $\overline{\text{RESET}}$ and $\overline{\text{IRQ}}$ as they have internal pullup resistors.
 - No connections are required for PTB1–PTB3.

ICP Using
the External
Communications
Circuit (No ICS)

Use this procedure for performing ICP via an external communications circuit in place of the ICS to your target application.

1. Materials required:
 - a. PC with P&E software installed (version 1.33 or higher)
 - b. Adapter/connector to connect the male end of the 9-pin serial cable to the target application
 - c. RS-232 communications circuit and a 5-volt power source to power this circuit (see [Figure 3](#) and [Figure 4](#))
 - d. Pin assignment diagram (see [Figure 1](#))
 - e. Monitor mode entry requirements (see [Table 1](#))
 - f. Crystal oscillator on the target or from an external clock source with a value from [Table 2](#).
 - g. Target board must have the ability to perform a POR not just a reset (required to enter monitor mode).
2. Connections (see [Figure 3](#)):
 - a. 9-pin serial cable from PC to the external communications circuit
 - b. V+ pin of the RS-232 part to the $\overline{\text{IRQ}}$ pin of the part
 - c. Communications pin of HC125 to PTB0 of the part
 - d. Target pin requirements:
 - PTB1 of part to V_{DD} via a pullup resistor
 - PTB2 of the part to V_{SS}
 - PTB3 of the part to V_{SS} (crystal frequency $\div 2$) or to V_{DD} via pullup resistor (crystal frequency $\div 4$). See [Table 2](#).
 - $\overline{\text{RESET}}$ has an internal pullup resistor.
3. Operation — Standard monitor mode entry:
 - a. Launch the P&E WINIDE in the ICS08JLZ software.
 - b. Open desired file. (Demo file can be used for testing purposes.)
 - c. Assemble/Compile the file (see [Figure 5](#)).

- d. Apply power to the communications circuit.
 - e. Turn on power to the target.
 - f. Launch the programmer.
 - g. From “Target Hardware Type,” select “Class III” (see [Figure 6](#)).
 - h. From “PC Serial Port Configuration,” select the PC port in use and the appropriate baud rate (see [Table 2](#)).
 - i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).
 - j. Select “Contact Target with these Settings...”
 - k. Follow the instructions in the “Power Cycle Dialog” window.
 - l. Select appropriate algorithm for the part.
 - m. Double click on “Erase Module” – EM (see [Figure 7](#)).
 - n. Double click on “Program Module” – PM.
 - o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, \$FFF6–\$FFFD.
4. Operation — Forced monitor mode entry:
- a. Blank part with oscillator value from [Table 2](#). See [Figure 4](#).
 - Remove connection from $\overline{\text{IRQ}}$ pin from V+ of the RS-232 communications circuit.
 - No connections to PTB1, PTB2, and PTB3 are necessary in this mode.
 - $\overline{\text{IRQ}}$ has an internal pullup resistor.


Figure 1. MCU Pin Assignments
Table 1. Monitor Mode Entry

$\overline{\text{IRQ1}}$	\$FFE and \$FFF	PTB3	PTB2	PTB1	PTB0	Clock Source and Frequency	Bus Frequency	Comments
$V_{DD} + V_{HI}$	X	0	0	1	1	OSC1 at 4.9152 MHz	2.4576 MHz	Bypasses X-tal or RC oscillator; external clock driven directly into OSC1. 9600 baud communication on PTB0. COP disabled.
$V_{DD} + V_{HI}$	X	1	0	1	1	OSC1 at 9.8304 MHz	2.4576 MHz	
V_{DD}	Blank (contain \$FF)	X	x	X	1	X-tal or RC oscillator at 9.8304 MHz	2.4576 MHz	Low-voltage entry to monitor mode. 9600 baud communication on PTB0. COP disabled.
V_{DD}	Not blank	X	X	X	X	X-tal or RC oscillator at desired frequency	$\text{XTALCLK} \div 4$ or $\text{RCCLK} \div 4$	Enters user mode. If \$FFE and \$FFF are blank, MCU will encounter an illegal address reset.

Table 2. Crystal Frequency vs. Baud Rate

Divide by 2 Option (PTB3 to Development Tool or V _{SS})		
Crystal Frequency (MHz)	Internal Bus Frequency (MHz)	Baud Rate
2.4576	1.2288	4800
4.9152	2.4576	9600
7.3728	3.6864	14,400
9.8304	4.9152	19,200
14.7456	7.3728	28,800
Divide by 4 Option (PTB3 to V _{DD})		
4.9152	1.2288	4800
9.8304	2.4576	9600
14.7456	3.6864	14,400
19.6608	4.9152	19,200
29.4912	7.3728	28,800

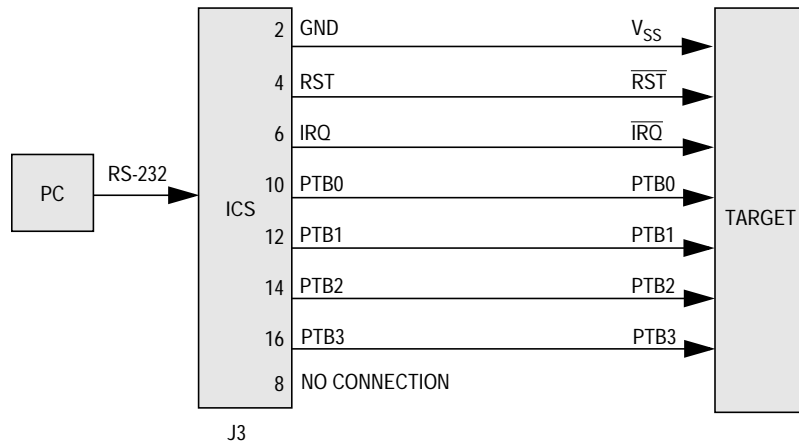


Figure 2. MC68HC908JL/JK MON08 Connections

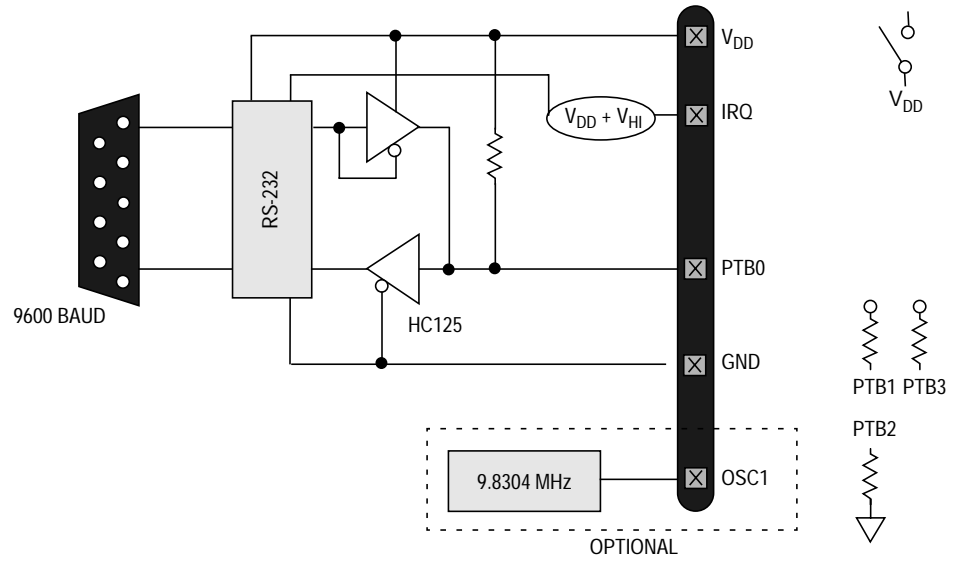


Figure 3. MC68HC908JL/JK Standard Monitor Mode (9.8304 MHz)

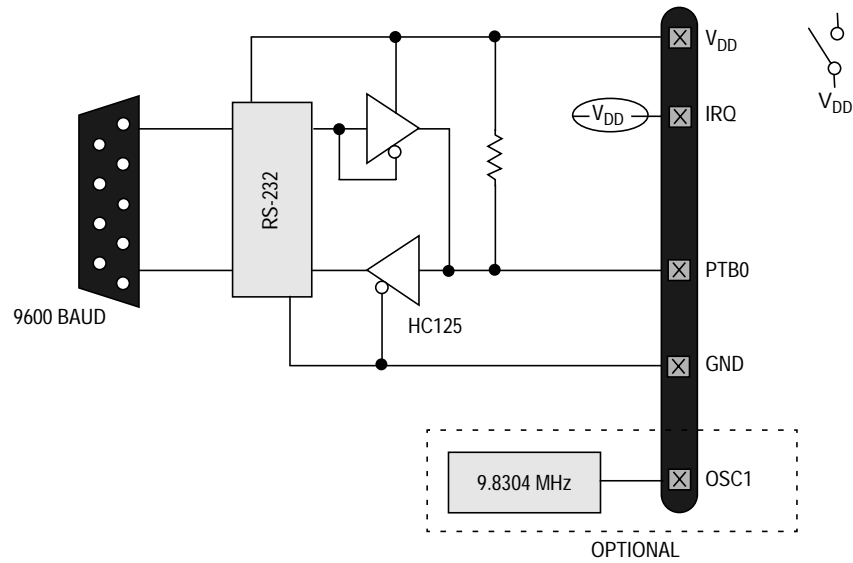


Figure 4. MC68HC908JL/JK Forced Monitor Mode (9.8304 MHz)

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; Here is the sample application...

RAMStart EQU $0000
RomStart EQU $F000 ; Valid for all JLS, JK3, JK1
VectorStart EQU $FF0E

$Include 'j13regs.inc' ; For the 68HC908JL3, 68HC908JK3, 68HC908JK1

    org RamStart

temp_long ds 4
temp_word ds 2
temp_byte ds 1
Timeout1 ds 1 ; Allows three timeout routines to be called each of which
Timeout2 ds 1 ; can run for up to ~ 1/2 second.
Timeout3 ds 1

    org RomStart

*****
* Init_Timer - Turns on timer 1 channel 0 for an Output *
* Compare in approximately 2ms. The timer *
* interrupt service routine continually sets *
* the next interrupt to occur 2ms later. *
*****
Init_Timer:
    mov    #$36,TSC      ; Timer 1 - Cleared + Stopped.
                        ; Clicks once every 64 BUS Cycles
                        ; 200T Clicks ~ 2ms

    mov    #$0,TCR00     ; Set Output Compare to happen 77T clicks
    mov    #77T,TCR0L    ; after we start the timer. (~2ms). The
                        ; timer interrupt will set OC for another ~2ms.

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Figure 5. P&E's WINIDE Window

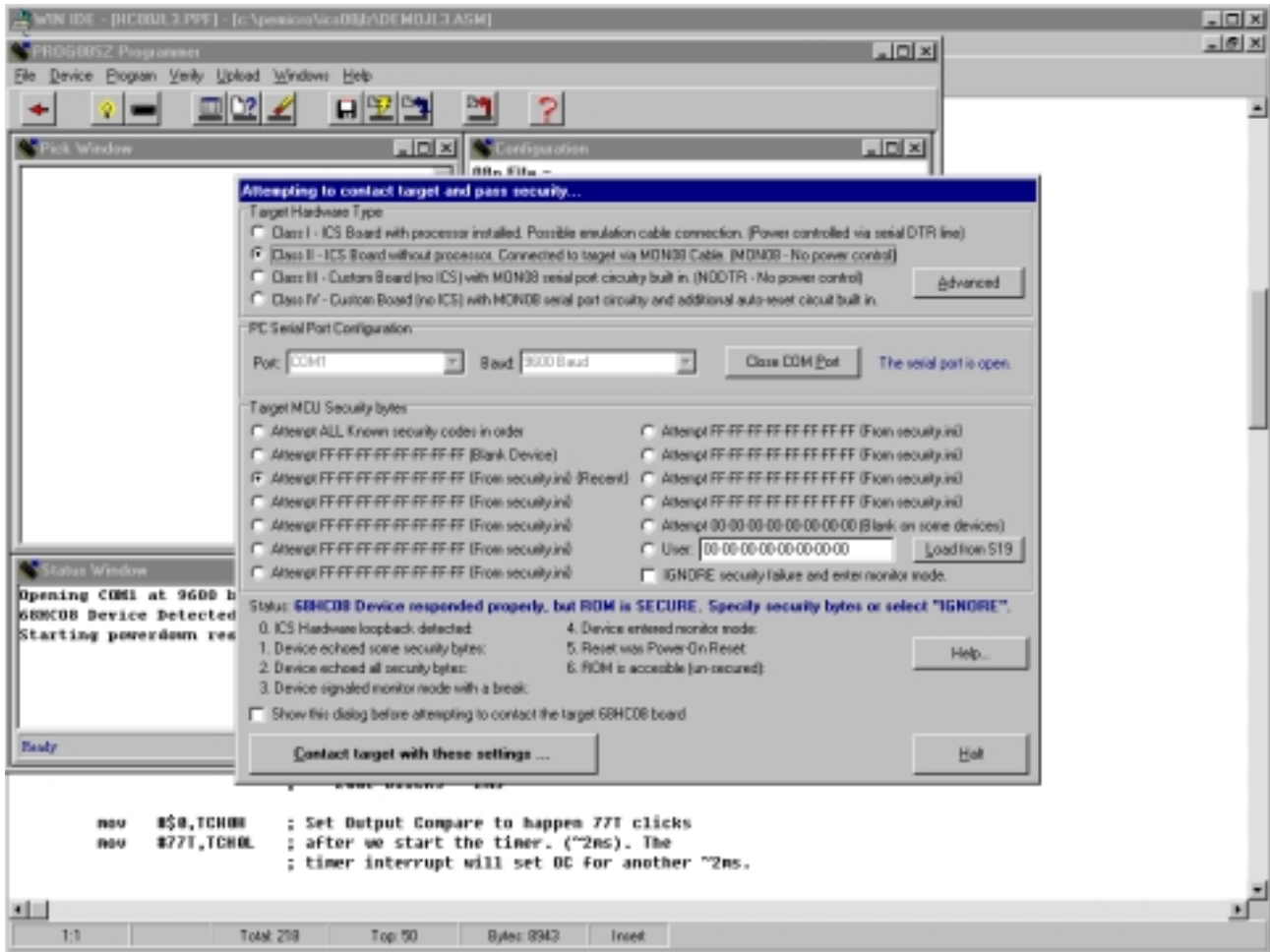


Figure 6. P&E's Target and Security Window

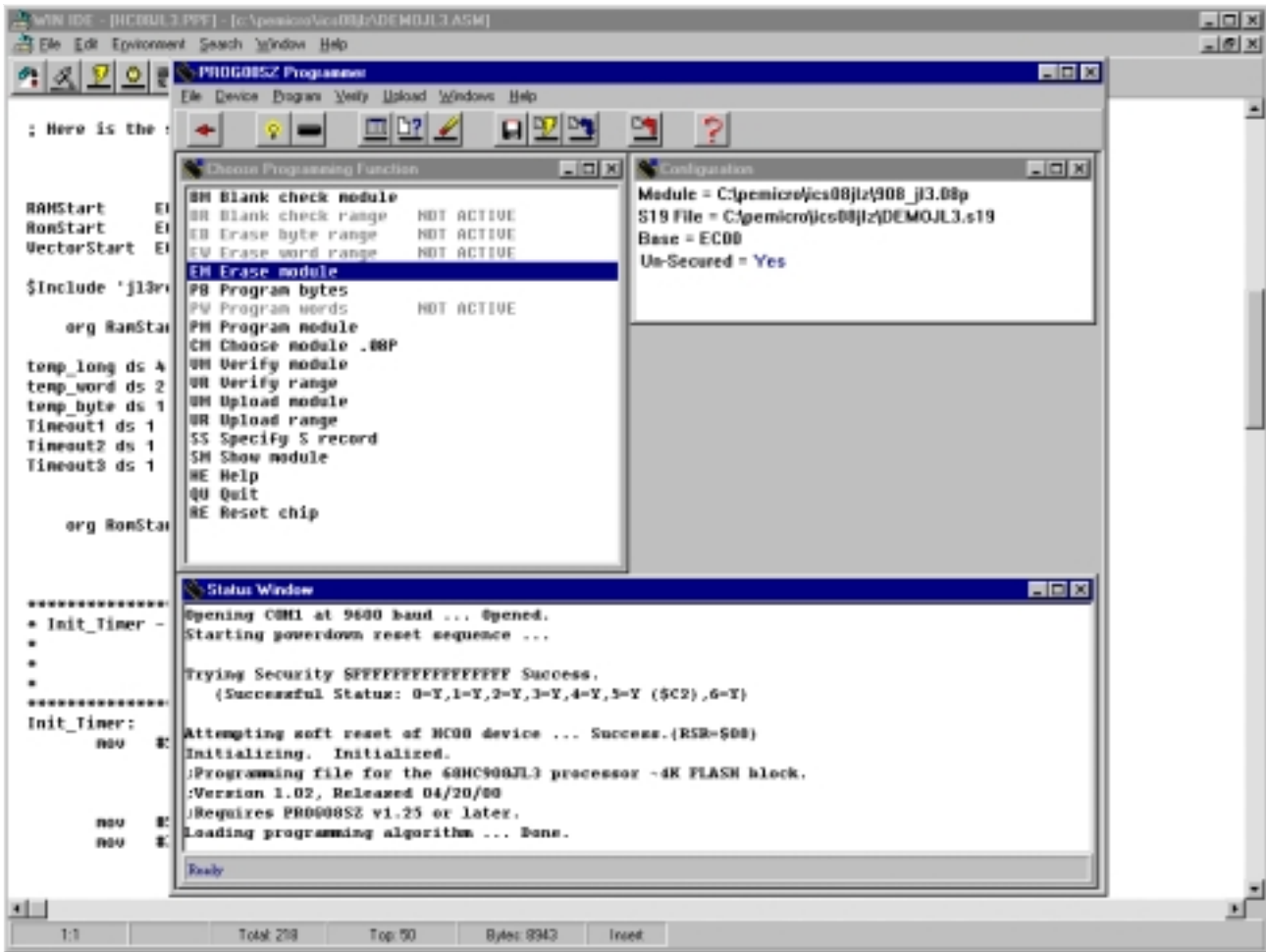


Figure 7. P&E's Programmer Window

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