Using the CodeTEST Probe with Freescale™ MPC8xx Processors

This document describes the requirements for connecting the CodeTEST Probe to MPC8xx processors.

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and the MPC860, MPC850, MPC823, or MPC821 processor and to configure the Probe with the CodeTEST Manager. This application note also applies to other MPC8XX processors with the same external bus interface.

Hardware Connections

The CodeTEST Probe supports targets with 100 MHz bus clocks with no wait states and 100-133 MHz bus clocks with one wait state.

The Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

Non-dedicated or no chip select

Use this connection method if there is not a chip select dedicated for use with the CodeTEST Probe. The chip select that controls the Probe port region can be connected to the extended bus to further qualify the bus cycles.

The following connections are required:

Probe	Processor	Notes
D31:0 D15:0	D0:31 D0:15	32-bit port 16-bit port Note the bit-wise inversion of the bus.
A31:0 A25:0	A0:31 A6:31	MPC860 and MPC821 MPC850 and MPC823 Note the bit-wise inversion of the bus.
X15:8	NC	
X7:0	CS7:0*	Connect as needed to further qualify bus cycles.

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C0	VCC	VCC – not required
C1	CLKOUT	CLK
C2	NC	DS - can be connected to TA* if using 2 Strobe mode.
C3	TS*	AS
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	NC	CYC
C7	RD/WR*	WS

Dedicated CodeTEST chip select

Use this connection method when a chip select is dedicated for use with the CodeTEST Probe. The chip select used for the Probe port must be configured so that it meets the requirements of the Probe AS signal.

The following connections are required:

Probe	Processor	Notes
D31:0 D15:0	D0:31 D0:15	32-bit port 16-bit port Note the bit-wise inversion of the bus.
A31:0 A25:0	A0:31 A6:31	MPC860 and MPC821 MPC850 and MPC823 Note the bit-wise inversion of the bus.
X15:0	NC	
C0	VCC	VCC – not required
C1	CLKOUT	CLK
C2	NC	DS - can be connected to TA* if using 2 Strobe mode.
C3	CSx*	AS
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	NC	CYC
C7	RD/WR*	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Non-dedicated CodeTEST chip select or no chip select

Use the Universal Probe type and select the following settings:

Field	Setting		Notes
	MPC860 and MPC821	MPC850 and MPC823	
Port Address			Enter address of the Probe tag port.
Port Address Mask	0x00000000	0xfc000000	
Extended Bus	0x0000	0x0000	
Extended Bus Mask	0xFFFF	0xFFFF	See Note.
Bus Type	Non-multiplexed	Non-multiplexed	
Port Size			Select appropriately for target hardware.
Reset Configuration	Both	Both	
Strobe Configuration	1 Strobe + internal data strobe	1 Strobe + internal data strobe	Can use 2 Strobe mode if TA* is connected
Address Strobe Polarity	Low	Low	
Write Strobe Polarity	Low	Low	
Bus Arbitration Polarity	Disabled	Disabled	
Endianess	Big	Big	
Word Swap	No	No	
Frequency Range			Set to the frequency of CLKOUT.
Invert Clock	No	No	
Phase Shift	0	0	Adjust as necessary to obtain accurate data.

Note: The extended bus mask must be set to allow qualification of the cycle with the appropriate chip select if necessary. For example, if the Probe ports reside in a region of memory controlled by chip select ‘0’ (CS0*), then the mask must be set to 0xFFFE; if the ports reside in a region of memory controlled by chip select ‘1’ (CS1*), then the mask must be set to 0xFFFD, and so on.

Dedicated CodeTEST chip select

Use the Universal Probe type and select the following settings:

Field	Setting		Notes
	MPC860 and MPC821	MPC850 and MPC823	
Port Address			Enter address of the Probe tag port.
Port Address Mask	0xFFFFFFFF	0xFFFFFFFF	

Extended Bus	0x0	0x0	
Extended Bus Mask	0xFFFF	0xFFFF	
Bus Type	Non-multiplexed	Non-multiplexed	
Port Size			Select appropriately for target hardware.
Reset Configuration	Both	Both	
Strobe Configuration	1 Strobe	1 Strobe	
Address Strobe Polarity	Low	Low	
Write Strobe Polarity	Disabled	Disabled	
Bus Arbitration Polarity	Disabled	Disabled	
Endianess	Big	Big	
Word Swap	No	No	
Frequency Range			Set to the frequency of CLKOUT.
Invert Clock	No	No	
Phase Shift	0	0	Adjust as necessary to obtain accurate data.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least 2 clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.