

Using VRC_CTL to Control an External VDD_LV Supply on the MPC5748G

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1 Introduction

The MPC5748G MCU is a multi-core high performance Power Architecture® based microcontroller targeted for automotive gateway and body applications but also equally suited to other applications due to the rich communication peripheral set and embedded Hardware Security Module (HSM).

For maximum flexibility, the MPC5748G family supports various regulation modes for the VDD_LV (1.25 V) supply. This application note describes a proposed scheme using a FET to control an external VDD_LV supply using the VRC_CTRL signal.

Note that the proposed scheme has been simulated as detailed in this application note however the customer is responsible for full hardware testing and validation of the implemented solution.



2 Regulator summary

The MPC5748G family of devices has various internal regulators as detailed below. All of these regulators are powered from the VDD_HV_A domain.

- 3.3 V Flash regulator¹
- 1.25 V Full Power Regulator (FPREG)
- Low power regulator (LPREG) active during LPU mode
- Ultra Low Power Regulator (ULPREG) active during STANDBY mode

3 1.25 V regulator operation

The 1.25 V internal regulator essentially has the following two modes:

- Internal Regulation Mode:
 - The internal regulator (FPREG) is enabled and controls the voltage applied to the VDD_LV pins. On MPC5748G, an external ballast transistor is required to dissipate the power lost in going from the ballast supply voltage to the 1.25 V VDD_LV.
 - The VRC_CTL pin is controlled by the internal FREG and is connected directly to the base of the external ballast transistor to create a control loop. FPREG measures the voltage on the VDD_LV domain and adjusts VRC_CTL accordingly. If the MCU enters STANDBY mode the VRC_CTL drive is stopped, the external ballast transistor turns OFF, and VDD_LV is no longer supplied.
- External Regulation Mode:
 - The internal regulator is disabled. There is no external ballast transistor and VRC_CTL is not driven so can be left unconnected.
 - A 1.25 V VDD_LV supply must be supplied externally and be within the current and voltage ranges as specified in the datasheet.
 - A pin is supplied (EXT_REG_CTRL) which can be used to control the external regulator (see the device reference manual for details).

In STANDBY mode, the VDD_LV supply should be disconnected or excess leakage will occur driving up the STANBY current.

NOTE

During power-up, the PORST pin can be used to hold the MCU in reset whilst the external VDD_LV is stabilizing. Equally the PORST pin can be tied to VDD_HV_A and the MCU LVD will hold the MCU in reset until VDD_LV is in the correct range. See the device reference manual for more details.

4 Using VRC_CTRL

As mentioned above, the EXT_REG_CTRL pin can be used to control an external VDD_LV supply. Using this pin however will result in the loss of a GPIO/peripheral pin.

The VRC_CTRL is a dedicated pin with no GPIO functionality and is disabled in external regulation mode. By enabling internal regulation mode and using an external FET, it is possible to use VRC_CTRL to control an external VDD_LV supply as detailed below. By disconnecting the VDD_LV supply when the MCU is in STANDBY mode, excess leakage current is avoided.

1. The 3.3 V flash regulator does not function when VDD_HV_A is 3.3 V. In this instance, external power must be supplied via the VDD_HV_FL A pin

Note that NXP has simulated a very specific circuit which must be implemented as described below. Any deviations from the recommended circuit or operation out-with the specification will result in un-defined behavior.

Following are the implementation requirements:

- The MPC5748G internal regulator is enabled to allow VRC_CTRL to function
- The FET is a DMG3414U
- The component values and supply voltage must adhere to the specification detailed below.

Table 1. Circuit component values

Symbol	Description	Value
VDD_SBC	SBC output voltage	1.3 V +/- 2%
Cd	Total Drain Capacitance	= Cs ¹
Cg	Total Gate Capacitance	4 nF to 8 nF X7R
Rg0	Series Resistance	0 Ω
Rg	Total Gate Resistance	0.8 KΩ to 1.2 KΩ
Cs	Total Source Capacitance	6 uF to 12 uF X7R

1. Drain capacitance must be greater than or equal to the Source capacitance. Drain capacitance is defined by the requirements of the external VDD_LV supply.

The following figure shows the circuit schematic:

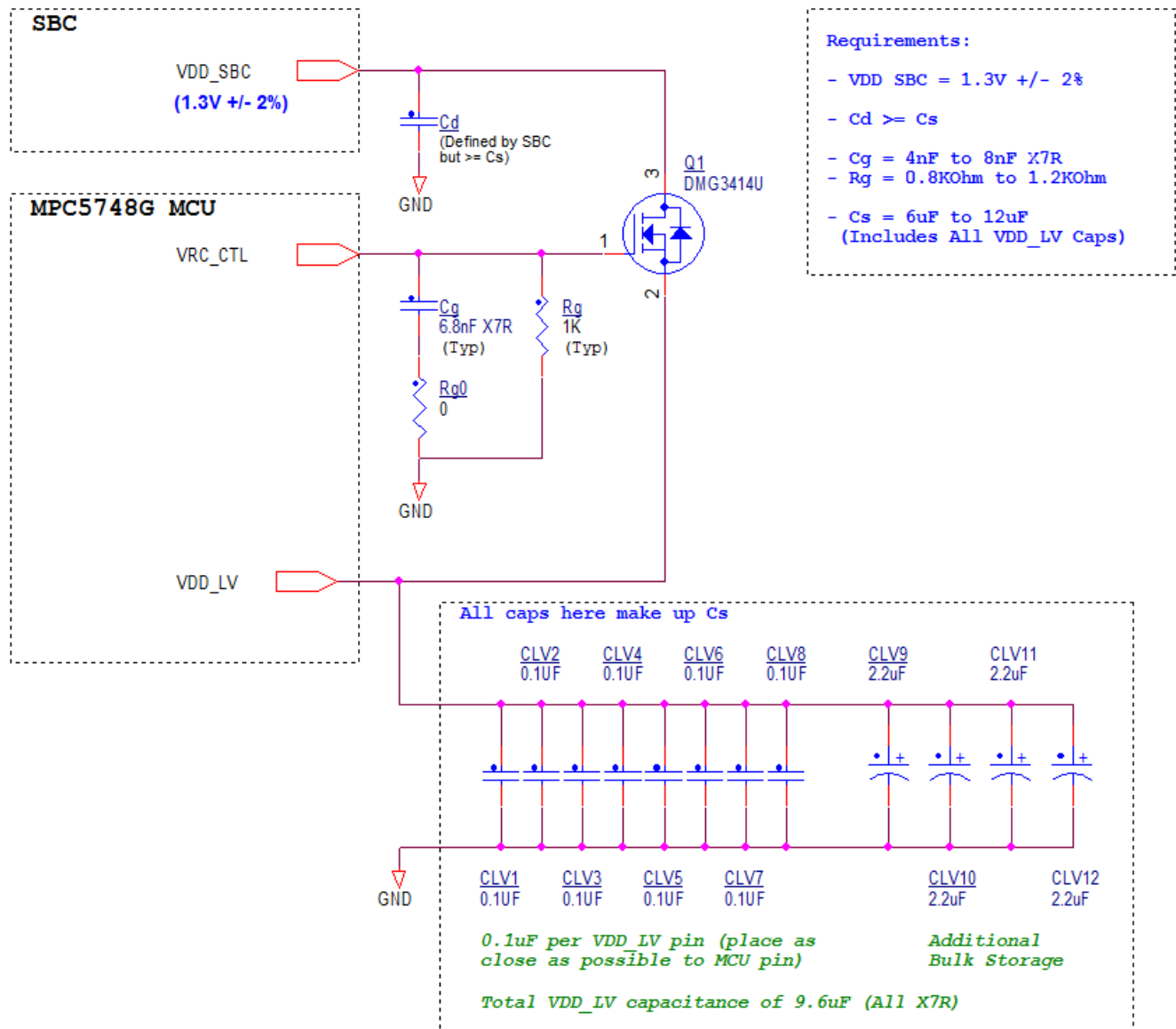
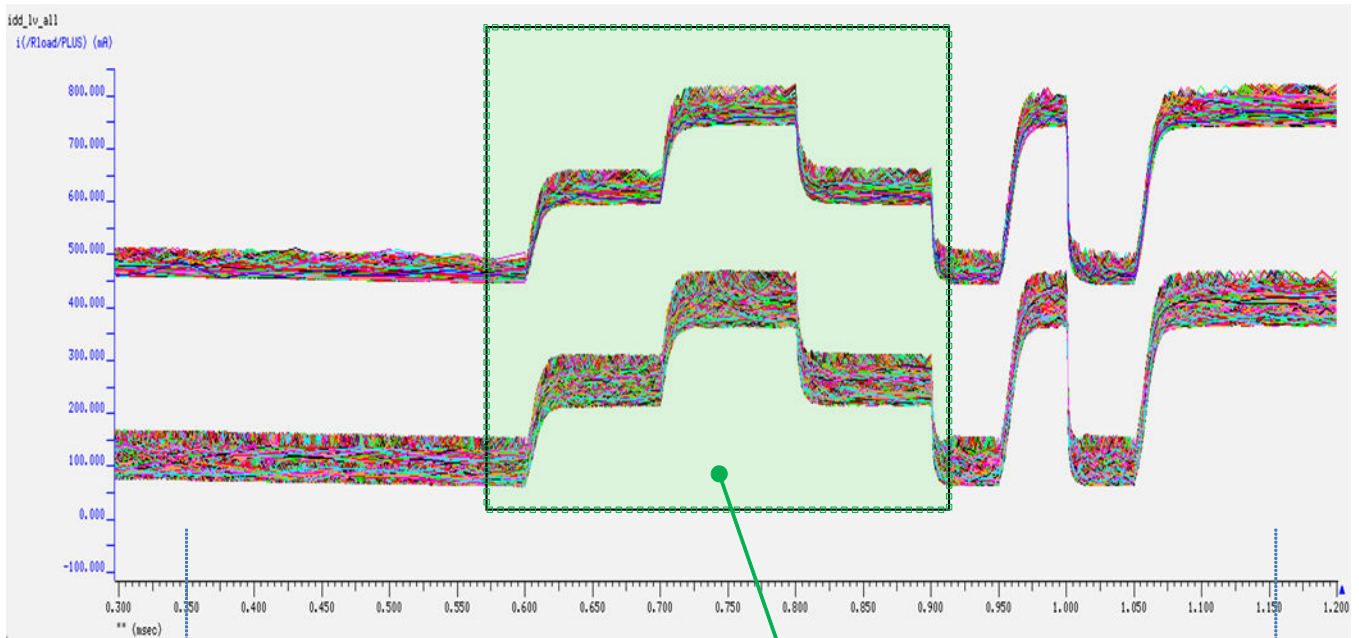


Figure 1. Schematic implementation

NOTE

Extensive simulations have been run using the circuit and component values shown above. The critical simulation results are shown below however the customer must perform complete validation of this circuit implementation on their hardware to ensure functionality over all operating conditions.



Simulated VDD_LV load under normal conditions³

Corresponding VDD_LV transients at the pin

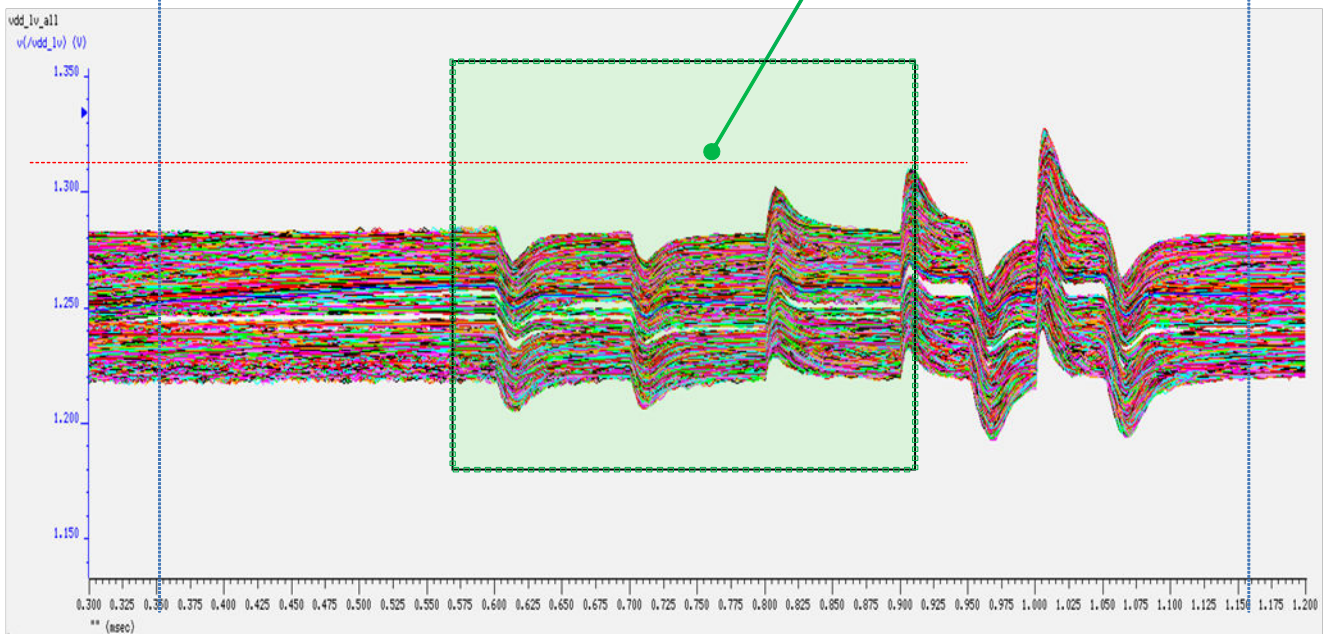


Figure 2. Simulation results

³Normal conditions are defined to be those within specification in the datasheet

Under normal load conditions, simulation has shown that the VDD_LV voltage remains within the permitted range of 1.20 V – 1.32 V.

5 Conclusion

The MPC5748G can use the VRC_CTL pin to control an external FET to control and externally generated VDD_LV as long as:

- The internal FPREG is enabled.
- The design criteria for the components and implementation described in this application note are followed.
- No additional circuitry is added to the control loop.

Although NXP has made every effort to simulate this configuration, it is up to the customer to ensure that the implemented circuit functions as expected over the range of expected operating conditions (temperature, voltage) and core loadings.

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