

# MPC5675K Hardware Design Guide

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## 1 Introduction

This document summarizes necessary information to design the board based on MPC5675K. It describes the differences of internal and external power supply mode, decoupling of power supplies, and boot configuration.

## 2 Power sequencing

Power rail sequencing recommendations (Power Up):

- Power up all VDD\_HV\_xxx rails before VDD\_LV\_xxx rails
- Power up all VDD\_HV\_xxx rails simultaneously
- Power up all VDD\_LV\_xxx rails simultaneously

Power rail sequencing recommendations (Power Down):

- Power down VDD\_LV\_xxx rails before VDD\_HV\_xxx rails
- Power down all VDD\_LV\_xxx rails simultaneously
- Power down all VDD\_LV\_xxx rails simultaneously

### 2.1 Power supply modes

### Contents

1	Introduction.....	1
2	Power sequencing.....	1
3	Nexus and JTAG.....	6
4	Reset considerations.....	7
5	Clock out pins.....	9
6	Digital IO pads.....	9
7	Built in Oscillator XOSC.....	9
8	Boot configuration pins.....	11
9	Special signals.....	12
10	Decoupling.....	12



## Power sequencing

MPC5675K implements two power supply modes namely internal and external mode. The state on VREG\_INT\_ENABLE pin selects the power supply mode. There are internal weak pull downs (100K) on VREG\_INT\_ENABLE\_B and RESET\_SUP\_B. The following table summarizes the differences between both modes.

**Table 1. Power Supply modes**

Power Supply Modes	Package Pins			Power On Reset Source	Description
	VREG_INT_ENABLE_B	RESET_SUP_B	VREG_CTRL		
Internal VREG Mode	Low level on this pin selects Internal VREG Mode	Not used. Tie to VSS	Internal VREG output that controls the gate of external SMPS pMOS	Internal POR	Internal VREG enabled. All internal LVDs and HVD enabled. VDD_LV_XXX rail is supplied by internal VREG.
External VREG Mode	High level on this pin selects external VREG mode	Power On Reset Source ( RESET_SUP_B shall be protected by a 10 kOhm series/pull up resistor depending on POR generator output push/pull or open drain)	Not used. Pull up to VDD_HV_PMU	RESET_SUP_B ( must be asserted as long as core voltage is outside of its valid range of operation) and internal HV POR	Internal VREG in bypass mode. LVD and HVD for core voltage disabled out of reset. LVDs for high voltage rails enabled. VDD_LV_XXX needs to be regulated by external voltage regulator.

Why external LVDs are required if core supply is regulated externally

- Margin required between external voltage and internal voltage (voltage drop over bond wires)
- Internal IR drop between LVD location and location of lowest voltage (dynamic conditions in different modes of operation)
- Limited accuracy of internal bandgap before trimming
- Hysteresis between rising edge (need to come out of reset) and falling edge of LVD (detection of minimum guaranteed operating range)
- Limited guaranteed operating range of given technology (especially analog IP)

MPC5675K dual supply concept

- Separate internal VREG operation from external VREG operation
- One dedicated pin to select between internal or external VREG mode
- Optimize internal core voltage LVD and HVD thresholds for internal VREG operation
- In external VREG mode internal core voltage, LVDs and HVD can be enabled by software after reset with adjusted thresholds to allow redundant operation to external LVDs (second level of detections)
- All LVDs and HVD are supplied by VDD\_HV\_PMU

### 2.1.1 Internal VREG mode

1.2 V core supply is regulated by an internal SMPS regulator with external power components.

PMU related signals in internal VREG mode:

- VREG\_INT\_ENABLE\_B low level selects internal VREG mode
- VREG\_CTRL used to control gate of external pMOS

- RESET\_B used as bidirectional functional reset. No POR functionality. It can be used by debugger to determine start of instruction execution
- RESET\_SUP\_B not used. It should be tied to VSS

Sequencing:

- Internal PMU will start generating core voltage as soon as PMU supply is valid

LVDs and HVD

- All internal LVDs and HVD active

VREG PCB layout is critical for efficient and reliable PMU operation. NXP can assist in PCB layout design and review process. Ensure supplies for PMC and Ballast are star routed. Please Review the application note AN3898.

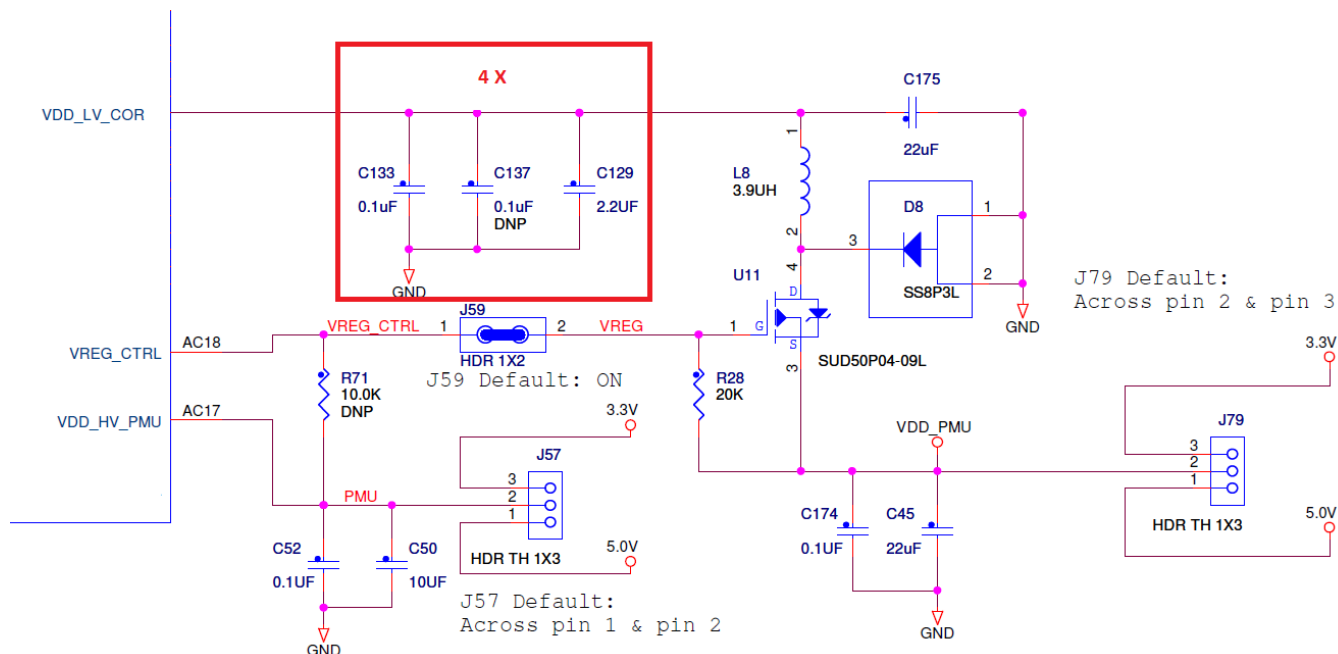


Figure 1. Internal VREG mode circuitry

The parameters of used components is summarized in the table below.

Table 2. Internal VREG mode circumstance component list

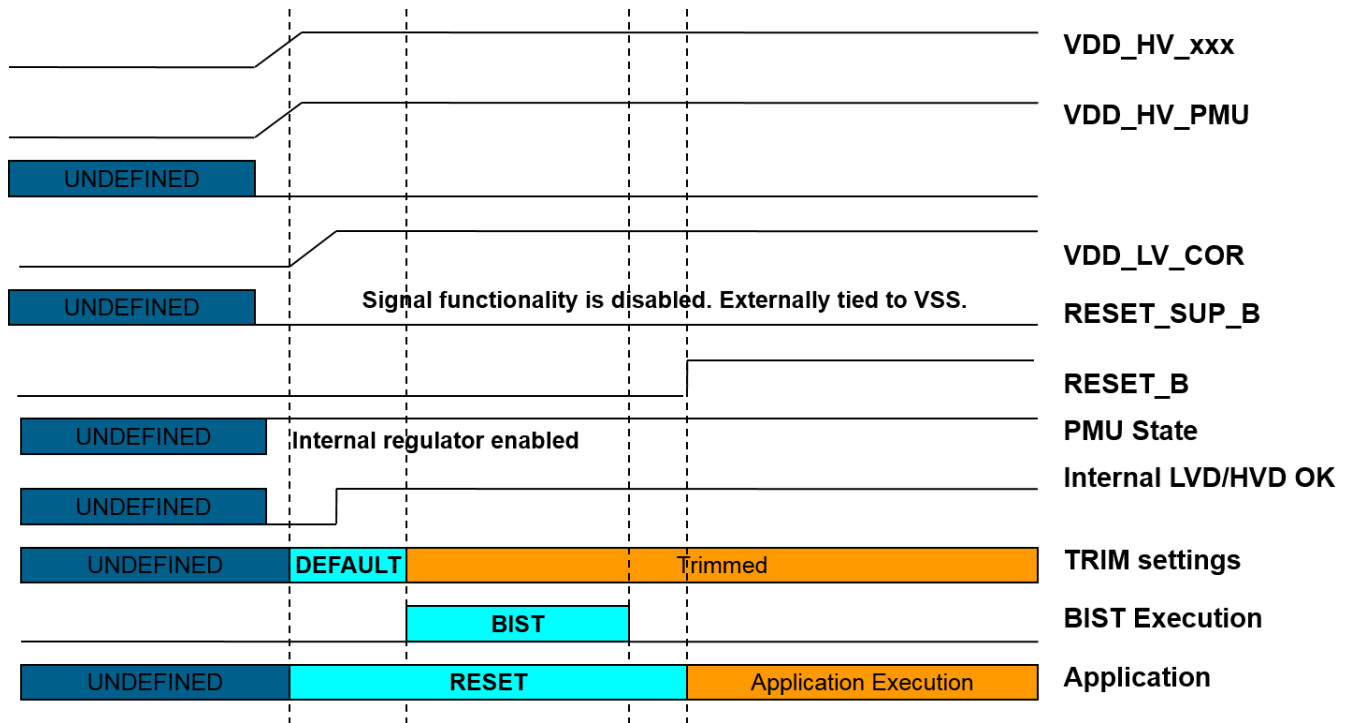
Part name	Part Type	Nominal value	Description
U11	SUD50P04 / SQD50P04 pMOS	2 A - 40 V	Vishay TM low threshold p-MOS, Vth < 2.5 V, Rdson@4.5 V < 20 mOhm, Cg < 5 nF
D8	SS8P3L Schottky		Vishay TM low Vf Schottky diode
L8	inductor	3.9 $\mu$ H -1.5 A	Buck shielded coil low ESR
C129	capacitor	4 x 2.2 $\mu$ F	Filter capacitor
C137	Capacitor (DNP)	X times 0.1 $\mu$ F - > 16 V	Ceramic—See VDD_LV_COR slides for more details on placement and quantity
C133	capacitor	X times 0.1 $\mu$ F - > 16 V	Ceramic —See VDD_LV_COR slides for more details on placement and quantity
C52	capacitor	0.1 $\mu$ F - 20 V	Filter capacitor
C50	capacitor	10 $\mu$ F - 20 V	Filter capacitor
R28	Resistor	20 k – 100 k	Pull up for power p-MOS gate

Table continues on the next page...

**Table 2. Internal VREG mode circumstance component list (continued)**

Part name	Part Type	Nominal value	Description
C45	Capacitor	22 $\mu$ F - 20 V	Supply decoupling cap, ESR < 50 mOhm - as close to p-MOS source as possible. (To prevent DC/DC noise to propagate on the GND plane)
C174	Capacitor	0.1 $\mu$ F - 20 V	Filter capacitor
C175	Capacitor	22 $\mu$ F - 20 V	Buck capacitor, total ESR < 100 mOhm - as close to the coil as possible

The voltage rating of 20 V or higher is recommended for the SMPS input capacitors (C45, C174, C50 and C52), as these capacitors are exposed to the high current switching of the drain, therefore voltage peaks might be high under heavy load conditions. It is critical that capacitor C45 have a very low ESR and a high bandwidth of at least 50 MHz to dampen higher order harmonics of the SMPS.



**Figure 2. Power-on chart for internal regulator mode**

### 2.1.1.1 Capacitor ratings

General Remarks on Capacitor Voltage Ratings:

- The following recommendation assumes that all capacitors used are ceramic capacitors.
- The reason for a proposed voltage rating which is higher than its nominal operating voltage is primarily driven by the higher pulse current capability of capacitors with higher voltage ratings compared to capacitors with the same capacitance but lower voltage ratings.
- Tentatively a higher voltage rating is recommended for capacitors with higher capacitance values as they typically have a lower ESR which leads to higher pulse currents through the capacitor. On the other side those capacitors also allow higher energy densities due to their bigger size. Based on that a detailed analysis with information from the capacitor manufacturer is a recommended way to determine the minimum required voltage rating for a given capacitor and a given pulse current exposure over lifetime.

- A more detailed analysis is also recommended to be executed with more detailed data from the capacitor manufacturers on the capacitor's current surge capabilities over lifetime.
- The following figure (source: [edn.com](http://www.edn.com)) shows the two different current loops of a buck converter. A high  $di/dt$  current loop ( $i_{Cin}$ ) on the converter input side and a lower  $di/dt$  current loop ( $i_{Cout}$ ) on the output side of the buck converter. Depending on whether a capacitor is used on the input side or at the output side different pulse current capabilities are required for the capacitors used. Typically capacitors with a higher voltage rating also provide a higher pulse current capability at the same capacitance value.

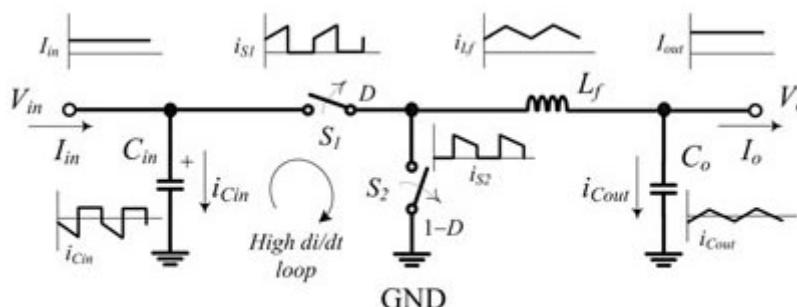


Figure 3. Buck Converter Power Stage

## 2.1.2 External VREG mode

1.2 V core supply is regulated by an external voltage regulator. PMU related signals in external VREG mode.

- VREG\_INT\_ENABLE\_B high level selects external VREG mode by putting the internal VREG in bypass mode
- VREG\_CTRL not used. Tie to VDD\_HV\_PMU via 100 kOhm pull up. Pull Up might be replaced by 0 Ohm (hard tie) or floating after char (HTOL) results are available
- RESET\_B used as bidirectional functional reset. No POR functionality. Can be used by debugger to determine start of instruction execution
- RESET\_SUP\_B determines POR. Must not be deasserted by external reset generator if core voltage is outside of specified range. Input shall be protected by a 10 kOhm series resistor

### Sequencing

- See chapter [Power sequencing](#)

### LVDs and HVD

- Core voltage LVD and HVD disabled. Can be enabled by software after start up
- Internal LVDs on high voltage rail are active

### Voltage levels

- RESET\_SUP\_B, INT\_VREG\_ENABLE\_B need 3.3 V signal levels

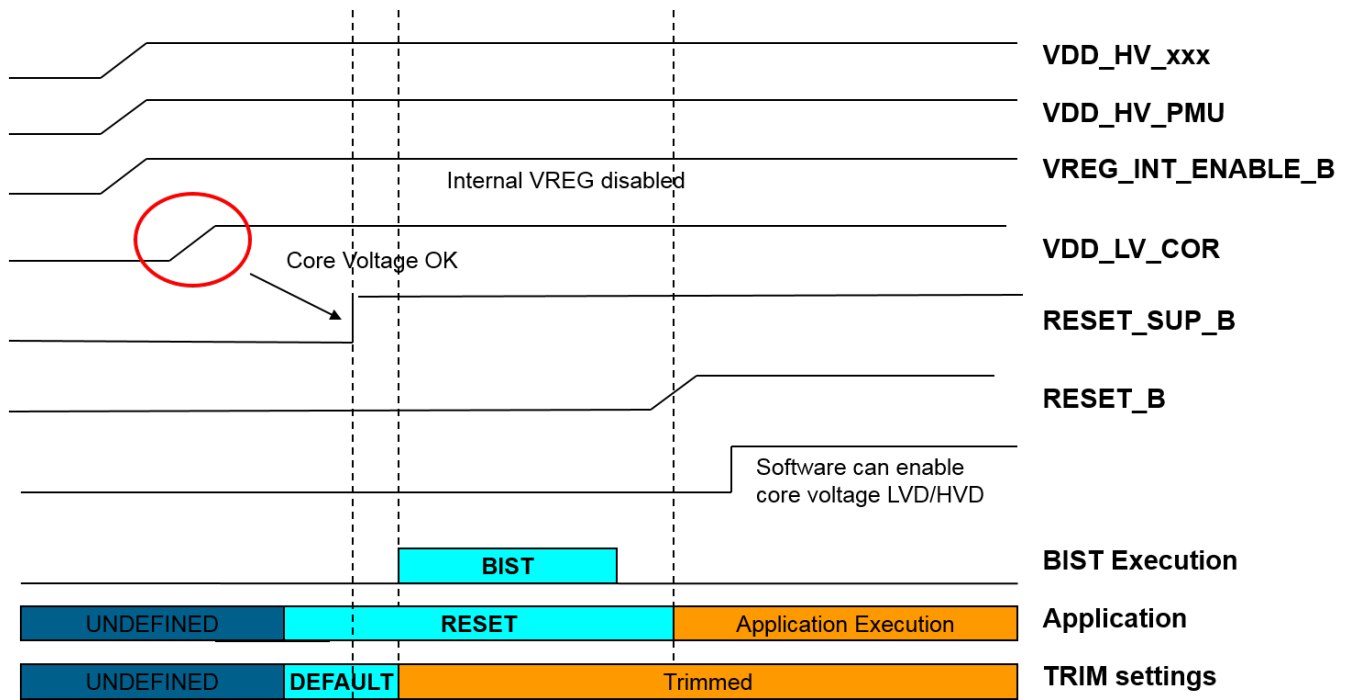


Figure 4. Power-on chart for external regulator mode

### 2.1.3 SoC voltages generated with linear regulators

In case when SoC voltages are generated with linear regulators none of the capacitors directly connected to one of the SoC supply rails is exposed to huge pulse currents during system power up or steady system operation. In this case the current through the capacitors is limited by the voltage which slowly ramps up to its nominal value during power on.

For this case NXP recommends a minimum voltage rating for noise filtering and decoupling capacitors of 16 V.

### 2.1.4 High voltage rails supplied by external SMPS regulator

In case the pulse current capability (voltage rating) of the SMPS output capacitors depend on the type of SMPS selected by the customer for the supply of the high voltage rails. For standard SMPS regulators also a minimum 16 V rating for the output capacitors (capacitors connected to SoC VDD\_HV\_IO, VDD\_HV\_FLASH, VDD\_HV\_ADC, VDD\_HV\_DRAM, VDD\_HV\_PDI) is recommended.

The input capacitors pulse current (voltage rating) highly depends on the design of the SMPS and its parameters selected by the customer.

## 3 Nexus and JTAG

6 pin JTAG Interface IEEE 1149.1 with 3.3 V levels.

- JTAG\_RST, weak pull down, dedicated pin
- JCOMP input that provides the ability to share the TAP, internal weak pull down, dedicated pin
- TMS, internal weak pull up, dedicated pin

- TCK, internal weak pull up, dedicated pin
- TDI, internal weak pull up, muxed with GPIO
- TDO, muxed with GPIO

During reset sequence a low level (tbc) on MDO[0] indicates that SoC is ready for debugger communication. No polling required. 22 pin Nexus class 3+ debug interface.

- EVTO\_B
- EVTI\_B
- MCKO, typical frequency 45 MHz @ 180 MHz core clock
- MSEO\_B[1:0]
- RDY\_B, can selectively be enabled via JTAG register
- Full port mode with 16 MDO[15:0] signals (FPM)
- Reduced port mode with 12 MDO[11:0] signals (RPM)
- DDR mode supported (tbc after validation)

Nexus Interface is enabled via JTAG configuration setting. All Nexus pins except for MDO[0] muxed with GPIOs and other alternate functions. Default state for muxed Nexus pins after reset is GPIO.

- Nexus pins are automatically muxed from GPIO setting to Nexus functionality when Nexus is enabled via JTAG. This affects:
  - MCKO
  - MSEO\_B[1:0]
  - MDO[15:1] in FPM
  - MDO[11:1] in RPM
- Nexus RDY\_B can be enabled separately via JTAG TEST\_CTRL register bitfield NEX\_RDY\_PORT\_EN, JTAG TEST\_CTRL register bitfield NEX\_RDY\_sel select whether RDY from Core 0 or Core 1 is driven as an output
- Nexus EVTI\_B together with EVTO\_B can be enabled by a single bit via Nexus PCR register bitfields EVT\_EN

For 12 bit or 16 bit MDO port mode, the following Nexus connector is recommended:

- HP25-2 (ASP-148422-01) by Samtec (2 rows with 25 pins each; 0.8 mm pitch)
- Supported by Lauterbach

NXP will provide example schematics. The final connector signal assignment depends on the development tool requirements.

## 4 Reset considerations

### 4.1 SoC Power Up Reset Considerations

In internal VREG mode, all the standard GPIOs are kept in High-Z unless none of the following LVDs and HVD detect any under/over voltage condition:

- VDD\_LV\_COR LVD/HVD
- VDD\_HV\_IO LVD
- VDD\_HV\_FLASH LVD
- VDD\_HV\_ADC LVD
- VDD\_HV\_PMU LVD

Built in self tests are executed (if enabled) as soon as POR is released

- When no LVD and no HVD is asserted
- Independent of state of RESET\_B

The recommended reset circuitry is shown in the [Figure 5](#).

## Reset considerations

- External Pull Up as RESET\_B is a bidirectional functional reset.
- Tie RESET\_SUP\_B to VSS.

VDD\_LV\_CORE LVD and HVD circuitries are enabled from POR.

### External VREG Mode

- All standard GPIOs are kept in High-Z unless none of the following LVDs detect any under voltage condition:
  - VDD\_HV\_IO LVD
  - VDD\_HV\_FLASH LVD
  - VDD\_HV\_ADC LVD
  - VDD\_HV\_PMU LVD
- All standard GPIOs are kept in High-Z if RESET\_SUP\_B is asserted.
  - RESET\_SUP\_B must not be released if VDD\_LV\_XXX rails are out of specified range of operation.

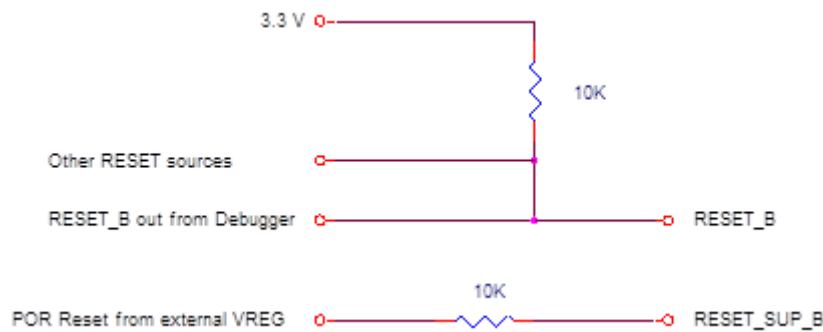
Built in self tests are executed (if enabled) as soon as POR is released

- When no active internal LVD is asserted (3.3V rail LVDs only)
- When RESET\_SUP\_B is de-asserted

The recommended reset circuitry is shown in the [Figure 5](#).

- Series resistor if POR generator has push pull output
- Pull up resistor to VDD\_HV\_PMU if POR generator has open collector output

VDD\_LV\_CORE LVD and HVD circuitries are disabled from POR, but can be enabled by software after SoC is out of reset condition.



**Figure 5. Recommended Reset circuitry**

## 4.2 SoC reset considerations

### SAFE Mode

- All standard GPIO pads go to High-Z upon entering Safe\_Mode
- Weak pulls can be configured for standard GPIOs to become active in Safe\_Mode

The following pads have their input buffers enabled during reset:

- TCK (internal weak pull up)
- TMS (internal weak pull up)
- TDI (internal weak pull up)
- JCOMP (internal weak pull down)
- NMI (internal weak pull up)
- eTimer1\_ETC[3] (FAB) (internal weak pull down)
- eTimer0\_ETC[4] (ABS[0]) (internal weak pull down)
- eTimer0\_ETC[3] (ABS[2]) (internal weak pull down)



The following pads get their input buffers and output buffers enabled automatically after reset:

- FCCU\_F\_0 (external pull recommended; shall be selected in alignment to configured FCCU “error out protocol”)
- FCCU\_F\_1 (external pull recommended; shall be selected in alignment to configured FCCU “error out protocol”)

## 5 Clock out pins

Two dedicated clockout signals are available. Both pins muxed between Clock Output Generator and eTimer 2 channel 5.

- BGA 257:
  - Pin B3: GP Fast/Slow pad, 3.3 V
  - Pin F14: PDI Fast pad, 1.8 V – 3.3 V
- BGA 473:
  - Pin B3: GP Fast/Slow pad, 3.3 V
  - Pin E20: PDI Fast pad, 1.8 V – 3.3 V

Other possibility of generating Clkout:

- All FlexPWM timer outputs usable as clockoutput generators
- All eTimer outputs usable as clockoutput generators

Series termination recommended for high frequency outputs to reduce reflections.

## 6 Digital IO pads

MPC5675K implements different pads with different IO capabilities and characteristics. Following pad types are available for nominal 3.3 V operation:

- GP Slow:  $F_{\max} = 4 \text{ MHz @ } 25 \text{ pF}$
- GP Medium:  $F_{\max} = 40 \text{ MHz @ } 25 \text{ pF}$
- GP Fast:  $F_{\max} = 72 \text{ MHz @ } 25 \text{ pF}$
- GP Symmetric:  $F_{\max} = 50 \text{ MHz @ } 25 \text{ pF}$

Following pad types are available for nominal 1.8 V – 3.3 V (1.62 V – 3.6 V) operation (package dependent):

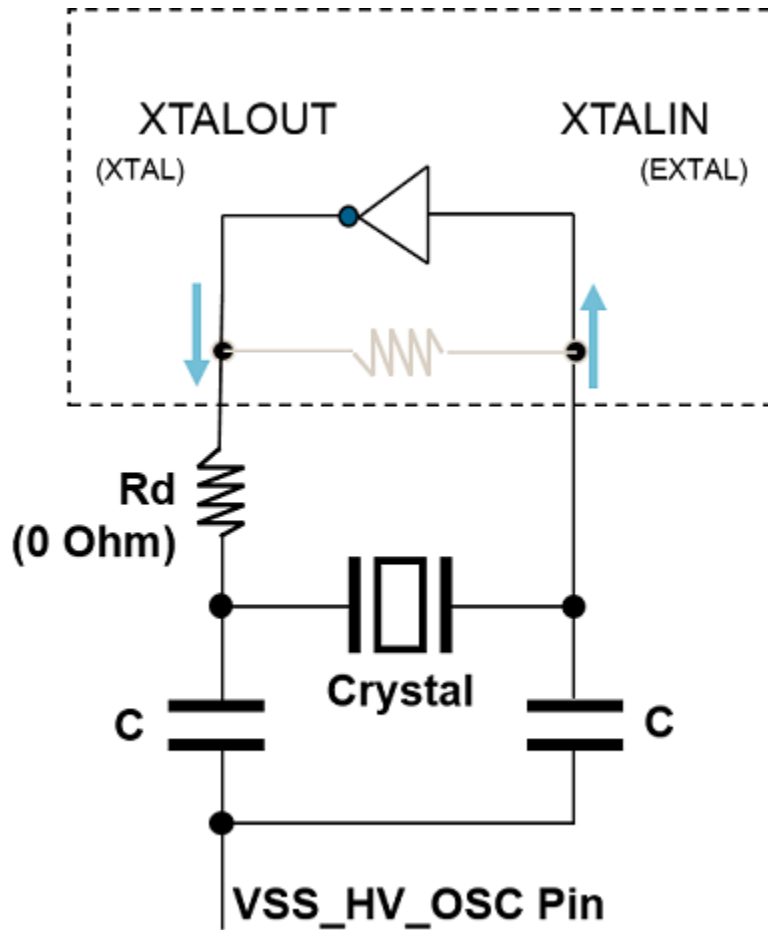
- PDI Fast
- PDI Medium
- DRAM ODT CTL
- DRAM ACC
- DRAM CLK
- DRAM DQ

Please refer to IBIS models and Data Sheet information for more detailed information on IO characteristic. Refer to Data Sheet and Reference Manual on mapping of package pins to pad information.

## 7 Built in Oscillator XOSC

### 7.1 Crystal / Oscillation mode

The crystal is connected between XTALIN and XTALOUT pins, as shown in the figure below:



**Figure 6. Crystal circuitry**

Refer to Data Sheet for internal feedback resistor value.

## 7.2 Bypass mode

In this mode, the analog portion of crystal oscillator (amplifier) is disabled. An external clock, compatible to CMOS levels, can be applied at XTALOUT (XTAL). XTALIN (EXTAL) can be tied to VSS or can be left floating. See the figure below:

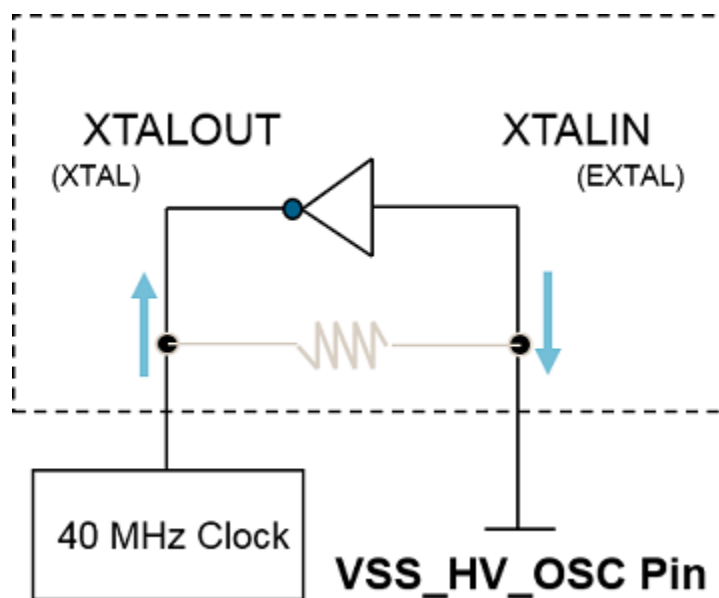


Figure 7. Bypass circuitry

Refer to Data Sheet for internal feedback resistor value.

## 8 Boot configuration pins

MPC5675K provides three boot configuration pins which are evaluated during SoC reset sequence.

Table 3. Boot Configuration Pins

Pin Name	LBGA257 Pad	LBGA473 Pad	Description	Internal weak pull
FAB	P8	Y11	Force Alternate Boot	Pull Down
ABS[0]	D7	C6	Alternate Boot Selection [0]	Pull Down
ABS[2]	C9	C9	Alternate Boot Selection [2]	Pull Down

Boot configuration pins can be used as GPIOs or alternate functions **after boot**. For "normal" booting from internal flash (FAB=0), make sure that internal weak pull down is strong enough for potential leakage current generated by external circuitry connected to FAB pin.

Table 4. Boot possibility

Boot Configuration Pins			Boot Options	
FAB	ABS [2]	ABS [0]	Auto Baud	Boot type
0	X	X	-	Normal boot from internal flash controlled by SSCM. No serial boot loading. No BAM code is executed.
1	0	0	No	Serial Boot via LINFlex_0
1	0	1	No	Serial Boot via FlexCAN_0

Table continues on the next page...

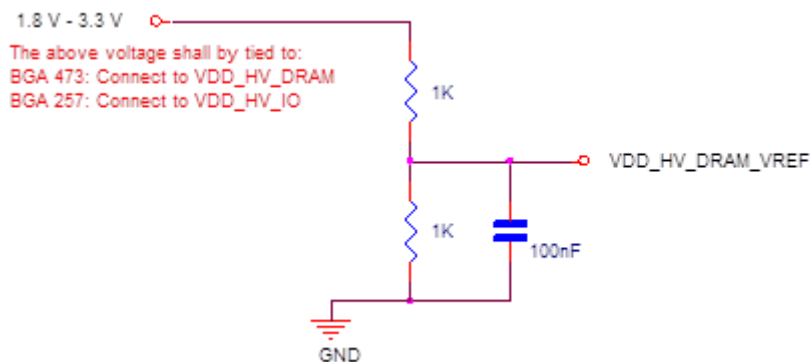
**Table 4. Boot possibility (continued)**

Boot Configuration Pins			Boot Options	
FAB	ABS [2]	ABS [0]	Auto Baud	Boot type
1	1	0	Yes	Serial boot via LINFlex_0 or FlexCAN_0 with autobaud support for each peripheral. The serial boot loading is executed by the peripheral answering to a boot load request.
1	1	1	-	Reserved. BAM places the device in Safe Mode.

## 9 Special signals

### DRAM Reference Pin

- Always needs valid reference level even if DRAM interface is not used.
- Voltage level on this pin is used as comparator reference for DRAM input pads. All alternate functions available on DRAM pins are affected by that.
- BGA 473:
  - Provide 50% voltage level of VDD\_HV\_DRAM to VDD\_HV\_DRAM\_VREF
- BGA 257:
  - Provide 50% voltage level of VDD\_HV\_IO to VDD\_HV\_DRAM\_VREF



**Figure 8. DRAM Reference Pin Circuitry**

Unused Pins (not used in application but present on SoC) are recommended to be put in this configuration:

- Output buffer disabled
- Input buffer disabled
- Weak Pull Down enabled

Reserved Pins (no functionality provided by SoC):

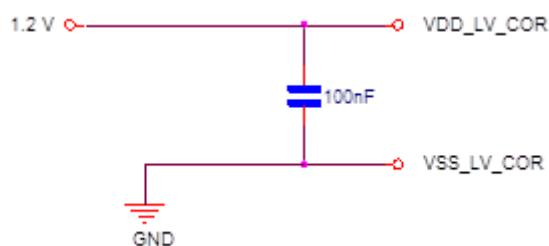
- Reserved pins are internally not connected.
- It is recommended to leave them floating for future compatibility.

## 10 Decoupling

## 10.1 Core supply

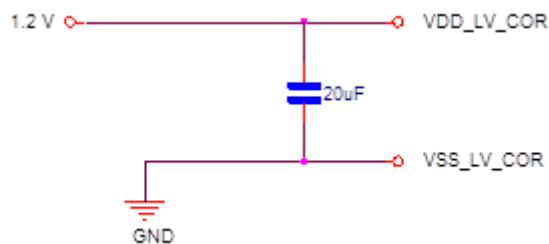
### 10.1.1 Internal VREG mode

Place 100 nF circuitry 8 times as close as possible to VDD\_LV\_COR and VSS\_LV\_COR pins. Ideal placement at bottom side of PCB between center ball matrix and IO ring.



**Figure 9. Core supply decoupling circuitry in internal VREG mode**

Place 20  $\mu$ F circuitry as close to the coil of the VREG circuitry as possible.



**Figure 10. Core supply bust capacitor circuitry**

For more information see [Internal VREG mode](#).

### 10.1.2 External VREG mode

Place four times the circuitry from the figure [Figure 11](#) as close as possible to VDD\_LV\_COR and VSS\_LV\_COR pins. Ideal placement at bottom side of PCB between center ball matrix and IO ring. One 2.2  $\mu$ F per package side.

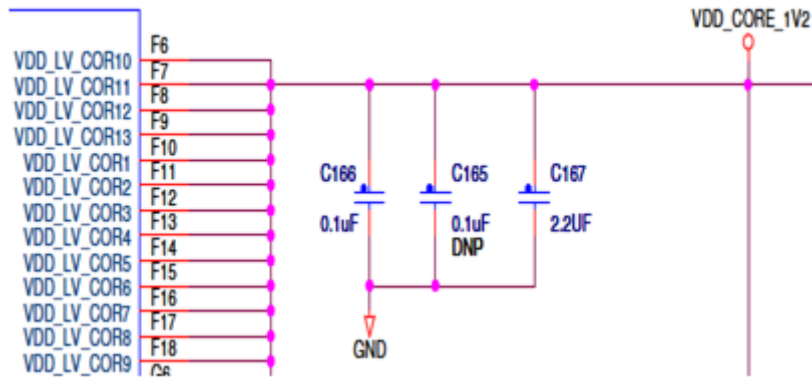


Figure 11. Core supply decoupling circuitry in external VREG mode

For more information see [External VREG mode](#)

### 10.1.3 PLL supply

Place caps as close to the corresponding VDD and VSS pin pair. The decoupling circuitry is shown in the figure below:

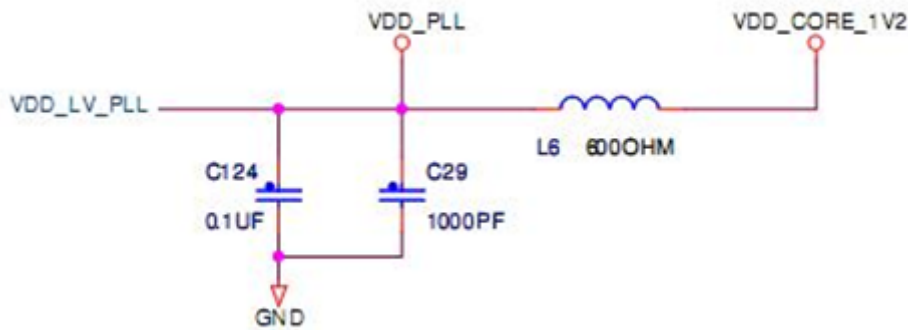


Figure 12. PLL supply decoupling circuitry

## 10.2 Flash Power supply

Place caps as close as possible to the corresponding VDD and VSS pin pair.

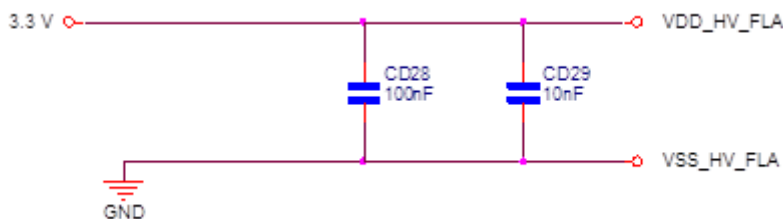


Figure 13. Flash supply decoupling circuitry

## 10.3 Oscillator supply

Place caps as close as possible to the corresponding VDD and VSS pin pair.

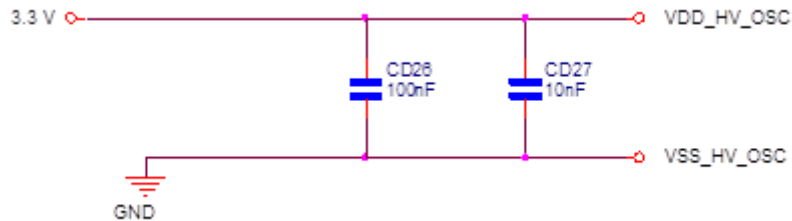


Figure 14. Oscillator supply decoupling circuitry

## 10.4 Parallel digital interface supply

Place caps (2x) as close as possible to the corresponding VDD and VSS pin pair.

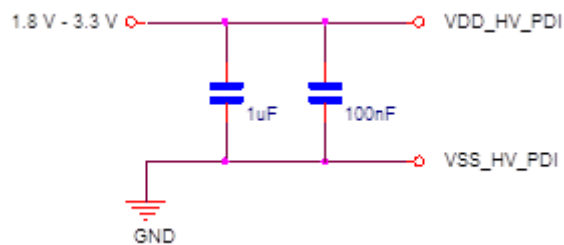


Figure 15. PDI supply decoupling circuitry

## 10.5 DRAM

### 10.5.1 DRAM supply

Place caps as close as possible to their corresponding VDD and VSS pin pairs, 4 pairs in total.

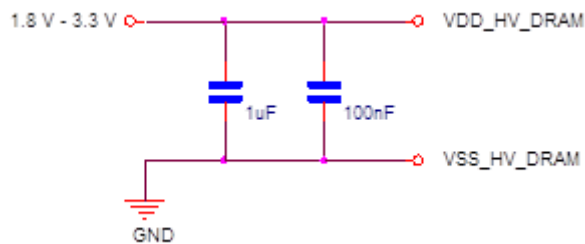


Figure 16. DRAM supply decoupling circuitry

## 10.5.2 DRAM reference supply

Place the circuitry from figure below close to VDD\_HV\_DRAM\_VREF pin. VDD\_HV\_DRAM\_VREF needs to be supplied with 50% of the supply used for VDD\_HV\_DRAM (BGA473) or 50% of the supply used for VDD\_HV\_IO ( BGA 257). VDD\_HV\_DRAM\_VREF needs to be supplied with a valid voltage level even if the DRAM interface is not used and pins are used with an alternate function.

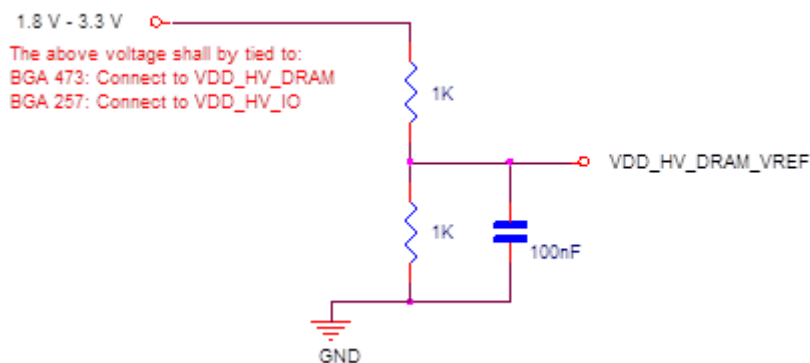


Figure 17. DRAM Reference supply decoupling circuitry

## 10.5.3 DRAM VTT supply

Recommended DRAM memory type is mobile DDR which does not use On Die Termination (ODT). Tie VDD\_HV\_DRAM\_VTT to GND. Disable ODT by software if not used.

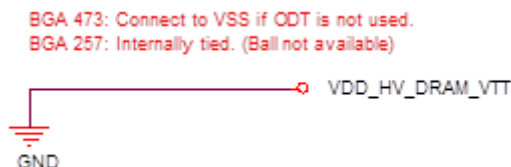


Figure 18. DRAM VTT supply circuitry

## 10.6 General purpose IO supply



Place nF/pF caps as close as possible to the corresponding VDD and VSS pin pair, the values of capacitors depends on the frequency of switching interface.

## 10.6.1 High frequency switching interfaces

For BGA473:

- High speed: A3& C1 (A1, A2, B1, B2), G2 (H2), M4 (L4), U22 (V22), P23 (P22), L23 (L22), H22 (H23), A14 (B14)

For BGA257:

- High speed: High speed or low speed recommendation depends on pin usage in customer application and external load.

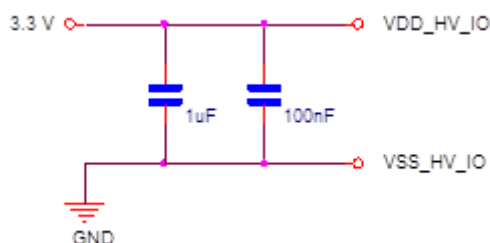


Figure 19. High frequency switching interfaces decoupling circuitry

## 10.6.2 Low frequency switching interfaces

BGA473:

- Low speed: D8 (D9), M2 (N2), T4 (R4), V2 (W2), AB2 (AB1, AC1, AC2), Y13 (Y12), Y20 (AA21), AB22 (AB23, AC22, AC23), L20 (K20), B22 (A22, A23, B23)

BGA257:

- Low speed: High speed or low speed recommendation depends on pin usage in customer application and external load

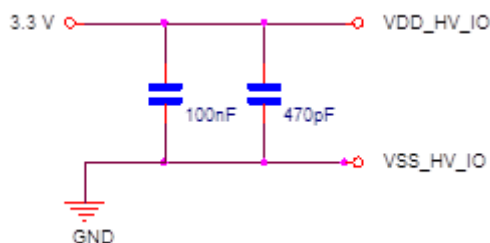


Figure 20. Low frequency switching interfaces decoupling circuitry

## 10.7 ADC

VDD\_HV\_ADV as common ADC supply (3.3 V). VDD\_HV\_ADRx as ADC reference voltage (3.3 V or 5.0 V). All references supplies must be at the same supply level - either 3.3 V or 5.0 V.

ADC channels alternatively available as general purpose digital inputs.

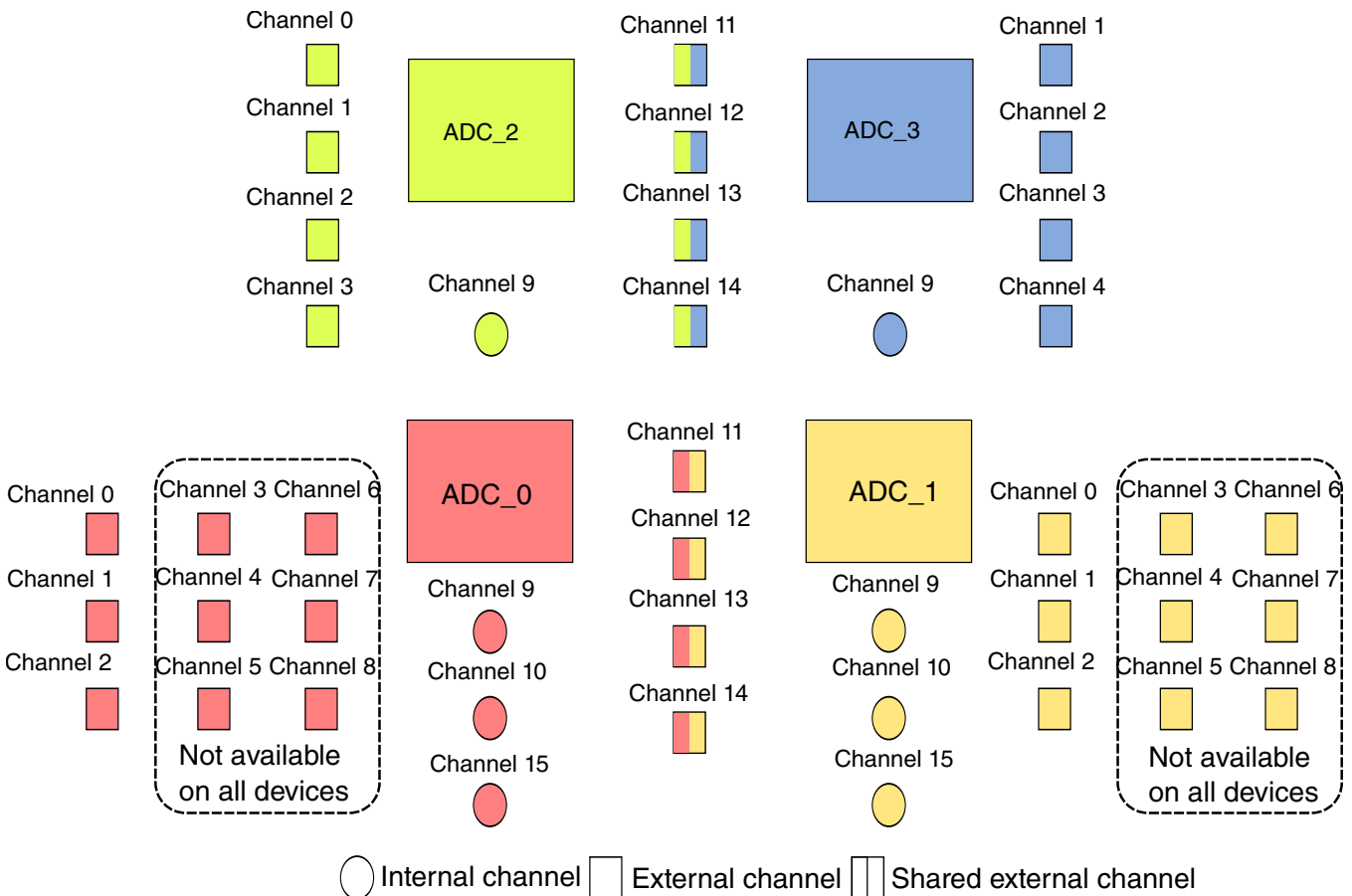
## Decoupling

- Digital signal input levels allowed up to VDD\_HV\_ADRx
- Digital input thresholds as for 3.3 V CMOS inputs independent of VDD\_HV\_ADRx level

Both packages allow four simultaneous A/D conversions. Four common channels are shared between two ADCs. For detailed calculation of required ADC channel input circuitries please refer to MPC5675K DS and RM.

**Table 5. Number of external ADC channels**

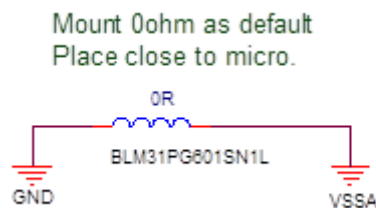
ADC Number	BGA 257	BGA 473	Comment
0	3 channels	9 channels	
0 & 1	4 channels	4 channels	Shared channels. Conversion either by ADC_0 or by ADC_1 because Accurate results cannot be guaranteed if both ADCs are configured to simultaneously sample the same shared channel.
1	3 channels	9 channels	
2	4 channels	4 channels	
2 & 3	4 channels	4 channels	Shared channels. Conversion either by ADC_2 or by ADC_3 because Accurate results cannot be guaranteed if both ADCs are configured to simultaneously sample the same shared channel.
3	4 channels	4 channels	
Total	22 channels	34 channels	



**Figure 21. ADC Channel muxing**

## 10.7.1 ADC ground

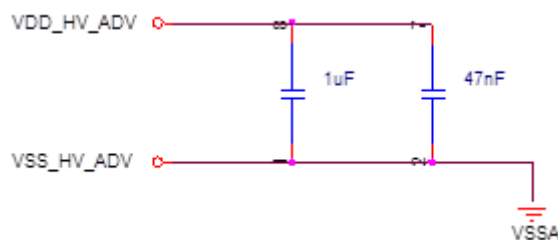
Create analog GND for the ADC as shown in figure below.



**Figure 22. Creating analog ground for ADC**

## 10.7.2 ADC supply voltage

Shared among all four ADCs. Voltage supply must be at 3.3 V. Place 1  $\mu\text{F}$  + 47 nF capacitor pair close between VDD\_HV\_ADV and VSS\_HV\_ADV supply pins.



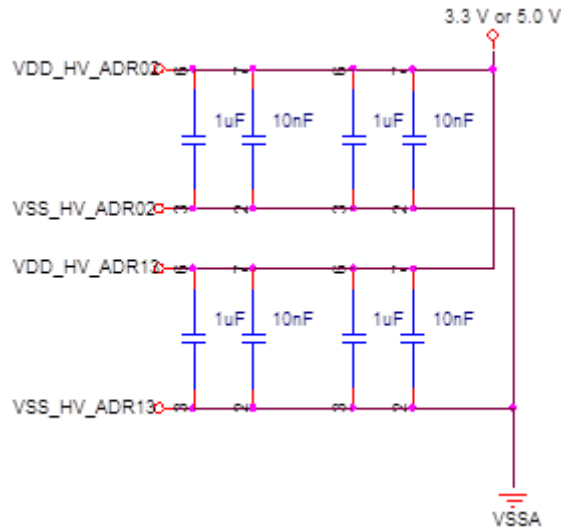
**Figure 23. ADC Supply Voltage Decoupling**

## 10.7.3 ADC reference voltage

Reference supply can be 3.3 V or 5.0 V. All references supplies must be at the same supply either 3.3 V or 5.0 V.

Reference Voltage Supply BGA 257:

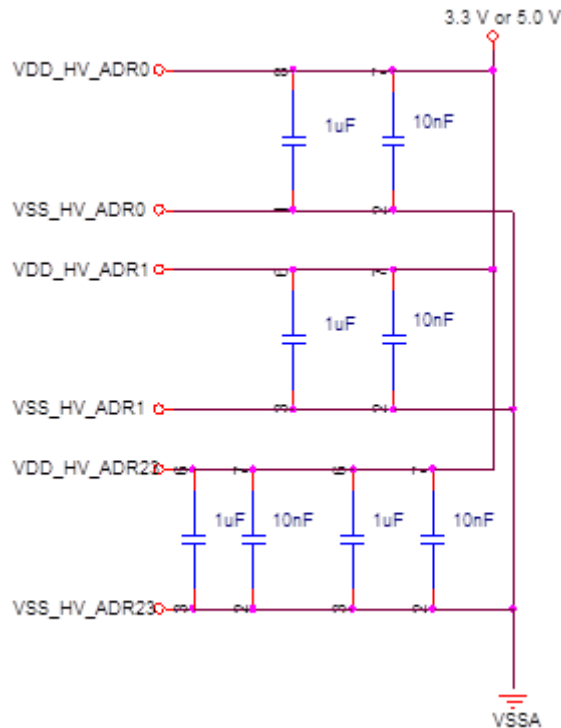
- ADC\_0 and ADC\_2:
  - Share VDD\_HV\_ADR02, VSS\_HV\_ADR02
  - Place two 1  $\mu\text{F}$  + 10 nF capacitor pair close to these supply pins
- ADC\_1 and ADC\_3:
  - Share VDD\_HV\_ADR13, VSS\_HV\_ADR13
  - Place two 1  $\mu\text{F}$  + 10 nF capacitor pair close to these supply pins



**Figure 24. ADC Reference voltage supply decoupling (BGA257 package)**

Reference Voltage Supply BGA 473

- Reference Voltage Supply BGA 473
  - Place one 1  $\mu$ F + 10 nF capacitor pair close to these supply pins
- ADC\_1: VDD\_HV\_ADR1, VSS\_HV\_ADR0 (separated reference)
  - Place one 1  $\mu$ F + 10 nF capacitor pair close to these supply pins
- ADC\_2 and ADC\_3:
  - Share VDD\_HV\_ADR23, VSS\_HV\_ADR23
  - Place two 1  $\mu$ F + 10 nF capacitor pair close to these supply pins



**Figure 25. ADC Reference voltage supply decoupling (BGA473 package)**

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