

MPC5606E: Design for Performance and Electromagnetic Compatibility

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1. Introduction

This document provides information about designing automotive board with MPC5606E. It details the key design consideration, the PCB layout and components selection. This document is focus on Broadcom part of MPC5606E the BroadR-reach interface.

This document is intended primarily for hardware-design engineers, printed-circuit layout engineers and system engineers interested in designing products that contain automotive BroadR-Reach.

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2. Overview

The purpose of this document is to summarize and update the results of design work in the field of electromagnetics compatibility (EMC), which led to the successful implementation of MPC5606E with Boradcom BroadR-Reach Ethernet in automotive applications. It includes a summary of the applied automotive EMC requirements and detailed description of the design recommendations for meeting them.

3. Exploring the MPC5606E Reference board 6-layer design

NOTE

The main design considerations are described here using the example of the 6-layer Freescale automotive BroadR-Reach board. For best performance, it is critical to closely follow these design guidelines.

NOTE

Use this document in conjunction with the reference board schematic and layout files. For generic design guidelines, refer to the documents available at the following link:

http://cache.freescale.com/files/training/doc/dwf/AMF_AUT_T0750.pdf

This board has been designed with a relatively conservative approach to maximize the performance. It is reflected in the number of PCB layers, their designation, and in selection of the filtering components on the board.

3.1. PCB Stackup

A 6-layer construction is used, as shown in [Figure 1](#). Special attention has been made that all signal traces and all power nets to always have a logic zero (GND) plane in the adjacent layer, and that there is one main power distribution layer. Routing signal traces adjacent to any voltage plane or shape is not recommended. This PCB stackup and layout arrangement are designed to avoid such routing.

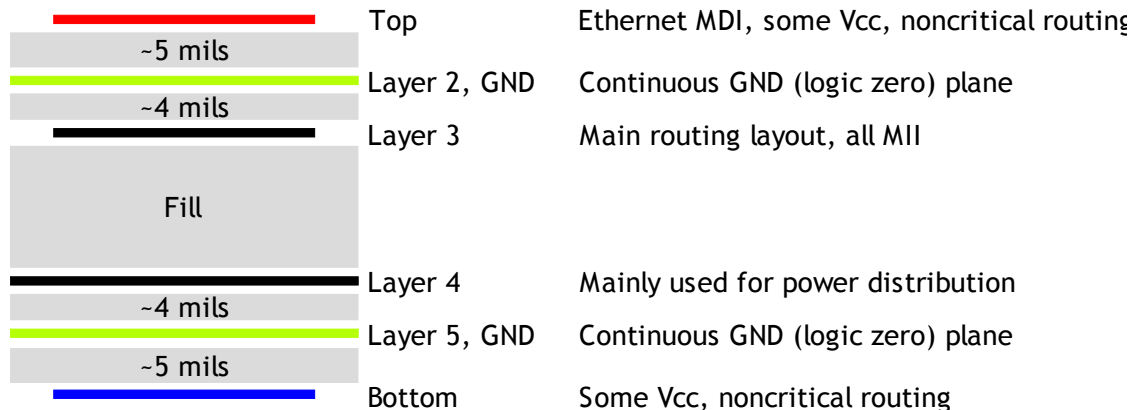


Figure 1. Layers arrangement in 6-layer stackup

3.2. 6-Layer PCB Overview-Layer by Layer

3.2.1. Layer 1 (Top layer)

The top layer shown in [Figure 2](#) contains the main components and most of the analog BroadR-Reach routing.

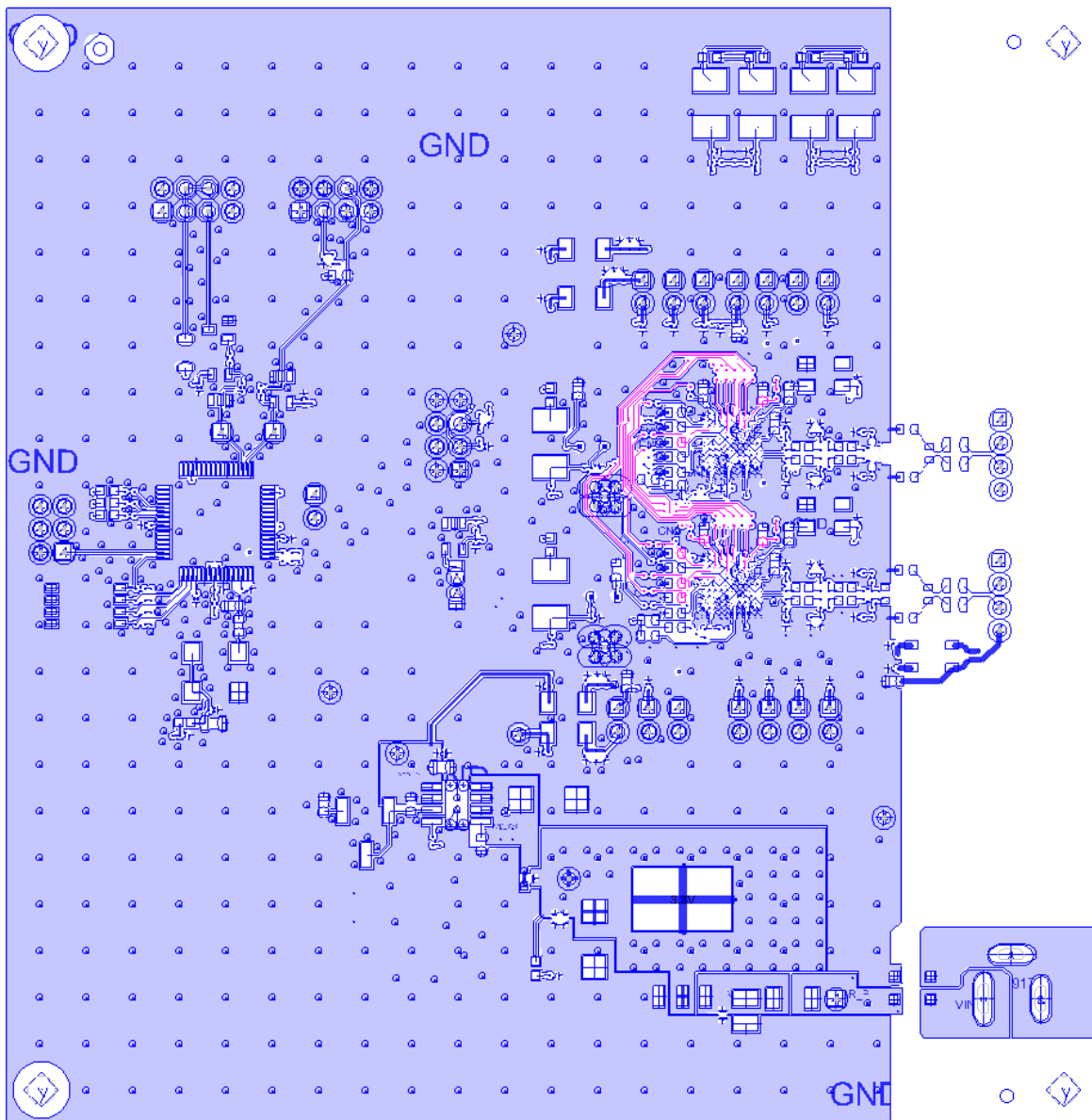


Figure 2. 6-Layer PCB – Layer 1 (Top Layer)

The routing of any high-speed or critical traces on top layer is minimized, allowing only for the shortest necessary lengths to escape from the components. The main concern here is the MII routing (signals, clocks, power supply). Testing shows that filter capacitors and series resistors on the MII lines are not required and the signal can be connected directly. The optional MII signal-filtering components are placed on the top layer to avoid transition of these signals between the top and bottom layers.

MII interface is the common source of radiated emission from Ethernet devices (harmonic of the 25 MHz clock). It is critical for good EMC performance to take utmost care of routing this interface. All MII routing is placed in the top layer. The MII signal traces are shown in purple color. For additional EMC improvement, route MII trace on layer 3.

VDD_3V3 is generated by linear regulator. It has large size that aids heat dissipation. The 3.3V shapes on the top layer and layer 3 are well connected with multiple vias to aid heat dissipation.

3.2.2. Layer 2 and Layer 5 (GND)

In a 6-layer PCB, layer 2 and layer 5 are identical (see [Figure 3](#) for layer 2 and [Figure 4](#) for layer 5). They both contain GND planes, which are continuous under the entire board except under the following areas:

- BroadR-Reach Ethernet signal common-mode choke and power-supply common-mode choke
- BroadR-Reach connector (Molex Mini50) and power connector
- Traces that connect the common-mode chokes and the connectors

GND-fills in all other layers are well connected to the main GND planes with many vias. The edges of the GND shapes are connected together with multiple vias.

NOTE

Logic zero (GND) is shown in blue color on all layers.

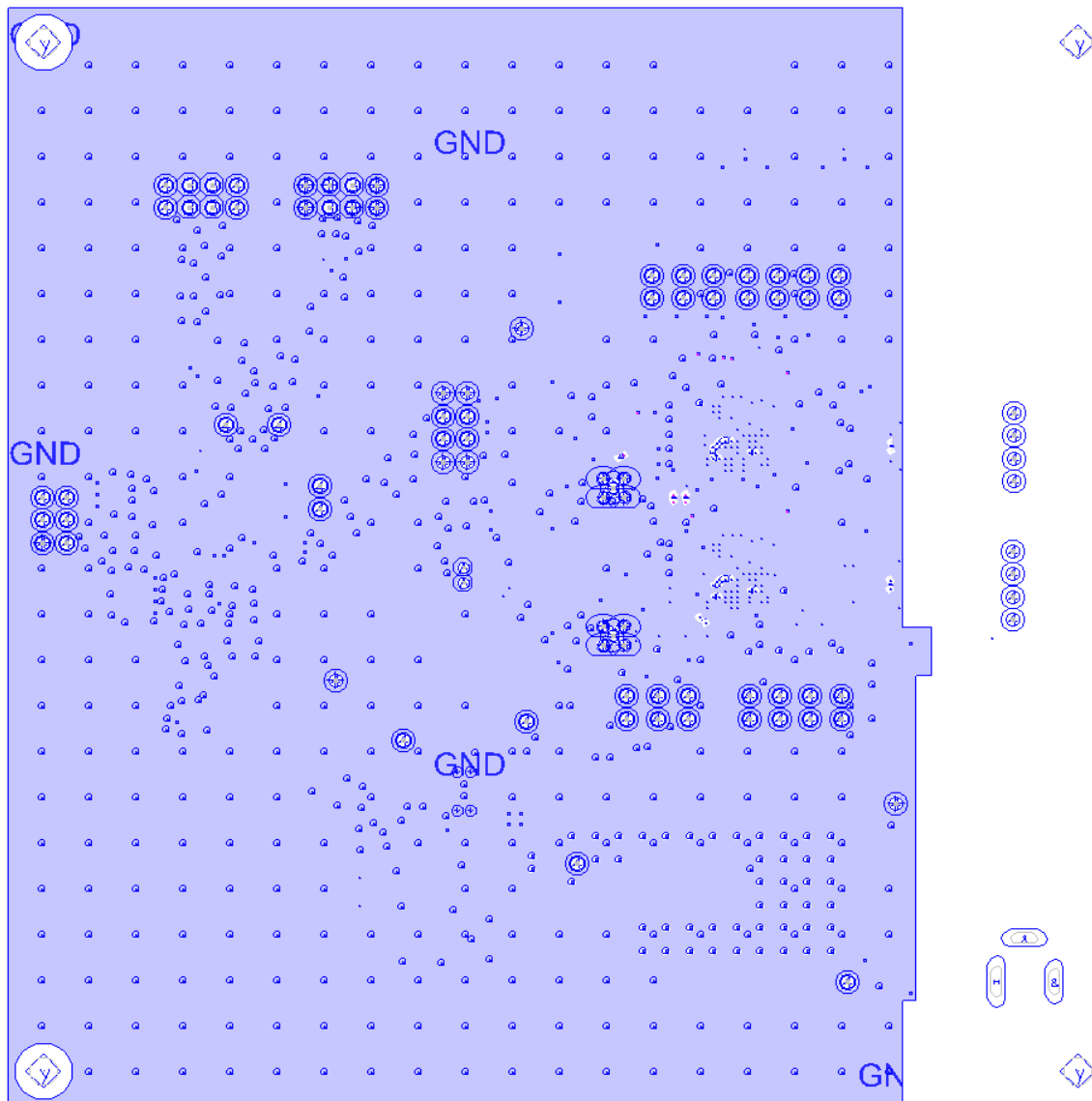


Figure 3. 6-layer PCB - Layer 2 (GND)

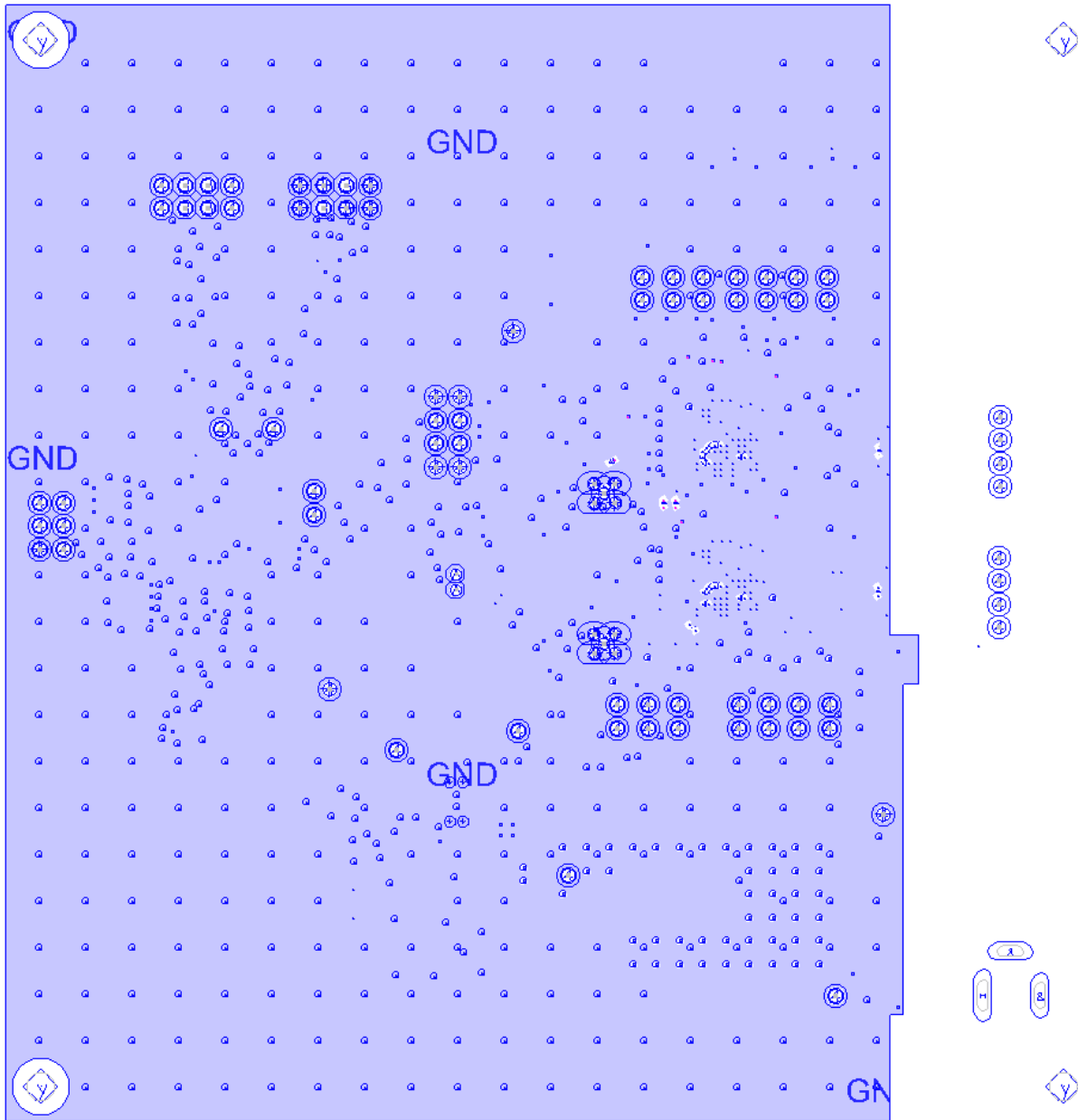


Figure 4. 6-Layer PCB – Layer 5 (GND)

NOTE

The area under the common-mode choke and under the DC-block capacitors, including the area under the connector, is voided of any other routing or planes as an example of a design without a shielded enclosure. However, if there is another PC board under that area, for example, in stacked PC boards often used for automotive cameras or if the board is completely enclosed in a metal enclosure, it is recommended to keep the GND plane continuous under the entire I/O section and well-connected to the metal enclosure (shield).

3.2.3. Layer 3 (internal layer)

Layer 3 is the best routing layer, dedicated to all critical and high-speed or noisy nets as shown in [Figure 5](#).

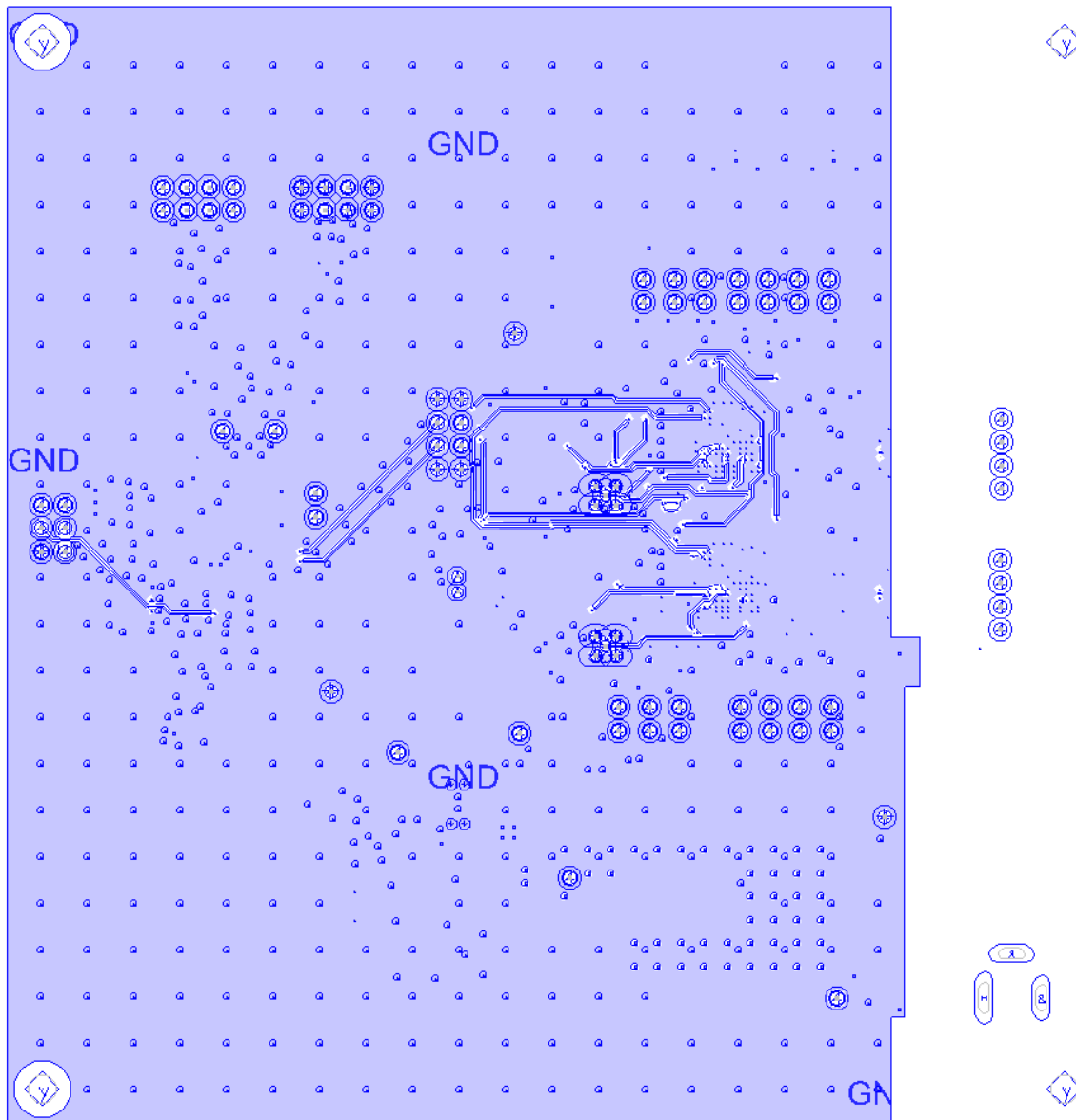


Figure 5. 6-Layer PCB – Layer 3 (Critical signals)

3.2.4. Layer 4 (power distribution)

The main supply nets for each PHY (OVDD_U7 and OVDD_U9) are in layer 4 as shown in [Figure 6](#). OVDD_U7 and OVDD_U9 are separated from the main power supply (VDD_3V3) by ferrite beads. Power pins of each PHY are grouped and further filtered by ferrite beads. 0 Ω resistors can be used if testing shows that some ferrite beads are not required.

The MII power supply of MPC5606E, OVDD_MII*, can be very noisy. Its size is, therefore, minimized (in red as shown in the following figure). For additional EMC improvement, route MII power supply trace on layer 3.

The size of each power supply net is minimized. It only cover the approximate area where the power is needed. The power supply nets do not go near (or under) any I/O sections and do not go near the edges of the board.

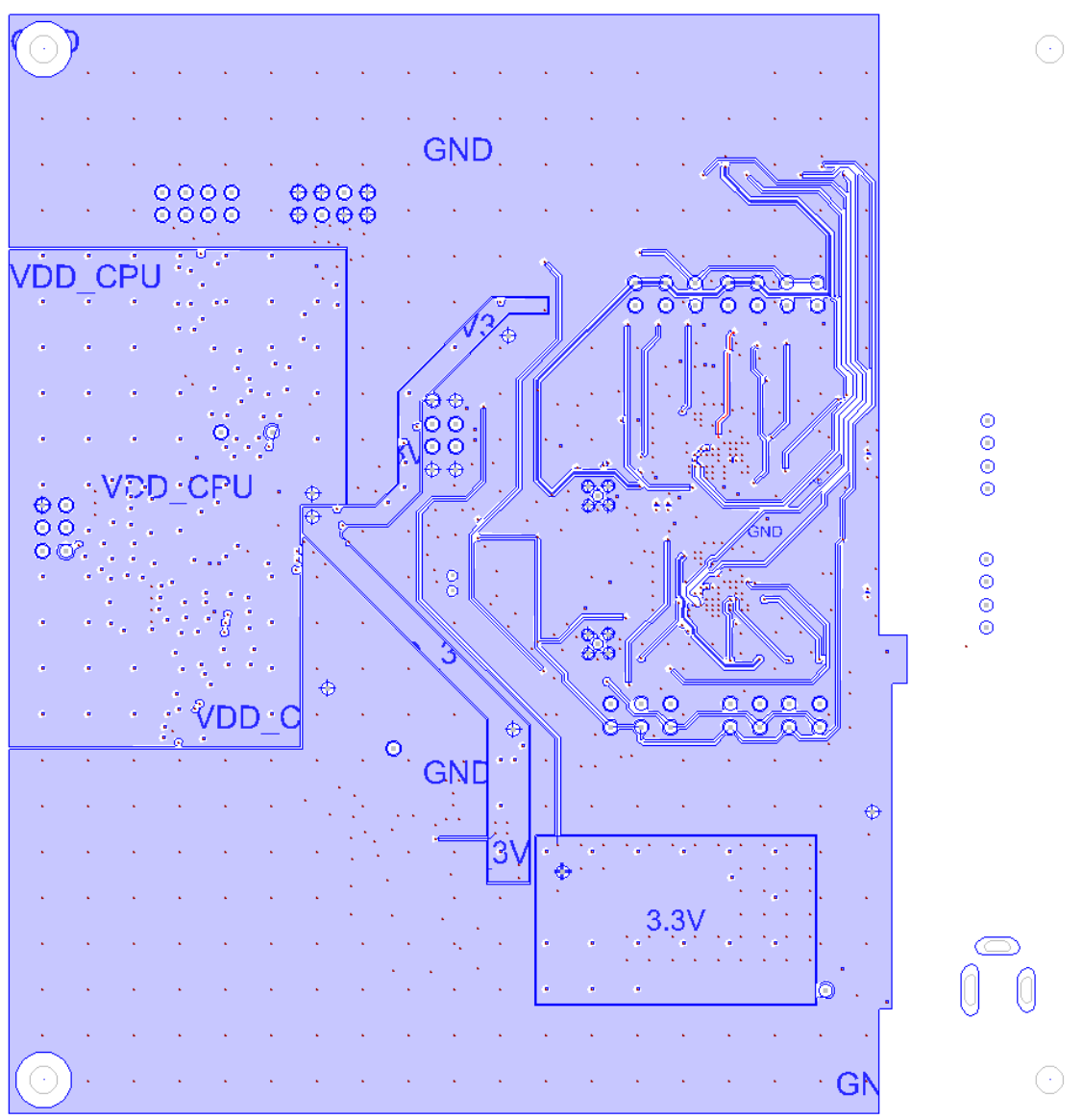


Figure 6. 6-Layer PCB – Layer 4 (Power)

3.2.5. Layer 6 (bottom layer)

Layer 6 is the bottom layer and contains only small SMD components as shown in Figure 7. The MII power supply of MPC5606E, OVDD_MII*, can be very noisy. Its size is, therefore, minimized (in red as shown in the following figure). For additional EMC improvement rout MII power supply trace on

layer 3. The OVDD_MII* nets are shown in the red. They are small nets (wide traces) separated from any other nets by filtering components (a ferrite bead and a resistor) and by distance.

Decoupling capacitors:

- Capacitors for U7 and U9 decoupling are placed on layer 6 as close as possible under the respective power supply pins.
- 0402-size capacitors with via-in-pad are used for the best placement and to minimize the mounted inductance of the capacitors.

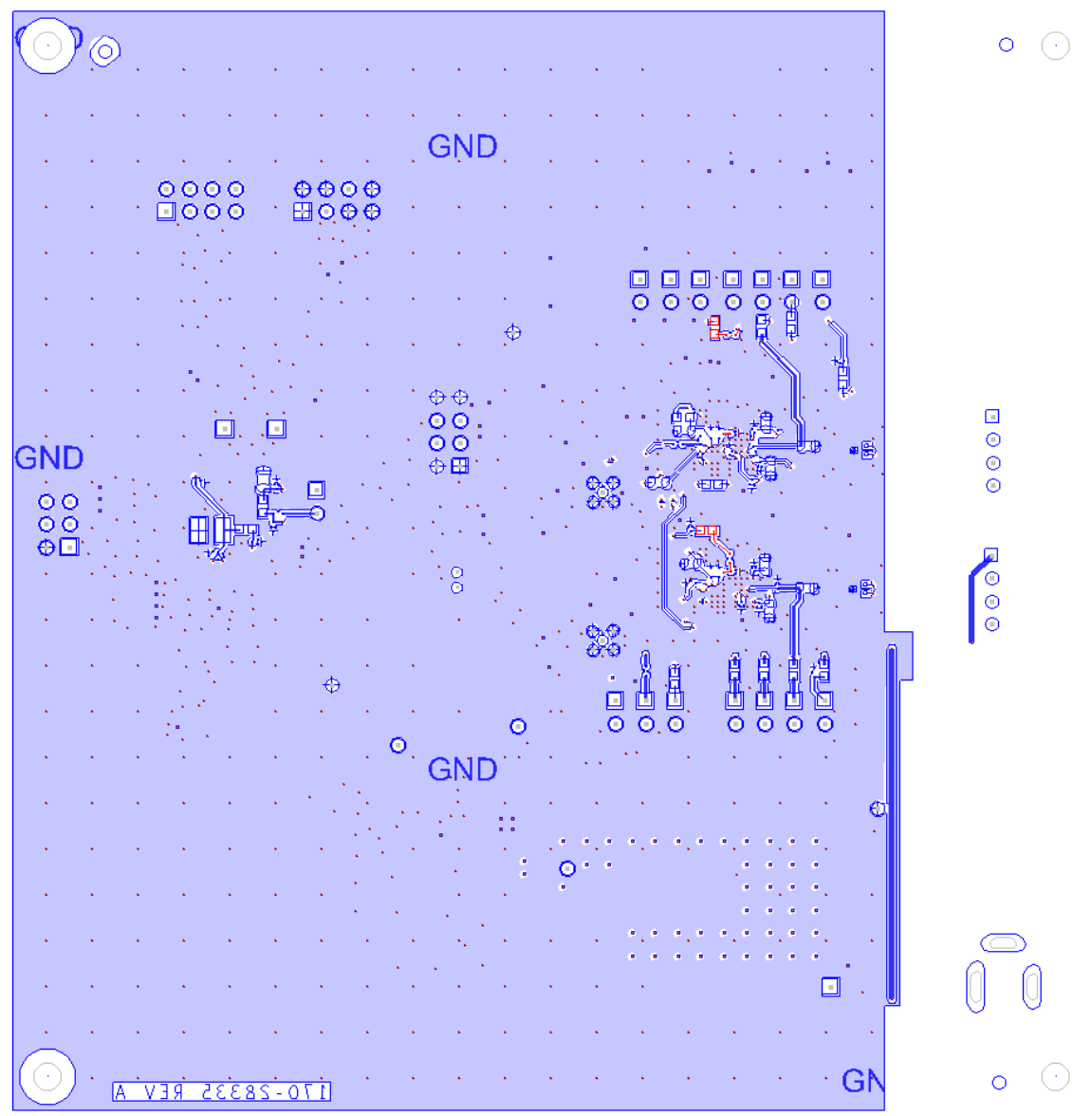


Figure 7. 6-layer PCB – Layout 6 (Bottom)

4. Power Distribution

All power groups on the BMC89810 transceiver part of the MPC5606E are filtered with ferrite beads as shown in Figure 8.

The following guidelines should be followed:

- Do not overlap the power nets from two sides of ferrite beads in layout (filtered and non-filtered supplies).
- Limit the size of each local power distribution only to the minimum necessary area.
- Filter the power supply for each IC used on the board separately.
- It may be possible to remove some of the ferrite beads and replace them with 0 Ω resistors. However, it is recommended to layout the board with these components in place to begin with.

NOTE

Separating the MII supply (OVDD_3V3 and OVDD_RGMII_3V3 pins on the BCM89810 part of the MPC5606E) with resistor and a ferrite bead should always be considered.

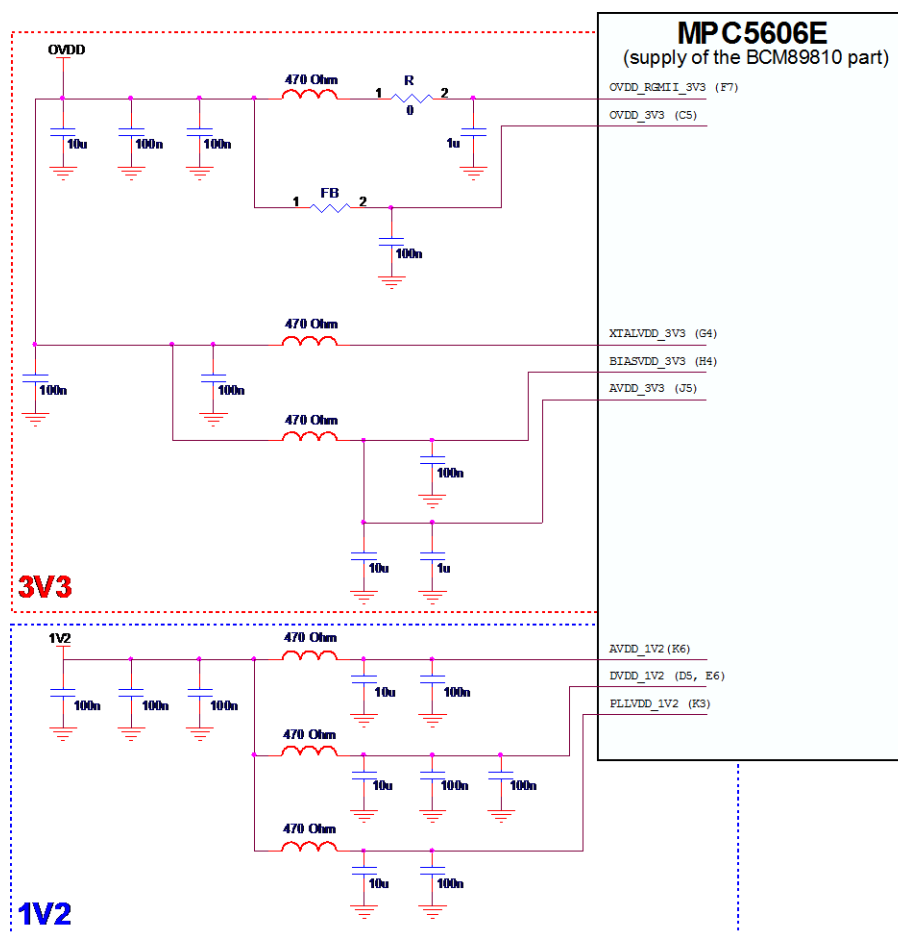


Figure 8. Power distribution of BCM89810 part of MPC5606E

4.1. OVDD MII Layout

The xMII power (OVDD) requires special attention. [Figure 9](#) shows the layout of the OVDD_MII power supply net (If the serial resistor is used, OVDD_MII is only the green layout when the serial resistor is not used (0 Ω resistor) the OVDD_MII is green and red layout.).

OVDD_MII is derived from the OVDD voltage, through a ferrite bead and an optional resistor. On eof the decoupling capacitor on the OVDD_MII pin is connected directly between the OVDD pin of the device and the GND paddle under the device. In order to minimize the mounted inductance, via-in-pad geometry can be used on 0402 decoupling/bypass and filtering capacitors.

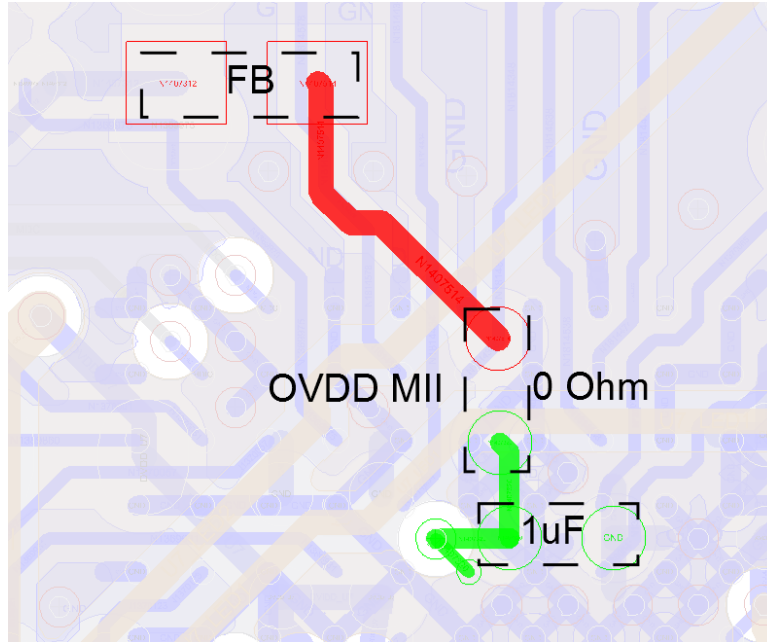


Figure 9. OVDD MII power supply net

4.2. DC power Entry EMI Filtering

The DC power entry in the MPC5606E reference boards has a high-impedance common-mode choke. This is shown in [Figure 10](#). The common-mode choke on this board has been selected with particular attention to the frequency characteristics of the common-mode impedance and compared to the BroadR-Reach signal spectrum.

Because of the low-frequency characteristic of this common-mode choke, a high-frequency ferrite bead and a capacitor are also used in conjunction with it. Select a ferrite bead with a current rating of at least twice the maximum DC current through it.

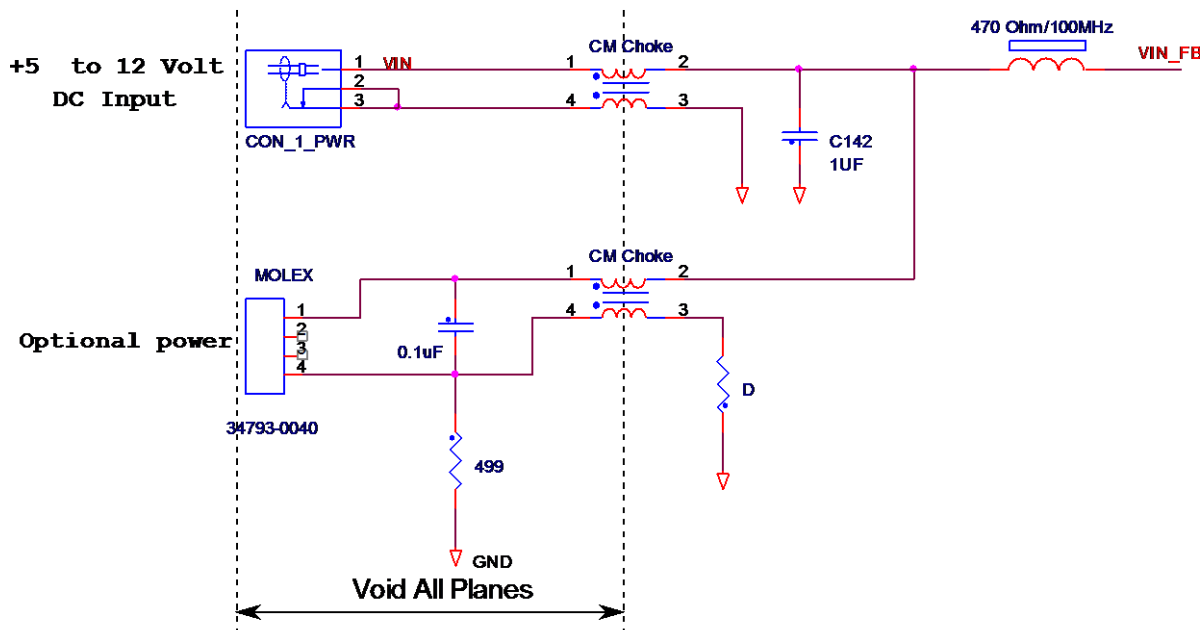


Figure 10. DC connector-section schematic

The area of the PCB under the power connector and all the way to under the common-mode choke needs to be cleared of any routing and planes. This area should only contains traces between the common-mode choke and the connector. Connect the edges of the GND shapes together with multiple vias as shown in Figure 11.

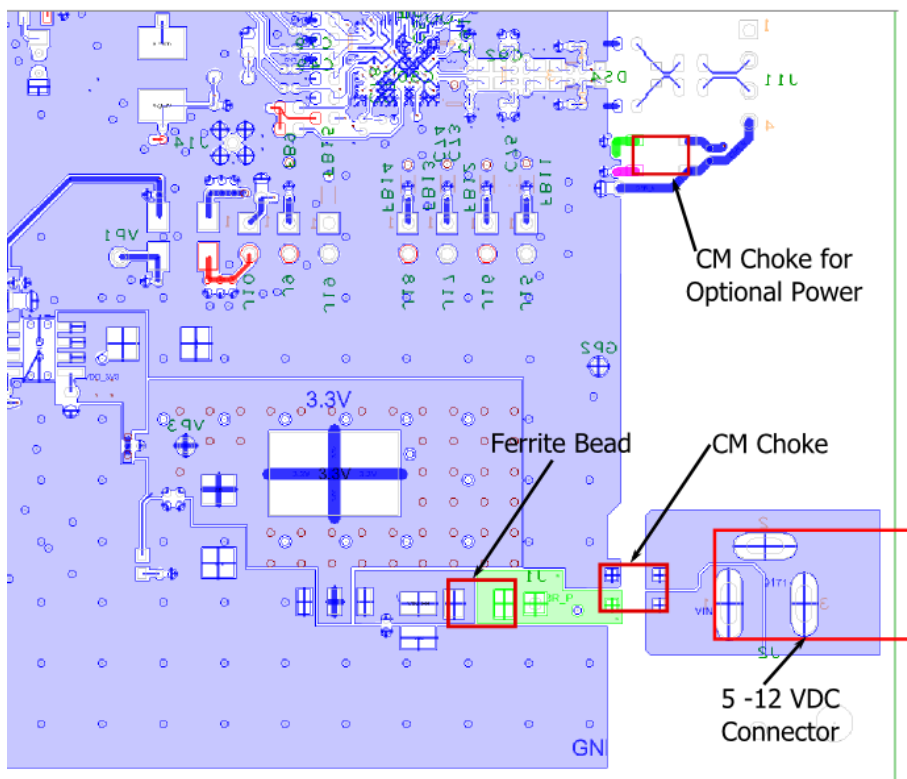


Figure 11. DC Power input Layout-Bottom interface

5. Digital/Critical Signals

Following are the base recommendations:

- Minimize the length of critical traces.
- Use GND planes as a reference for routing all signal traces.
- Do not route any signals in layers next to the voltage layers or shapes.
- Route critical signals mainly in inner layer 3.
- If a change of layers is necessary, add GND-stitching vias immediately next to the signal vias.

Figure 12 shows the MII routing in red.

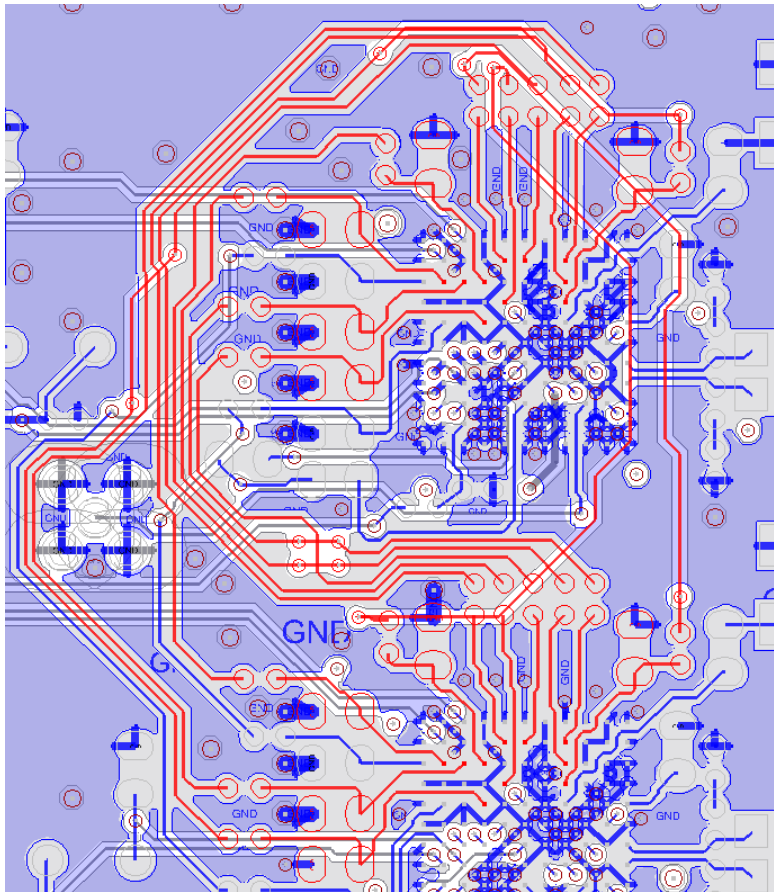


Figure 12. MII routing

Follow these additional considerations:

- Minimize the length of the MII traces.
- All optional MII filter capacitors and series resistors are placed on top layer (the same layer as the MPC5606E transceiver).
- Testing showed that filter capacitors and series resistors on the MII lines are not required.
- The optional series resistors should be placed on the top layers, and connected to layer 3 as close as possible to the pads. You want to minimize the MII traces on the top layer. This will help to minimize EMC from the MII lines.

6. Analog Front-End BroadR-Reach Differential Pair

Figure 13 shows the components used between the PHY and the connector to the signal line:

- Low-pass filter is using 1 % capacitors (0402-size), 1% resistors (0402-size) and 2 % inductors (0603-size).
- Data-line common-mode choke.
- Common-mode termination.
- DC block capacitors.
- Optional low-capacitance ESD diodes.

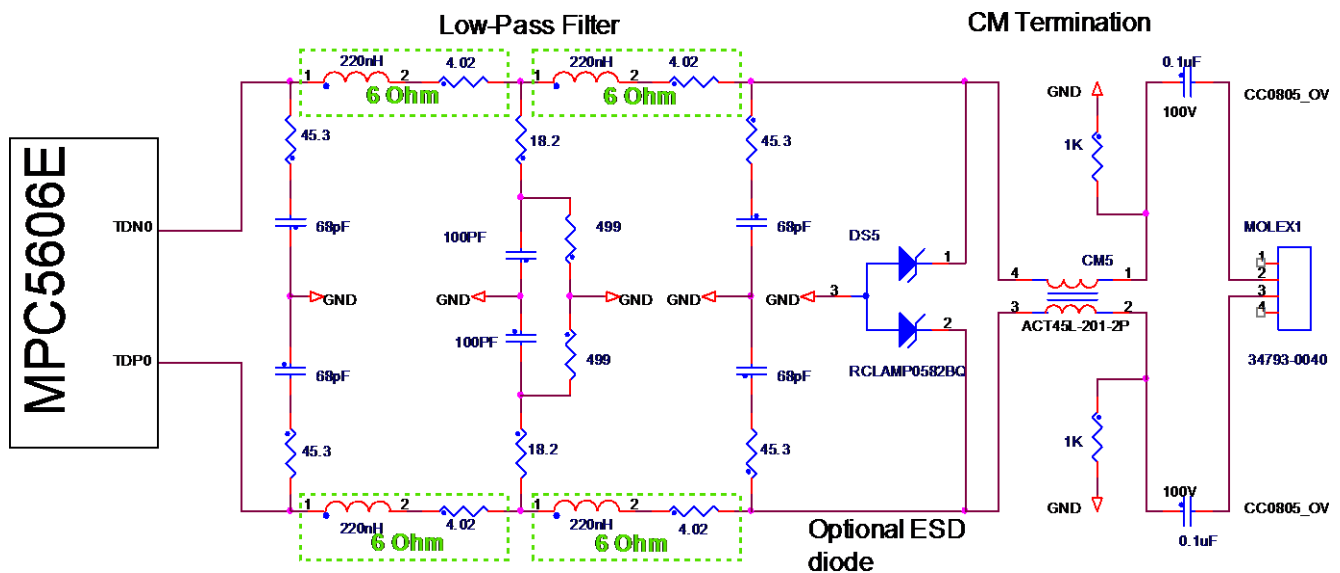


Figure 13. BrodR-Reach EMC filter components

NOTE

In the above figure, the combined DC resistance of the inductor and series resistor should be 6 Ohm.

Following are the recommended common mode chokers:

- TDK ACT45L-201-2P
- Murata DLW43MH201XK2
- Pulse AE2000

Consult with local Field Application Engineer (FAE) for the most current recommendations for component selection or for the contact information for these components.

Depending on ESD requirements, optional bidirectional and low-capacitance (<2pF recommended), ESD-protection diodes (DS5) may be used between the common-mode choke and the low-pass filter. The Semtech RCLAMP0528BQ or equivalent performs is recommended for ESD-protection diodes.

The layout of the differential-pair interface is shown in Figure 14.

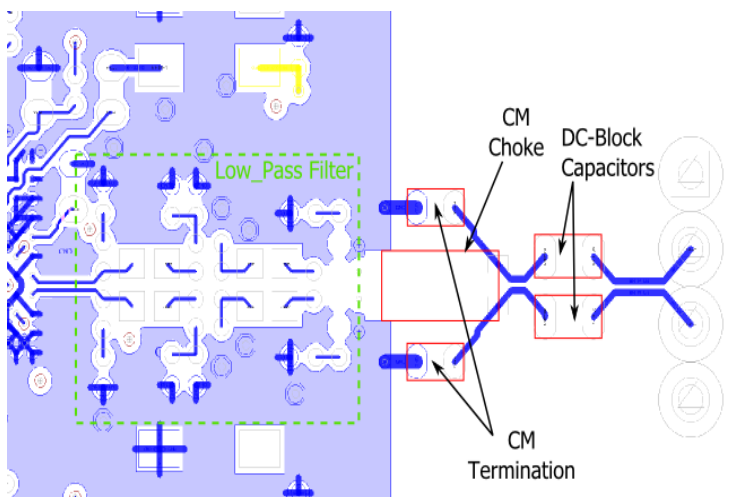


Figure 14. BroadR-Reach front-end layout - top view

The traces are on the top layer. Special attention has to be paid to ensure that the pairs are symmetrical. Placement of the filter components can be on top or bottom, but they must be symmetrically placed and routed.

The target impedance for the differential pairs is 100 Ohm \pm 10%. In the section that voided of any planes, the trace width and spacing are adjusted to keep the target impedance.

To reduce coupling, the inductors of the low-pass filters are spaced away from one another. The minimum recommended spacing between the inductors is equal to the inductor width.

The edges of the GND shapes are connected together with multiple vias.

The length of connection between the BroadR-Reach pair and the common-mode termination resistors should be minimized.

6.1. Connector and Cable

6.1.1. Connector for Twisted-Pair Cable

NOTE

Balance of all components in the differential-signal path is absolutely critical for the EMC performance. The two lines and pins of each differential pair should be kept as close as possible to each other and as far as possible from anything else.

Each of the two Ethernet signal pins in the connector must have the same length. This can be accomplished by selecting two horizontal pins rather than two vertical pins for each pair.

If there are ground and voltage-supply pins in the connector, the relative distance of the pins of each differential pair to the nearby ground or voltage pins must be equal.

It is recommended to provide extra separation between the differential Ethernet signal pins and any other signals, especially aggressive signals that can couple noise into the pins of the twisted-pair interface.

Figure 15 shows an example of a balanced connector pinout on demo board. The BroadR-Reach pair is connected to pins 2 and 3 of the 4-pin connector (Figure 15a). If power supply is used on the same connector, the 12 V and 0 V can be connected through pins 1 and 4 (Figure 15b). Such an arrangement preserves the symmetry of the differential pair, as opposed for example, using pins 1 and 2 for power and pins 3 and 4 (Figure 15c) for the differential signal which results in an unsymmetrical arrangement.

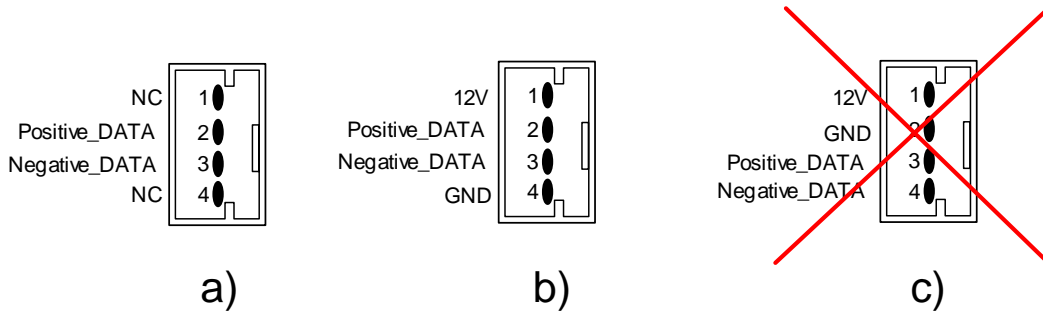


Figure 15. BroadR - Reach connector

Figure 16 shows an example of a suggested connector pinout guideline. The two pins of each pair have the same length (see side view of Figure 16) to keep them balanced. It is suggested to leave the extra pins in the section unused or used only for the signals that do not interfere with the BroadR-Reach Ethernet application. In case these pins are used or in case the pairs are placed on top of another, an analysis of the particular connector and its effects should be done, which is beyond the scope of this document.

NOTE

For further information on how connector pinout can affect functional and EMC performance, refer to Broadcom docSAFE site.

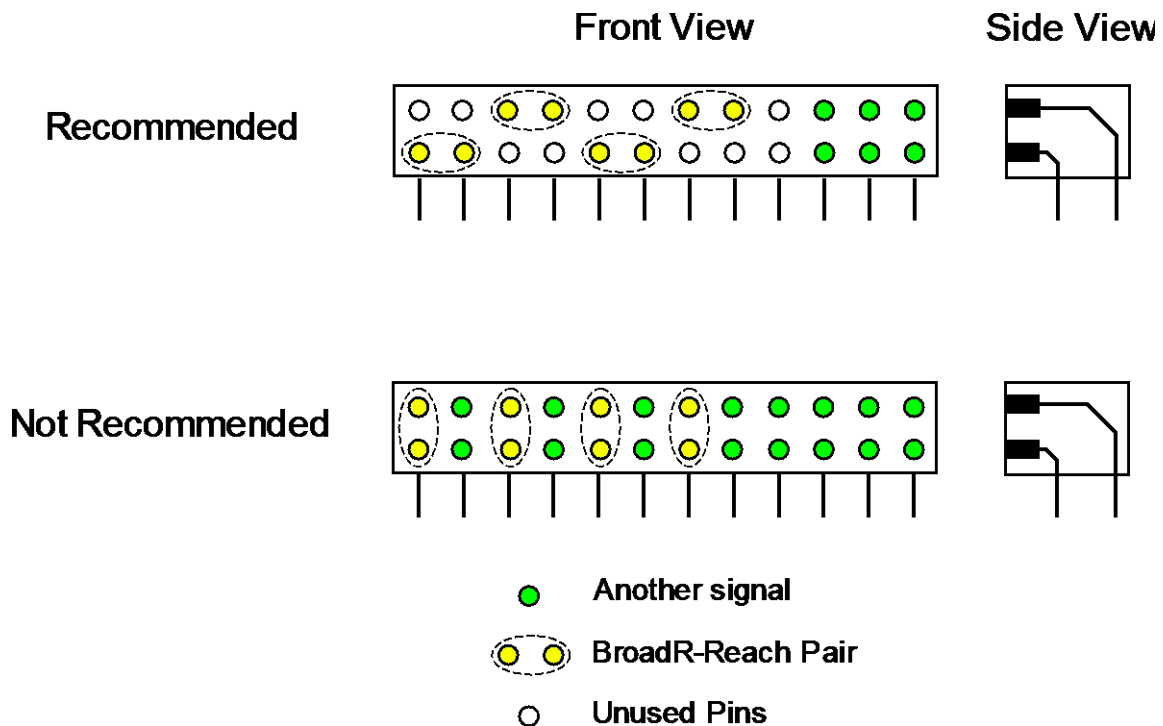


Figure 16. Examples of recommended and not recommended connector pinout

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6.1.2. Twisted-Pair Cable

Unshielded twisted-pair cables are recommended for BroadR-Reach interface. A well-balanced and well-twisted differential-pair cable with characteristic impedance of 100 Ohm \pm 10 % must be used. Other factors to consider are degradation of the cable parameters with temperature as well as presence or lack of a jacket that can provide protection from the environment and mechanical stress.

7. Small Form-Factor Stacked Boards (Camera Example)

The automotive environment often requires a small form-factor stacked board application (such as camera system), where the previous design recommendations cannot be followed completely. In a stacked board environment, noisy from one PCB can be coupled to other PCBs. In this case, a cleared GND area in the I/O section should not be used because of such coupling. PCB GND planes connected to an enclosure or shield can be used to isolate the I/O section (common mode chokes, filters, and cables) from the noise inside the system (digital signals and power supplies). Thin metal liners can provide additional shielding and separation between the boards. [Figure 17](#) and [Figure 18](#) are illustrate example of a stacked board application. These are generic examples and suggestions for stacked board applications.

[Figure 17](#) shows the following main effects that can cause strong emissions from the data and power cable:

- Common-mode voltages VCM, especially on the I/O board.
- Unprotected I/O board and cleared (no planes) section with exposed I/O signals.
- Capacitive coupling between boards (and ICs).
- Voltage induced from the inductance of the connector pins.

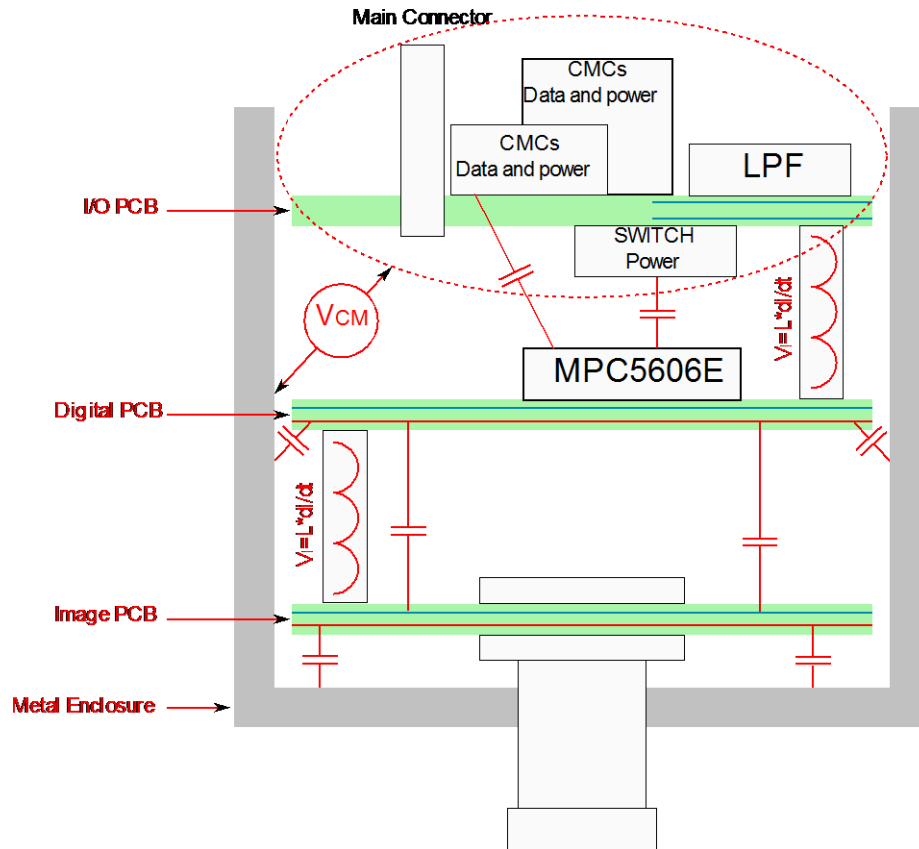


Figure 17. Sources of emission from stacked boards (Camera example)

One suggestion for design and arrangement of stacked boards is shown in Figure 18. This figure is an illustrative example that shows some possible ways to reduce emission from stacked boards rather than details of practical implementation. Many ways of practical realization can be devised, but it is recommended to follow this general idea.

One suggestion for design and arrangement of attached board is shown in Figure 18.

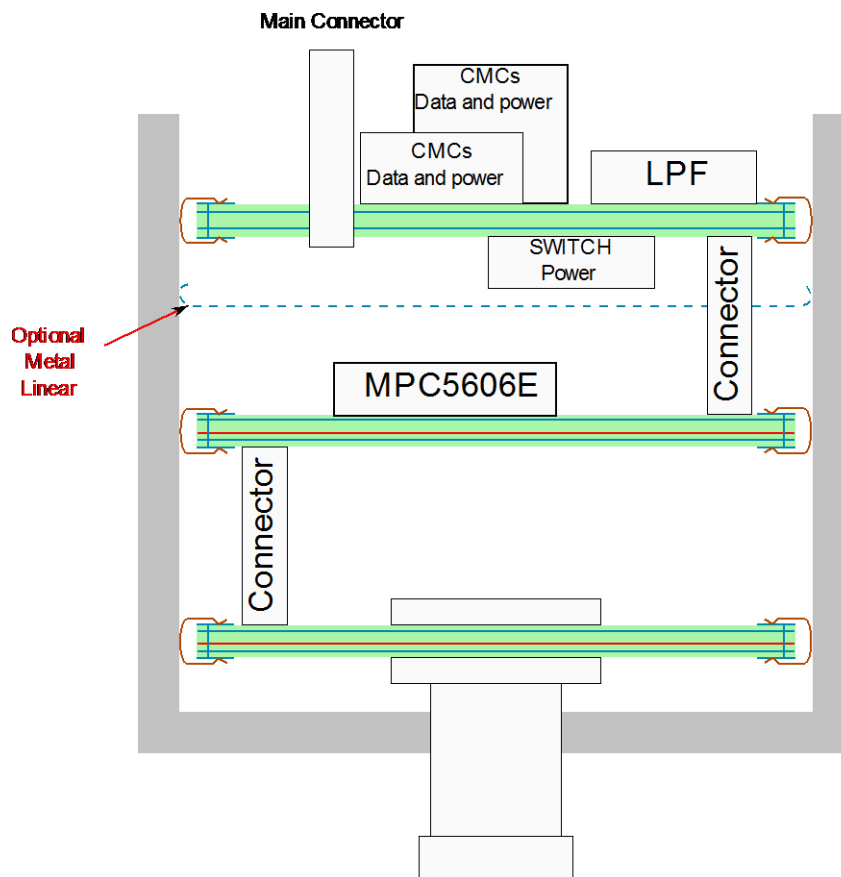


Figure 18. Reducing emission from stacked boards (Camera example)

Following is the list of recommendations for the camera example:

- Use continuous GND planes on all GND layers of all PCBs.
- Expose and plane GND traces around the board edges, top and bottom.
- Connect the exposed GND traces to GND planes with vias around PCB.
- Provide contacts between each PCB and the shield/enclosure. This forces $V_{CM} = 0\text{ V}$ at the locations of the contacts. There are various mechanical possibilities for doing this. Screws in four corners may not be enough for a quiet design
- Optional metal liner under the I/O board, connected to the enclosure around its perimeter can aid in protecting the I/O board from the noisy coupled from the other boards.
- If the camera is in a plastic enclosure, plan for a thin metal liner inside to provide function of the shield and contacts with the PCBs.

8. References

The following documents are available at freescale.com:

- *MPC5606ERM*: MPC5606E Microcontroller Reference Manual
- *MPC5606E*: MPC5606E Microcontroller Data Sheet

9. Technical Support

Freescale provides customer access to wide range information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information and software.

Freescale provides other product support via Downloads and Support site: freescale.com.

For further information on BroadR-Reach visit Broadcom docSAFE site.

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