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Application Note

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Mask Set Differences Between the MPC5606BF and MPC5606BK

The 32-bit Qorivva Microcontroller Family

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1 MPC5606BK overview

The MPC5606BK is a member of the Qorriva family of microcontrollers, built on Power Architecture® technology. It is suitable for use in automotive applications such as body, lighting, and gateway control. As two members of the same microcontroller family, the MPC5606BK and MPC5606BF are highly compatible; this document highlights the differences between the two devices and assists with the migration of applications previously designed for MPC5606BF. For further information on implementing the specific functions, refer to MPC5606BRM, *MPC5606B Microcontroller Reference Manual*.

The video at right demonstrates hardware and software compatibility for applications written for MPC560xBx that can be simply ported to MPC5606BK. It has been optimized for viewing in Adobe Acrobat® and may not display correctly in some web browsers.

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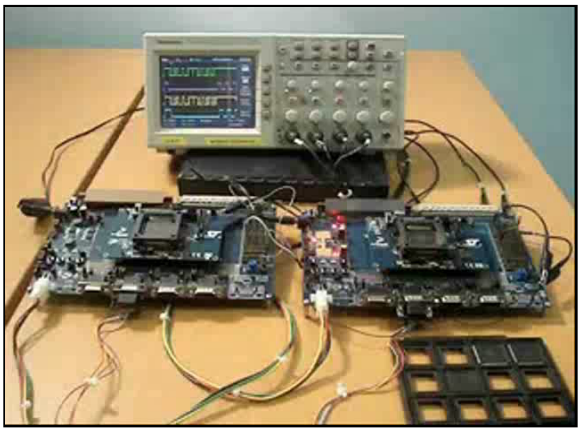

Table 1. Mask set identifier

Device	Mask set
xPC5606B**F**	1M03Y
xPC5606B**K**	01N3E

The majority of the modules used on both devices are the same technology, thus simplifying the transition from the MPC5606BF to the MPC5606BK. The rest of this document describes differences in further detail.

2 Memory map

Table 2 compares the memory maps of the MPC5606BK and the MPC5606BF, illustrating a high degree of compatibility between the flash memory, RAM, and register space. Where differences exist, this has been highlighted.

Note that applications that use code flash array 2 on the MPC560xBF and 16 KB of SRAM between 0x40014000–0x40017FFF will have to be altered because these resources are no longer supported. The memory space that is not used in the MPC5606BK has been marked as reserved. The SSCM_ERROR.PAE/RAE can be set to generate an exception if these reserved areas are accessed.

Table 2. Memory map for the MPC5606BK and MPC5606B

Start address	End address	Size (KB)	MPC5606BK	MPC5606BF
0x00000000	0x00007FFF	32	Code Flash Array 0	Code Flash Array 0
0x00008000	0x0000BFFF	16	Code Flash Array 0	Code Flash Array 0
0x0000C000	0x0000FFFF	16	Code Flash Array 0	Code Flash Array 0
0x00010000	0x00017FFF	32	Code Flash Array 0	Code Flash Array 0
0x00018000	0x0001FFFF	32	Code Flash Array 0	Code Flash Array 0
0x00020000	0x0003FFFF	128	Code Flash Array 0	Code Flash Array 0
0x00040000	0x0005FFFF	128	Code Flash Array 0	Code Flash Array 0
0x00060000	0x0007FFFF	128	Code Flash Array 0	Code Flash Array 0
0x00080000	0x0009FFFF	128	Code Flash Array 1	Code Flash Array 1
0x000A0000	0x000BFFFF	128	Code Flash Array 1	Code Flash Array 1
0x000C0000	0x000DFFFF	128	Code Flash Array 1	Code Flash Array 1
0x000E0000	0x000FFFFF	128	Code Flash Array 1	Code Flash Array 1
0x00100000	0x0011FFFF	128	Reserved	Reserved
0x00120000	0x0013FFFF	128	Reserved	Reserved
0x00140000	0x0015FFFF	128	Reserved	Reserved
0x00160000	0x0017FFFF	128	Reserved	Reserved
0x00180000	0x001FFFFF	512	Reserved	Reserved
0x00200000	0x00203FFF	16	Code Flash Array 0 Shadow Sector	Code Flash Array 0 Shadow Sector

Table 2. Memory map for the MPC5606BK and MPC5606B (continued)

Start address	End address	Size (KB)	MPC5606BK	MPC5606BF
0x00204000	0x003FFFFF	2032	Reserved	Reserved
0x00400000	0x00403FFF	16	Code Flash Array 0 Test Sector	Code Flash Array 0 Test Sector
0x00404000	0x007FFFFF	4080	Reserved (Code Flash Array 1 & 2 Test Sectors removed)	Reserved
0x00800000	0x00803FFF	16	Data Flash Array 0	Data Flash Array 0
0x00804000	0x00807FFF	16	Data Flash Array 0	Data Flash Array 0
0x00808000	0x0080BFFF	16	Data Flash Array 0	Data Flash Array 0
0x0080C000	0x0080FFFF	16	Data Flash Array 0	Data Flash Array 0
0x00810000	0x00BFFFFF	4032	Reserved	Reserved
0x00C00000	0x00C03FFF	16	Test Sector Data Flash Array 0	Test Sector Data Flash Array 0
0x00C04000	0x00FFFFFF	4080	Reserved	Reserved
0x01000000	0x1FFFFFFF	507904	Flash Emulation Mapping	Flash Emulation Mapping
0x20000000	0x3FFFFFFF	524288	Reserved for External Bus Interface	Reserved for External Bus Interface
0x40000000	0x40013FFF	80	SRAM	SRAM
0x40014000	0x7FFFFFFF	1048495	Reserved	Reserved
0x80000000	0xBFFFFFFF	1048576	Reserved	Reserved
Off-Platform Peripherals (PBRIDGE0)				
0xC0000000	0xC3F7FFFF	65024	Reserved	Reserved
0xC3F80000	0xC3F83FFF	16	Reserved	Reserved
0xC3F84000	0xC3F87FFF	16	Reserved	Reserved
0xC3F88000	0xC3F8BFFF	16	Code Flash 0 Configuration	Code Flash 0 Configuration
0xC3F8C00	0xC3F8FFFF	16	Data Flash 0 Configuration	Data Flash 0 Configuration
0xC3F90000	0xC3F93FFF	16	System Integration Unit Lite (SIUL)	System Integration Unit Lite (SIUL)
0xC3F94000	0xC3F97FFF	16	Wakeup Unit	Wakeup Unit
0xC3F98000	0xC3F9FFFF	32	Reserved	Reserved
0xC3FA0000	0xC3FA3FFF	16	eMIOS 0	eMIOS 0
0xC3FA4000	0xC3FA7FFF	16	eMIOS 1	eMIOS 1
0xC3FA8000	0xC3FAFFFF	32	Reserved	Reserved
0xC3FB0000	0xC3FB3FFF	16	Reserved	Reserved
0xC3FB4000	0xC3FB7FFF	16	Reserved	Reserved
0xC3FB8000	0xC3FD7FFF	128	Reserved	Reserved
0xC3FD8000	0xC3FDBFFF	16	System Status and Configuration Module (SSCM)	System Status and Configuration Module (SSCM)
0xC3FDC000	0xC3FDFFFF	16	Mode Entry Module (MC_ME)	Mode Entry Module (MC_ME)

Table 2. Memory map for the MPC5606BK and MPC5606B (continued)

Start address	End address	Size (KB)	MPC5606BK	MPC5606BF
0xC3FE0000	0xC3FE3FFF	16	Clock Generation Module (MC_CGM)[1]	Clock Generation Module (MC_CGM)
0xC3FE4000	0xC3FE7FFF	16	Reset Generation Module (MC_RGM)	Reset Generation Module (MC_RGM)
0xC3FE8000	0xC3FEBFFF	16	Power Control Unit (MC_PCU)	Power Control Unit (MC_PCU)
0xC3FEC000	0xC3FEFFFF	16	Real Time Counter (RTC/API)	Real Time Counter (RTC/API)
0xC3FF0000	0xC3FF3FFF	16	Periodic Interrupt Timer (PIT/RTI)	Periodic Interrupt Timer (PIT/RTI)
0xC3FF4000	0xC3FFFFFF	48	Reserved	Reserved
0xC4000000	0xDFFFFFFF	458752	Reserved	Reserved
0xE0000000	0xFFDFFFFF	522240	Reserved	Reserved
0xFFE00000	0xFFE03FFF	16	ADC0	ADC0
0xFFE04000	0xFFE07FFF	16	ADC1	ADC1
0xFFE0C000	0xFFE2FFFF	176	Reserved	Reserved
0xFFE30000	0xFFE33FFF	16	I2C 0	I2C 0
0xFFE34000	0xFFE3FFFF	48	Reserved	Reserved
0xFFE40000	0xFFE43FFF	16	LINFlex 0	LINFlex 0
0xFFE44000	0xFFE47FFF	16	LINFlex 1	LINFlex 1
0xFFE48000	0xFFE4BFFF	16	LINFlex 2	LINFlex 2
0xFFE4C000	0xFFE4FFFF	16	LINFlex 3	LINFlex 3
0xFFE50000	0xFFE53FFF	16	LINFlex 4	LINFlex 4
0xFFE54000	0xFFE57FFF	16	LINflex 5	LINflex 5
0xFFE58000	0xFFE5BFFF	16	LINFlex 6	LINFlex 6
0xFFE5C000	0xFFE5FFFF	16	LINFlex 7	LINFlex 7
0xFFE64000	0xFFE67FFF	16	CTU-LITE	CTU-LITE
0xFFE68000	0xFFE6FFFF	32	Reserved	Reserved
0xFFE70000	0xFFE73FFF	16	CAN sampler	CAN sampler
0xFFE74000	0xFFE7FFFF	48	Reserved	Reserved
0xFFE80000	0xFFEFFFFF	512	Mirrored Range 0x3F80000–0xC3FFFFFF	Mirrored Range 0x3F80000–0xC3FFFFFF
0xFFF00000	0xFFF03FFF	16	Reserved	Reserved
0xFFF04000	0xFFF07FFF	16	Reserved	Reserved
0xFFF08000	0xFFF0FFFF	32	Reserved	Reserved
0xFFF10000	0xFFF13FFF	16	MPU	MPU
0xFFF14000	0xFFF37FFF	144	Reserved	Reserved
0xFFF38000	0xFFF3BFFF	16	SWT	SWT
0xFFF3C000	0xFFF3FFFF	16	STM	STM

Table 2. Memory map for the MPC5606BK and MPC5606B (continued)

Start address	End address	Size (KB)	MPC5606BK	MPC5606BF
0xFFF40000	0xFFF43FFF	16	ECSM	ECSM
0xFFF44000	0xFFF47FFF	16	eDMA	eDMA
0xFFF4C000	0xFFF4BFFF	16	INTC	INTC
0xFFF90000	0xFFF8FFFF	272	Reserved	Reserved
0xFFF94000	0xFFF93FFF	16	DSPI 0	DSPI 0
0xFFF98000	0xFFF97FFF	16	DSPI 1	DSPI 1
0xFFF9C000	0xFFF9BFFF	16	DSPI 2	DSPI 2
0xFFFA0000	0xFFF9FFFF	16	DSPI 3	DSPI 3
0xFFFA4000	0xFFFA3FFF	16	DSPI 4	DSPI 4
0xFFFA8000	0xFFFA7FFF	16	DSPI 5	DSPI 5
0xFFFB0000	0xFFFAFFFF	32	Reserved	Reserved
0xFFFB4000	0xFFFB3FFF	16	Reserved	Reserved
0xFFFB8000	0xFFFB7FFF	16	Reserved	Reserved
0xFFFC0000	0xFFFBFFFF	32	Reserved	Reserved
0xFFFC4000	0xFFFC3FFF	16	FlexCan 0 (CAN0)	FlexCan 0 (CAN0)
0xFFFC8000	0xFFFC7FFF	16	FlexCan 1 (CAN1)	FlexCan 1 (CAN1)
0xFFFCC000	0xFFFCBFFF	16	FlexCan 2 (CAN2)	FlexCan 2 (CAN2)
0xFFFD0000	0xFFFCFFFF	16	FlexCan 3 (CAN3)	FlexCan 3 (CAN3)
0xFFFD4000	0xFFFD3FFF	16	FlexCan 4 (CAN4)	FlexCan 4 (CAN4)
0xFFFD8000	0xFFFD7FFF	16	FlexCan 5 (CAN5)	FlexCan 5 (CAN5)
0xFFFD8000	0xFFFDBFFF	16	Reserved	Reserved
0xFFFDC000	0xFFFDFFFF	16	DMA Ch Multiplexer	DMA Ch Multiplexer
0xFFFE0000	0xFFFFBFFF	16	Reserved	Reserved
0xFFFFC000	0xFFFFFFFF	16	BAM	BAM

[1] An additional register, CGM_AC0_SC (Auxiliary clock select control) has been added at address 0xC3FE_0380 on the MPC5606BK.

3 Pins and packages

Table 3. Available packages

Package	MPC5606BK	MPC5606BF
100 LQFP	Yes	Yes
144 LQFP	Yes	Yes
176 LQFP	Yes	Yes

The MPC5606BK is available in the same packages as the MPC5606BF and is pin compatible; therefore, it is capable of being used on hardware designed for the MPC5606BF device (same pin package).

These devices do not have a 208 BGA package. The MPC5607B, on the other hand, contains 8 pins dedicated for Nexus 2+ functions that are not present on the MPC5606BK or MPC5606BF devices: MCKO, MDO0, MDO1, MDO2, MDO3, EVTI, EVTO, MSEO. In addition, the associated Nexus power and ground pins are not available. (See Section 4.4, “Debug” for further information.)

4 Peripheral differences

The MPC5606BK has been created to be identical to the MPC5606BF and the modules use the same technology with subtle differences.

4.1 Flash memory

The code flash memory on the MPC5606BK consists of a single 1 MB array similar to the MPC5606BF. Both devices access these arrays through a single port (p0) on the P-flash controller. The flash memory array is accessed identically: doubleword write and page read.

The addressing is identical between the two devices. The following table compares the memory addressing:

Table 4. Code flash (C-flash) memory

	Address	Size	MPC56056K 768K	MPC5606BK 1M	MPC56056F 768K	MPC5606BF 1M
LAS	0x00000000–0x00007FFF	32K	B0F0	B0F0	B0F0	B0F0
	0x00008000–0x0000BFFF	16K	B0F1	B0F1	B0F1	B0F1
	0x0000C000–0x0000FFFF	16K	B0F2	B0F2	B0F2	B0F2
	0x00010000–0x00017FFF	32K	B0F3	B0F3	B0F3	B0F3
	0x00018000–0x0001FFFF	32K	B0F4	B0F4	B0F4	B0F4
	0x00020000–0x0003FFFF	128K	B0F5	B0F5	B0F5	B0F5
MAS	0x00040000–0x0005FFFF	128K	B0F6	B0F6	B0F6	B0F6
	0x00060000–0x0007FFFF	128K	B0F7	B0F7	B0F7	B0F7

Table 4. Code flash (C-flash) memory (continued)

	Address	Size	MPC56056K 768K	MPC5606BK 1M	MPC56056F 768K	MPC5606BF 1M
HAS	0x00080000–0x0009FFFF	128K	B0F8	B0F8	B0F8	B0F8
	0x000A0000–0x000BFFFF	128K	B0F9	B0F9	B0F9	B0F9
	0x000C0000–0x000DFFFF	128K	—	B0FA	—	B0FA
	0x000E0000–0x000FFFFF	128K	—	B0FB	—	B0FB
	0x00100000–0x0011FFFF	128K	—	—	—	—
	0x00120000–0x0013FFFF	128K	—	—	—	—
	0x00140000–0x0015FFFF	128K	—	—	—	—
	0x00160000–0x0017FFFF	128K	—	—	—	—
	0x00180000–0x001FFFFF	512K	Reserved			
	0x00200000–0x00203FFF	16K	Shadow Sector			
	0x00204000–0x003FFFFF	2032	Reserved			
	0x00400000–0x00403FFF	16K	Test			
	0x00404000–0x007FFFFF	4080	Test			

Table 4 highlights the flash sectors and their associated addresses. The stated flash block sizes and alignments have been maintained between MPC5606BK and MPC5606BF, creating compatibility.

The registers required to program and modify the flash memory remain compatible but some of these configuration register have different reset values.

Table 5. C-flash default register values

Register Value/Scenario	MPC5606BK	MPC5606BF	Comments
MCR Reset Value	3200600	4200600	This is due to the 'Size' nibble within C-flash MCR differing
ADR Reset Value	0000C000	0	This is the initial value, but would be updated with any an initial ECC error address in the rare case this occurred.
On writing the password (B2B22222) second time on HBL (that is, after writing once as password), the value of HBL becomes	80000FF2	80000F22	Since there are 8 sectors in the High Address space of MPC5606BF, but only 4 in MPC5606BK.

The 64 KB of D-flash memory is identical between the MPC5606BK and the MPC5606BF.

Table 6. Data flash (D-flash) memory

	Address	Size	MPC5605BK 768K	MPC5606BK 1M	MPC5606BF 768K	MPC5606BF 1M
LAS	0x00800000–0x00803FFF	16K	B0F0	B0F0	B0F0	B0F0
	0x00804000–0x00807FFF	16K	B0F1	B0F1	B0F1	B0F1
	0x00808000–0x0080BFFF	16K	B0F2	B0F2	B0F2	B0F2
	0x0080C000–0x0080FFFF	16K	B0F3	B0F3	B0F3	B0F3
	0x00810000–0x00BFFFFF	4032	RESERVED			
	0x00C00000–0x00C03FFF	16K	TEST			

4.2 SRAM

The MPC5606BF and the MPC5606BK both have 80 KB of internal SRAM. There are no differences between the addressing or functionality. On MPC5606BK, there are no wait states for RAM access at 64 MHz system frequency.

4.3 Clocking structure

The MPC5606BK has an additional feature that makes it possible to use the PLL with a 16 MHz IRC source. On the MPC5606BF, the PLL can only be used with FXOSC as the source. For both devices, FXOSC remains the default clock source, so user software will have to activate this new feature on the MPC5606BK by setting auxiliary clock register bit CGM_AC0_SC.SELCTL and any other appropriate mode entry transition that is required.

It should be noted that this register is not present on the MPC5606BF. On the MPC5606BK, it is found at address 0xC3FE_0380 in the MC_CGM module's memory map. This address is reserved on the MPC5606BF.

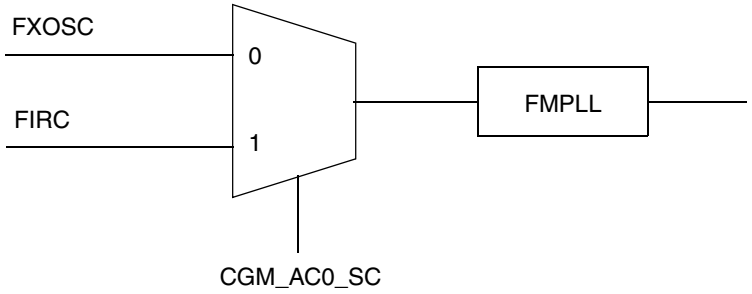

Figure 1. FMPLL clock source select via Auxiliary Clock Select 0

The following points should be followed when utilising the PLL for MPC5606BK and MPC560xBF devices

1. Ensure PLL is disabled
2. Program ODF/IDF/NDIV
3. Ensure PLL selected as system clock source at mode entry mode configuration register
4. Enable PLL at mode entry mode configuration register (e.g. ME.DRUN_MC.R)

If the PLL frequency is required to be altered, ensure the PLL is turned off at mode entry configuration register, configure PLL settings (ODF/IDF/NDIV) and re-enable PLL. Moreover, It is possible to adjust ODF whilst PLL locked, but IDF and NDIV cannot be adjusted.

4.4 Debug

Neither the MPC5606BF nor the MPC5606BK contain the Nexus port controller module; hence, they do not have Nexus 2+ capability. Debugging is available through JTAG OnCE, which is compatible with MPC5606BF. In the event that Nexus debug capability is required, the 208 BGA MPC5607B device could be used, which again has identical peripheral features and memory map (excluding the additional 512K C-flash memory it has) to both the MPC5606BF and MPC5606BK devices.

The JTAG ID is outlined within the SIU.MIDR register. In order to differentiate between devices, IDs differ. Any application that reads this register will have to be amended to take account of the different register state.

Table 7. JTAG IDs

Device	JTAG ID
MPC5606BK	0x06A4401D
MPC5606BF	0x2AE4301D

4.5 System Integration Unit Lite

This module only differs with the read only data contained within the MIDR registers for MPC5606BK. The MIDR1, MIDR_PARTNUM[31:16] has been updated to 0x5606 and MIDR2 is updated to reflect the flash memory size and part number, whether a body or gateway controller.

4.6 Device errata

NOTE

This section is written for guidance in understanding errata that are present on the MPC5606BF, but that do not apply to the MPC5606BK. At the time of publication, the information included here is accurate and up-to-date. It is *strongly recommended* that you consult the most up-to-date errata lists and reference manual for the most current information.

As a new addition to the Qorivva family, the MPC5606BK has fewer device errata than the MPC5606BF; this should be examined for migrating applications. The following table shows errata not present on MPC5606BK but present on MPC5606BF.

Table 8. Errata present on MPC5606BF but not on MPC5606BK

Errata Reference		Errata Title
ID before July 2010	ID After July 2010	
e8099	e3195	Limitations for DMA access to LINFlex
e3492	e2977	MC_RGM: Long Reset Sequence Occurs on “Short Functional” Reset Event
e8499	e3209	NMI pin configuration limitation in standby mode
e5095	e3049	MC_RGM: External Reset not asserted if Short Reset enabled
e6440	e3119	SWT: SWT interrupt does not cause STOP0 mode exit
e8761	e3219	MC_CGM: System clock may stop for case when target clock source stops during clock switching transition
e4781	e3021	LINFlex: Unexpected LIN timeout in slave mode
e1685	e2883	FMPLL: FMPLL_CR[UNLOCK_ONCE] wrongly set
—	e3449	DEBUG: Device may hang due to external or “functional” reset while using debug handshaking mechanism
—	e3606	32 kHz SXOSC stops oscillating during STANDBY mode exit
—	e6726	NPC: MCKO clock may be gated one clock period prior to Nexus state machine entering IDLE state when MCKO frequency is programmed as SYS_CLK/8

Table 8. Errata present on MPC5606BF but not on MPC5606BK (continued)

Errata Reference		Errata Title
ID before July 2010	ID After July 2010	
—	e3466	LINFlexD: Register bus aborts are not generated on illegal accesses to reserved addresses within the register address space of LINFlexD
—	e3574	MC_RGM: A nonmonotonic ramp on the VDD_HV/BV supply can cause the RGM module to clear all flags in the DES register
—	e3210	PA[1] pull-up enabled when NMI activated
—	e3242	PB[10],PD[0:1] pins configuration during standby

For applications developed on the MPC5606BF, it may be likely that workarounds constructed for the above errata have been implemented. These workarounds should have no impact upon the operation of the same application software, at the device level, on the MPC5606BK, where the errata do not exist.

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