

Migrating from MPC5607B cut1 to cut2

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1 Introduction

The 32-bit MPC560xB/C automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controllers, smart junction box, front module, peripheral body, door control, and seat control applications.

The MPC560xB/C is a series of automotive microcontrollers based on the Power Architecture® Book E and designed specifically for embedded automotive applications.

The MPC560xB/C is a highly scalable and compatible family of devices. However, designing an application that can easily be ported across different members requires knowledge of the device features and any significant differences between them.

This document focuses specifically on migrating MPC5607B applications from cut1 to cut 2.

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2 List of Differences Between MPC5607B cut1 and cut2

The *MPC5607B Microcontroller Reference Manual*, Rev.2 (document MPC5607BRM) refers to cut1 silicon. The *MPC5607B Microcontroller Reference Manual*, Rev.3 and later revisions reflects cut2 silicon implementation. The sections hereafter describe differences in detail.

2.1 Eight Additional ADC 12-bit Medium Accuracy Channels

There are eight additional ADC 12-bit medium accuracy channels on cut2. They are mapped as follows:

- ADC1_S[0] on PA[3]
- ADC1_S[1] on PA[7]
- ADC1_S[2] on PA[10]
- ADC1_S[3] on PA[11]
- ADC1_S[4] on PB[8]
- ADC1_S[5] on PB[9]
- ADC1_S[6] on PB[10]
- ADC1_S[7] on PE[12]

ADC1_S[4], ADC1_S[5], and ADC1_S[6] are shared with three ADC 10-bit medium accuracy channels.

Refer to [Figure 1](#) to see the additional ADC 12-bit channels in red.

NOTE

On earlier versions of the *MPC5607B Microcontroller Reference Manual* and the *MPC5607B Microcontroller Data Sheet* (document MPC5607B) the ADC channel names were referred to as:

ANS[n],

ANP[n],

ANX[n],

Starting from Revision 5 these are now referred to as:

ADC0_S[n] and ADC1_S[n],

ADC0_P[n] and ADC1_P[n],

ADC0_X[n] and ADC1_X[n]

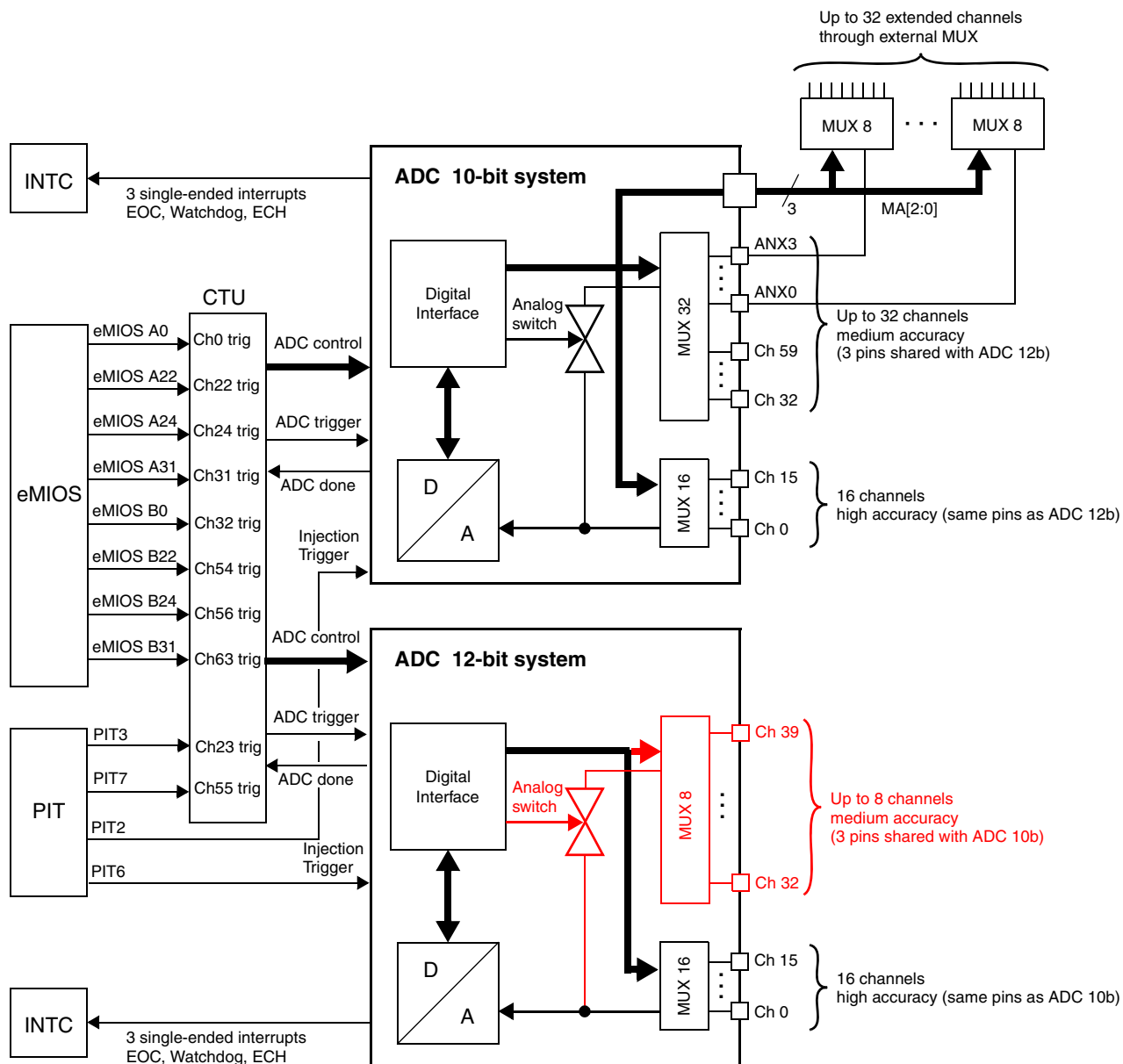


Figure 1. ADC Implementation of MPC5607B cut2

2.2 Four Additional Wakeup Lines

On cut2, four additional wakeup lines are mapped on PB8 / GPIO[24], PB9 / GPIO[25], PD0 / GPIO[48], and PD1 / GPIO[49], which are analog inputs. Refer to [Section 2.5, “Interrupt Vectors Mapping for Wakeup Lines”](#) for interrupt vector mapping.

2.3 LINFlex 0 and LINFlex 1 Support DMA

On cut1, none of the 10 LINFlex peripherals support DMA. On cut2, DMA is connected on LINFlex 0 and LINFlex 1.

2.3.1 DMA_MUX Mapping Change

Table 1. DMA_MUX in cut1 and cut2 comparison

DMA_MUX channel	cut1		cut2
	Module	DMA requesting module	Module
0	—	Always disabled	—
1	DSPI 0	DSPI_0 TX	DSPI 0
2	DSPI 0	DSPI_0 RX	DSPI 0
3	DSPI 1	DSPI_1 TX	DSPI 1
4	DSPI 1	DSPI_1 RX	DSPI 1
5	DSPI 2	DSPI_2 TX	DSPI 2
6	DSPI 2	DSPI_2 RX	DSPI 2
7	DSPI 3	DSPI_3 TX	DSPI 3
8	DSPI 3	DSPI_3 RX	DSPI 3
9	DSPI 4	DSPI_4 TX	DSPI 4
10	DSPI 4	DSPI_4 RX	DSPI 4
11	DSPI 5	DSPI_5 TX	DSPI 5
12	DSPI 5	DSPI_5 RX	DSPI 5
13	eMIOS 0	EMIOS0_CH0	—
14	eMIOS 0	EMIOS0_CH1	—
15	eMIOS 0	EMIOS0_CH9	—
16	eMIOS 0	EMIOS0_CH18	—
17	eMIOS 0	EMIOS0_CH25	eMIOS 0
18	eMIOS 0	EMIOS0_CH26	eMIOS 0
19	eMIOS 1	EMIOS1_CH0	eMIOS 0
20	eMIOS 1	EMIOS1_CH9	eMIOS 0
21	eMIOS 1	EMIOS1_CH17	eMIOS 0
22	eMIOS 1	EMIOS1_CH18	eMIOS 0
23	eMIOS 1	EMIOS1_CH25	eMIOS 1
24	eMIOS 1	EMIOS1_CH26	eMIOS 1
25	ADC 0	ADC0_EOC	eMIOS 1
26	ADC 1	ADC1_EOC	eMIOS 1
27	I ² C	IIC_RX	eMIOS 1
28	I ² C	IIC_TX	eMIOS 1
29	—	Always enabled	ADC 0
30	—	Always enabled	ADC 1
31	—	Always enabled	I ² C

Table 1. DMA_MUX in cut1 and cut2 comparison (continued)

	cut1		cut2
32	—	Always enabled	I ² C
33	—	Reserved	LINFLEX 0
34	—	Reserved	LINFLEX 0
35	—	Reserved	LINFLEX 1
36	—	Reserved	LINFLEX 1
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
51			
52			
53			
54			
55			
56			
57			
58			
59			
60	—	Reserved	—
61	—	Reserved	—
62	—	Reserved	—
63	—	Reserved	—

2.3.2 LINFlex 0 LINFlex 1 Change

LINFlex 0 and LINFlex 1 have the following additional features on cut2

- DMA
- FIFO in UART

Please refer to the LINFLexD chapter in the *MPC5607B Microcontroller Reference Manual, Rev.5*

2.4 Pin Multiplexing data

2.4.1 DSPI Chip Selects

On cut2, DSPI 1 chip selects are also available on the following ports on alternate function AF3:

- CS0_1 on PA[4]
- CS1_1 on PA[6]
- CS2_1 on PA[9]
- CS3_1 on PA[12]
- CS4_1 on PA[3]

2.4.2 LINFlex 0 and LINFlexCan 0 Functionality Multiplexed Onto the Same Pins

In order to support it, cut2 has:

- LIN0TX on PB[0], on alternate function AF3,
- LIN0RX on PB[1]

2.4.3 ADC 10-bit external multiplexing

ADC external multiplexer control MA[2] is multiplexed onto the alternate function AF3 of pad PA[2].

2.5 Interrupt Vectors Mapping for Wakeup Lines

Four wakeup lines have been added in cut2 on:

PB8 / GPIO[24], PB9 / GPIO[25], PD0 / GPIO[48], and PD1 / GPIO[49] (refer to [Section 2.2, “4 Additional Wakeup Lines](#)). They are mapped on WakeUp_IRQ_3.

Wakeup lines on GPIO[103], GPIO[105], GPIO[89], and GPIO[131] previously mapped on WakeUp_IRQ_3 on cut1 are mapped on WakeUp_IRQ_2 on cut2. Refer to [Table 2](#) for details.

Table 2. Wakeup lines interrupt vector mapping

Interrupt Vector	cut1	cut2	Comment
WakeUp_IRQ_0	API	API	Unchanged
	RTC	RTC	Unchanged
	GPIO[1]	GPIO[1]	Unchanged
	GPIO[2]	GPIO[2]	Unchanged
	GPIO[17]	GPIO[17]	Unchanged
	GPIO[43]	GPIO[43]	Unchanged
	GPIO[64]	GPIO[64]	Unchanged
	GPIO[73]	GPIO[73]	Unchanged
WakeUp_IRQ_1	GPIO[26]	GPIO[26]	Unchanged
	GPIO[4]	GPIO[4]	Unchanged
	GPIO[15]	GPIO[15]	Unchanged
	GPIO[19]	GPIO[19]	Unchanged
	GPIO[39]	GPIO[39]	Unchanged
	GPIO[41]	GPIO[41]	Unchanged
	GPIO[75]	GPIO[75]	Unchanged
	GPIO[91]	GPIO[91]	Unchanged
WakeUp_IRQ_2	GPIO[93]	GPIO[93]	Unchanged
	GPIO[99]	GPIO[99]	Unchanged
	GPIO[101]	GPIO[101]	Unchanged
	GPIO[0]	GPIO[0]	Unchanged
	Reserved	GPIO[103]	New
	Reserved	GPIO[105]	New
	Reserved	GPIO[89]	New
	Reserved	GPIO[131]	New
WakeUp_IRQ_3	GPIO[103]	GPIO[129]	Different
	GPIO[105]	GPIO[24]	Different
	GPIO[89]	GPIO[25]	Different
	GPIO[131]	GPIO[48]	Different
	GPIO[129]	GPIO[49]	Different
	Reserved	Reserved	Unchanged
	Reserved	Reserved	Unchanged
	Reserved	Reserved	Unchanged

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