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Application Note

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MPC5500 Multi-module Demo: Frequency Detection

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This application note describes how external frequencies can be detected and converted via analog inputs, by interfacing modules available on MPC5500 devices. The demo comprises two MPC5500EVB evaluation boards, and uses the following modules: QADC, eMIOS, DSPI, RAM, FLASH, INTC, eSCI, eDMA, FlexCAN, Core.

All software for the demo is available as a software package AN3524SW, which can be downloaded from www.freescale.com.

Contents

1 Design Aim

This multi-module demo was developed originally for the MPC5561, to replicate a typical application that may be run on MPC5500 family devices. Its purpose is to provide an example that illustrates the inter-operability of these modules.

The application on which the demo is based is that of frequency conversion and data transfer, a typical use for MPC5500 family devices. The demo illustrates how to interface many modules on the MPC5500 to perform a common task. The modules that are used are shown in Table 1.

Table 1. Modules Used in the Multi-module Demo

eQADC
eMIOS
DSPI
Internal RAM
Internal FLASH
INTC (Software Vector Mode)
eSCI
eDMA
Core (including SPE FFT)
FlexCAN

The integration of these modules is shown at a high level in Figure 1. This is described in more detail with the help of flow charts in the next section.

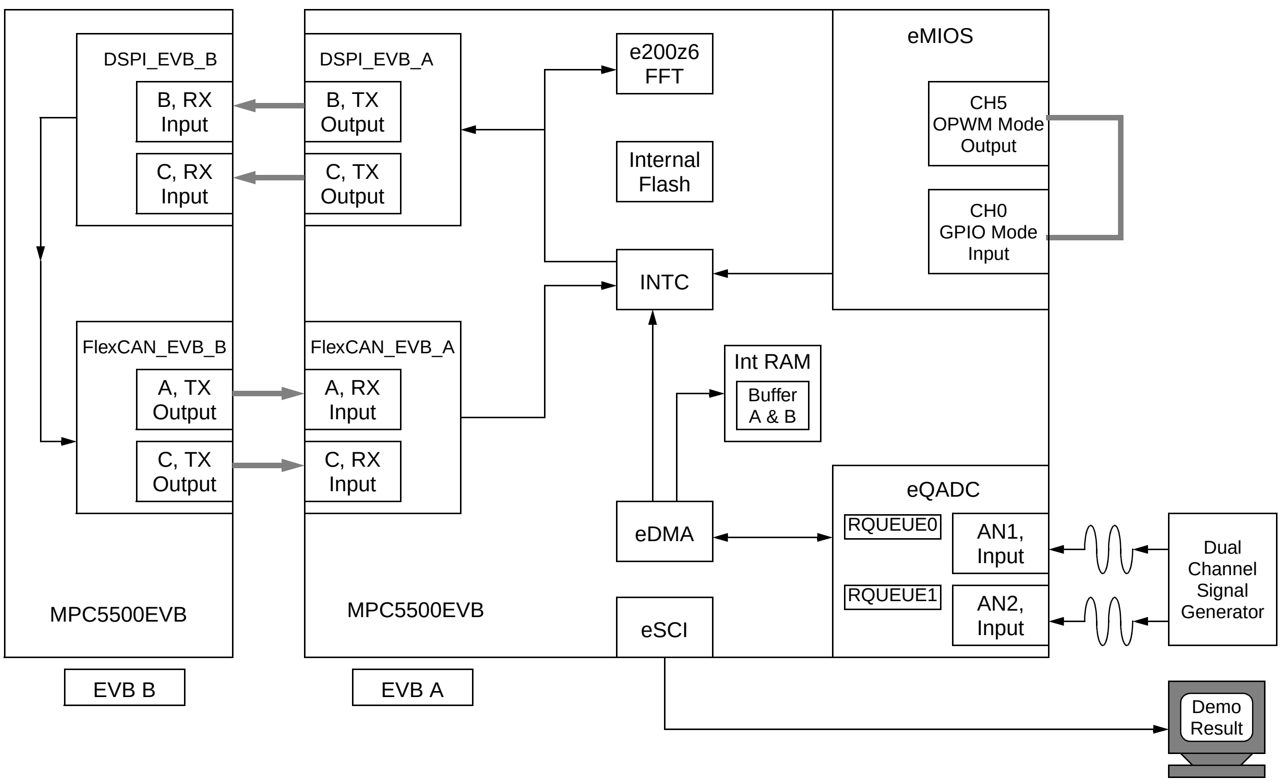

Figure 1. Interconnection of Modules in MPC5500 Multi-module Demo

2 Description of Demo

The multi-module example has been designed to represent an external frequency convertor and data transfer process. The process flow of the multi-module example is as follows.

1. Input two sine waves into two analog channels on EVB A — AN0 and AN1.
2. Capture a window of data using the two eQADC channels when an eMIOS trigger interrupt is received (external connection).
3. Transfer the eQADC converted data to RAM buffers via the eDMA.
4. Perform an FFT algorithm on the data in RAM using the SPE and determine the frequency from the results of the FFT.
5. Transmit the determined frequency from EVB A to EVB B via the DSPI modules.
6. On EVB B, send the received DSPI data back to EVB A via the CAN modules.
7. On EVB A, transmit the received data from the CAN (that is, the determined frequency) to a PC via the eSCI module.

See Section 3, “Software Functions” for further details.

2.1 High Level Flow Chart

The flow charts in Figure 2 and Figure 3 show how the software flows through the core, eDMA and interrupts for both EVBs.

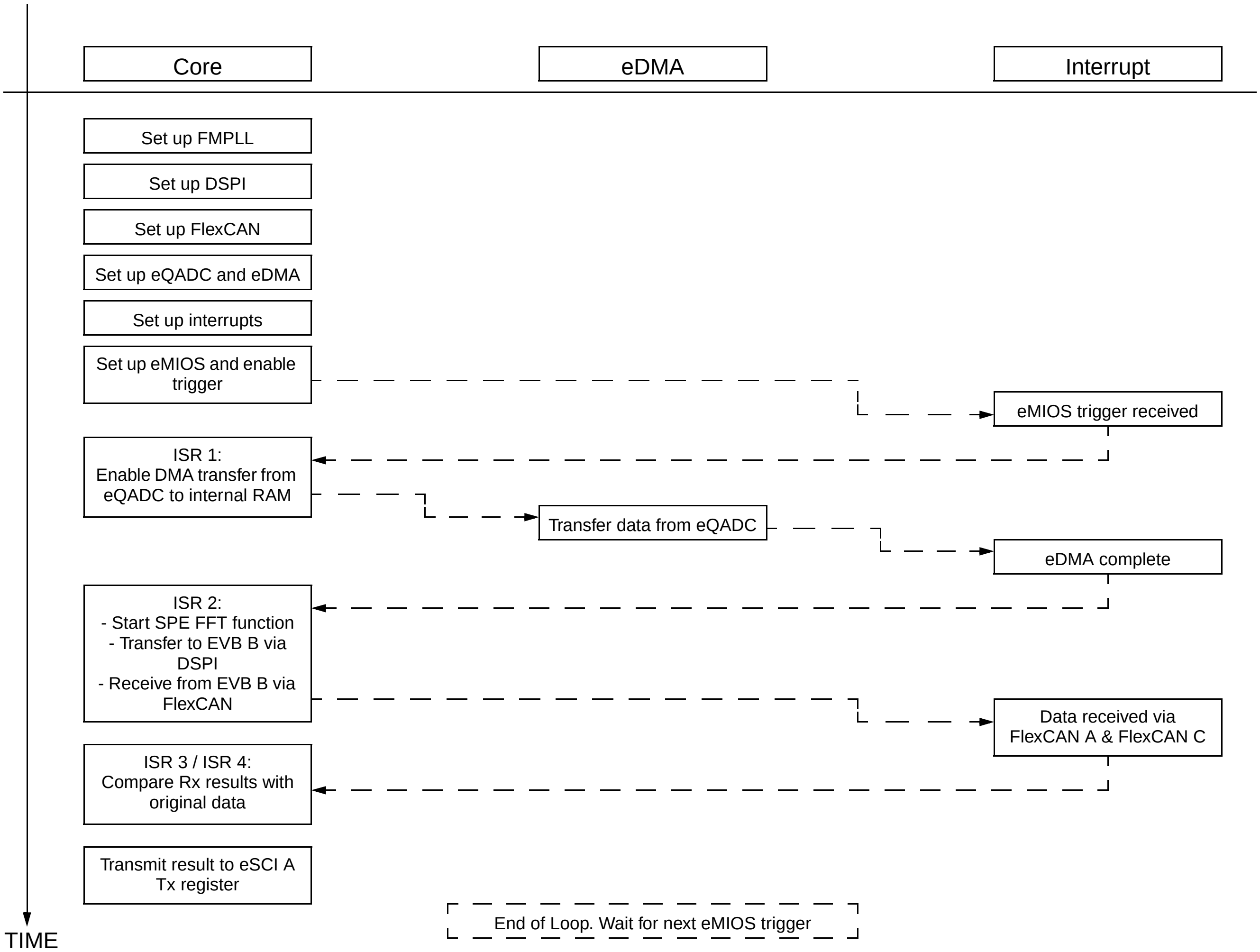

Figure 2. High Level Flow Chart of Multi-module Demo (EVB A)

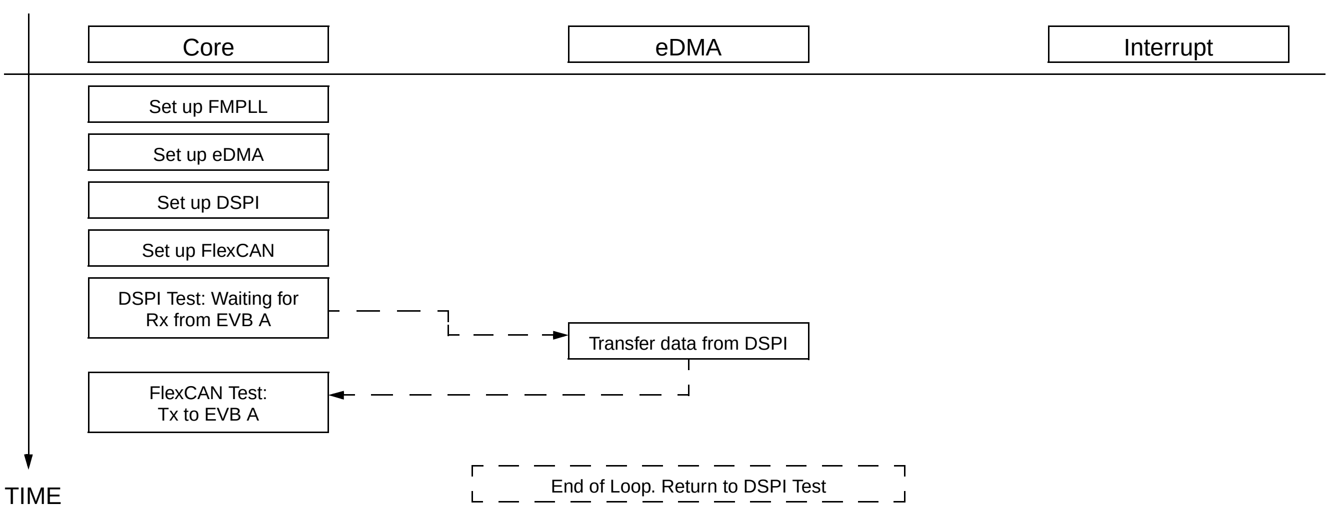

Figure 3. High Level Flow Chart of Multi-module Demo (EVB B)

3 Software Functions

In this section, the software flow shown in Figure 2 and Figure 3 is broken down into separate sections and described in more detail.

3.1 Setup Functions

The setup functions are called only at startup. Configuration of the eDMA, eQADC, DSPI, eMIOS, eSCI, FlexCAN modules and interrupts is described in the following sections.

3.1.1 Set Up FMPLL

The FMPLL is configured to operate at 128 MHz, derived from a 40 MHz crystal source.

3.1.2 Set Up DSPI (EVB A and EVB B)

The DSPI is set up with DSPI modules B and C as masters on EVB A and slaves on EVB B.

External connections between DSPI B and DSPI C on both EVBs must be made for the transmission to be successful. The corresponding PCR registers in the SIU are configured for DSPI functionality.

3.1.3 Set Up FlexCAN (EVB A and EVB B)

FlexCAN modules A and C are set up as follows on both EVBs.

EVB A sends eight words of trigger data (0x0102030405060780) on both FlexCAN modules.

EVB B waits to receive this data, then sends back the frequency variables highest_freq and highest_freq1 in the first four words of data.

EVB A compares this data with the original highest_freq and highest_freq1 variables, then outputs the results via the eSCI to the PC.

3.1.4 Set Up eQADC

Analog channels 1 and 2 (AN1 and AN2) are used to input sine waves from a signal generator. These two eQADC channels are set up to trigger each time a positive edge is detected in eMIOS CH0 (channel 0), via the eDMA.

There are 1024 conversions for each channel, and the results for AN1 and AN2 are stored in RQUEUE0 and RQUEUE1, respectively.

3.1.5 Set Up eDMA

Table 2 describes the configuration of the eDMA channels.

Table 2. eDMA Channel Configuration

TCD Channel	Function	Trigger	IRQ Vector	EVB
0/1	Transfer of CQUEUE0/RQUEUE0 to/from eQADC Push / Pop registers	Software	—	1
2/3	Transfer of CQUEUE1/RQUEUE1 to/from eQADC Push / Pop registers	Software	14	1
12	Transfer of TXQUEUE to DSPI B Push Register	Software	—	1
14	Transfer of TXQUEUE1 to DSPI C Push Register	Software	—	1
13	Transfer from DSPI B Pop register to RXQUEUE	Software	—	2
15	Transfer from DSPI C Pop register to RXQUEUE1	Software	—	2

3.1.6 Interrupts

The interrupt handler is run in software vector mode. Table 3 provides information on the interrupt sources that are used in the demo.

Table 3. Interrupt Handler Configuration

IRQ Vector	Source	ISR Called	ISR Name	EVB
14	eDMA data transfer completed (RQUEUE0 and RQUEUE1)	ISR 2	edma_ch3_ISR	1
51	eMIOS CH0 rising edge detected	ISR 1	emios_ch0_ISR	1
156	Data received on FlexCAN A	ISR 3	cana_buf1_ISR	1
179	Data received via FlexCAN C	ISR 3	canc_buf3_ISR	1

3.1.7 eMIOS

The eMIOS module uses CH0 (channel 0) and CH5 (channel 5) for the multi-module demo.

CH0 is configured for GPIO (General Purpose I/O) mode. CH5 is configured for OPWM (output pulse width modulation) mode. The OPWM signal is driven from CH5 to trigger CH0.

An external connection between CH0 and CH5 must be made for this stage of the demo process to operate. The corresponding PCR registers in the SIU are configured for eMIOS functionality. The OPWM is driven from the eMIOS channel to sample the sine waves at a frequency that is twice the maximum frequency of the sine wave, to avoid aliasing.

3.1.8 eSCI

The eSCI module is configured to run at a baud rate of 115200 bits per second, eight data bits, no parity, and one stop bit. The corresponding PCR registers in the SIU are configured for eSCI functionality. The results are transmitted to a PC via a serial connector.

3.2 EVB A ISRs

3.2.1 ISR 1 — eMIOS CH0 Rising Edge Detected (emios_ch0_ISR)

This is the main trigger for the demo. When a rising edge is detected on eMIOS CH0 (from eMIOS CH5), this interrupt service routine clears the interrupt and sets the eDMA set enable request register (SERQR) for CH1 and CH3 in order to start transfer of data from the eQADC.

3.2.2 ISR 2 — eDMA Transfer from eQADC Complete (edma_ch3_ISR)

This interrupt occurs when the eDMA has finished transferring data from the eQADC. The eDMA priority is set to make sure that eDMA CH1 has completed before eDMA CH3.

This service routine performs the FFT SPE function on both eQADC conversions. The function "FFT_freq" calls the SPE FFT function and converts the results to a frequency. Where possible, SPE is used to improve performance. Then, "analyse_FFT" takes the FFT output and analyses it to determine the frequency. The magnitude of the real and imaginary parts are analysed for an accurate frequency.

The results are transmitted via the DSPI modules to set up the FlexCAN modules for sending and receiving data.

3.2.3 ISR 3 — Data received on FlexCAN A (cana_buf1_ISR)

This function checks that the data received is valid by comparing it with the original value sent via DSPI B (highest_freq).

The results are output to the PC via the eSCI:

"Test has failed -FlexCAN_A" OR "Frequency on AN1 : highest_freq"

3.2.4 ISR 4 — Data received on FlexCAN C (canc_buf3_ISR)

This function checks that the data received is valid by comparing it with the original value sent via DSPI C (highest_freq1).

The results are output to the PC via the eSCI:

"Test has failed -FlexCAN_C" OR "Frequency on AN2 : highest_freq1"

4 Additional Information

Evaluation boards used in the demo are the Freescale MPC5561EVB RevB.

Software for the demo was compiled using the Wind River® Diab™ Compiler Version 5.2.1.0.

The multi-module demo runs continuously unless an error is detected.

Results are output via the eSCI and can be viewed on a PC using HyperTerminal (connected to COM 1 on EVB A).

The input range for the sine waves for an accurate conversion is from 1-180 KHz.

The sine waves must be connected to AN1 and AN2 before the demo can run. Resetting both EVBs (EVB A and EVB B) will restart the demo.

4.1 HyperTerminal Setup

A serial cable must be connected between EVB A and a PC. HyperTerminal is used to view the output of the demo. The settings for HyperTerminal are:

Bits per second:	115200
Data bits:	8
Parity:	None
Stop bits:	1
Flow Control:	Hardware

4.2 On Screen Messages

The PC will display the following message if the test loop is successful.

“Frequency on AN1 : highest_freq”

“Frequency on AN2 : highest_freq1”

Where highest_freq and highest_freq1 are the FFT results.

Other error messages may be shown if the demo fails:

“Test has failed -FlexCAN_A.” or “Test has failed -FlexCAN_C.”

Output will halt if the FlexCAN modules are disconnected.

4.3 External Connections

To ensure that the demo operates correctly, certain external connections must be made between signals on the MPC5500EVBs.

4.3.1 EVB A

Connect eQADC AN1 and AN2 to the signal generator output channels.

Connect eMIOS CH0 to CH5.

Set CAN_SEL jumpers 1, 2, 5, 6 = ON.

Connect serial cable (COM1) to PC.

4.3.2 EVB B

Set CAN_SEL jumpers 1, 2, 5, 6 = ON.

Connect test LEDs GPIO203, GPIO204, GPIO206, GPIO207 to USER_LED port (optional).

4.3.3 EVB A to EVB B (External Connections to DSPI B and DSPI C)

DSPI B and DSPI C require external connections for the demo to function (see Table 4). Note that the ball locations are for the MPC5561 device (324PBGA).

Table 4. EVB A to EVB B External Connections (DSPI)

EVB A			EVB B		
Ball	**Name**	**Function**	**Ball**	**Name**	**Function**
J19	SOUTB	DSPI_B Data Output	H22	SINB	DSPI_B Data Input
H22	SINB	DSPI_B Data Input	J19	SOUTB	DSPI_B Data Output
K21	SCKB	DSPI_B Clock	K21	SCKB	DSPI_B Clock
J21	PCSB0	DSPI_B Peripheral Chip Select	J21	PCSB0	DSPI_B Peripheral Chip Select
K22	PCSB2	DSPI_C Data Output	J20	PCSB3	DSPI_C Data Input
J20	PCSB3	DSPI_C Data Input	K22	PCSB2	DSPI_C Data Output
K20	PCSB4	DSPI_C Clock	K20	PCSB4	DSPI_C Clock
L19	PCSB5	DSPI_C Peripheral Chip Select	L19	PCSB5	DSPI_C Peripheral Chip Select

4.3.4 EVB A to EVB B (External FlexCAN Connector)

FlexCAN A and FlexCAN C on EVB A must be connected to FlexCAN A and FlexCAN C on EVB B.

This can be done using a male-to-male serial cable to connect pins CNTXA to CNRXA and CNTXB to CNRXB.

4.4 Loading Code

The multi-module demo was developed to run from internal flash on both EVBs.

The file “master_node.elf” found in the ‘Multi-module Demo\EVB A\obj’ directory should be loaded to the MPC5500 EVB A.

The file “slave_node.elf” found in the ‘Multi-module Demo\EVB B\obj’ directory should be loaded to the MPC5500 EVB B.

EVBs should be reset after programming internal flash.

The PC displays the results when the code is running. No debugger is needed when the multi-module demo is used in this way.

5 Adapting Code for MPC5500 Devices

The following changes must be made to allow the software to run on a specific MPC5500 device (MPC5533/4, MPC5553/4, MPC5565/6/7). (See ‘AN2789 –MPC5500 Initialization Code’ for further information.)

File	Changes
mpc5500_usrdefs.inc	Select processor, toolset and code location (RAM or FLASH). Alter FMPLL settings for appropriate crystal.
makefile	Select appropriate linker file.
Project source files	Include appropriate header file for device

NOTE

The code must be rebuilt after making any changes, by executing the makefile found in the ‘WR’ folder of each EVB (using ‘make’ and ‘make clean’ commands). Then it must be reloaded to each EVB’s target memory.

6 In Conclusion

The multi-module demo provides an example of multiple MPC5500 modules operating together. The software can be downloaded from the Freescale website at http://www.freescale.com. This demo was developed for the MPC5561, but can be adapted to run on any MPC5500 device.

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