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Application Note

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Differences between the TI MSP430 and MC9S08QE128 and MCF51QE128 Flexis Microcontrollers

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1 Introduction

From the RS08 to our highest-performance ColdFire® V4 devices, the Controller Continuum provides compatibility for an easy migration path up or down the performance spectrum. The connection point on the Controller Continuum is where complimentary families of the S08 and ColdFire V1 (CFV1) microcontrollers share a common set of peripherals and development tools to deliver the ultimate in migration flexibility. Pin-for-pin compatibility between many devices allows controller exchanges without redesigning the board. The MC9S08QE128 and the MCF51QE128 are the first products in this series known as Flexis.

The term Flexis means a single development tool to ease migration between 8-bit (S08) and 32-bit (CFV1), a common peripheral set to preserve software investment between 8-bit and 32-bit, and pin compatibility wherever practical, to maximize hardware reuse when moving between 8-bit and 32-bit.

Contents

This application note compares the Texas Instruments MSP430FG4619 to the QE128 devices from Freescale Semiconductor and highlights ways engineers can improve their power performance by using either of the Flexis devices.

NOTE

In the following text when the QE128 is referenced, this statement is applicable to both MC9S08QE128 and MCF51QE128. If the statement is only applicable to one or the other then the full part number is used.

The details of the MSP430 are based on publicly available data and form the basis of a comparative analysis to the QE128 devices on a number of features. For in depth analysis of the MSP430, Texas Instruments must be contacted directly.

2 Top Level Specification Comparison

The MSP430FG4619 and the QE128 are not identical parts in terms of pin count or features, but are reasonably similar and are targeted at similar applications. Table 1 gives a brief comparison of the devices.

Table 1. Feature Comparison Table

Features	Cross Reference	MSP430FG4619	QE128
Supply voltage range	n/a	1.8 V to 3.6 V	1.8 V to 3.6 V
Flash size	Section 3.10.2	120K	128K
Flash programming range	Section 3.10.4	2.7 V to 3.6 V	1.8 V to 3.6 V
RAM size	n/a	Up to 8K	Up to 8K
Pin quantity	n/a	100	Up to 80
Analog comparator (ACMP)	Section 3.2	1	2
Max CPU speed	n/a	8 MHz	50.233 MHz
Analog to digital convertor (ADC) channels (12-bit)	Section 3.1	12	Up to 24
Clock generation module	Section 4	FLL with up to two external or one internal source	FLL with one internal or one external source
Digital to analog convertor (DAC)	n/a	2-ch 12-bit	None
Debugger	Section 3.12	JTAG	BDC and DBG
Direct memory access (DMA)	n/a	Yes	None
Hardware multiplier	Section 3.5	Yes, 16-bit (peripheral)	Yes, up to 32-bit (core)
Inter IC (IIC)	Section 3.11.1	Up to 1	2

Table 1. Feature Comparison Table (continued)

Features	Cross Reference	MSP430FG4619	QE128
Interrupt request (IRQ)	Section 3.8	Yes	Yes
Liquid crystal display (LCD)	n/a	160 segments	None
Low voltage detect	Section 3.6	Yes, with 14 trigger levels	Yes, with 2 trigger levels
Keyboard interrupt (KBI)	Section 3.4.3	16 pins	16 pins
Port I/O	Section 3.4.1	80 (100-pin package)	70 (80-pin package)
Op Amp	n/a	3	None
RTC / Calendar	Section 3.3	Yes / Yes	Yes / No
Serial communication interface (SCI)	Section 3.11.2	Up to 2	2
Serial peripheral interface (SPI)	Section 3.11.3	Up to 3	2
Timer	Section 3.7	Up to 3	3
Watchdog	Section 3.9	Yes	Yes

The clock generation module and the core are key to the majority of the power saving techniques and these are discussed in Section 4, “Clock Generator Module” and Section 5, “CPU Cores”. A description of the differences between the peripheral modules that are common to all the devices are discussed in Section 3, “Module Comparisons”.

3 Module Comparisons

3.1 12-bit Analog to Digital Convertor (ADC)

Table 2 gives a quick overview of the key ADC parameters and shows the specification of both modules.

Table 2. Key ADC Features

Features	MSP430FG4619	QE128
Conversion time	Programmable	16-17 ADC clock cycles
Trigger	SW or timer	SW or RTC
Internal ref	1.5 V or 2.5 V (SAR supply)	1.2 V (input only)
Result registers	16	1
Total unadjusted error	2 LSB	3 LSB
Operating range	2.2 V to 3.6 V	1.8 V to 3.6 V

The 12-bit ADC on the QE128 and the MSP430FG4619 are successive approximation (SAR) modules with a selectable clock source and integrated temperature sensors. Like the ACMP, the module and the internal reference can be turned off independently on all devices.

The QE128 ADC module has a fixed cycle conversion time of 16–17 ADC clock cycles, a variation due to synchronization at start. In this time, three cycles are the sample. The MSP430FG4619 has a programmable sample and hold period.

Where the MSP430FG4619 ADC can be triggered from a timer event, the QE128 can be triggered from the RTC. This normally has very little impact to an application. The difference is the MSP430FG4619 timer trigger is more flexible (input capture, output compare or PWM) and the QE128 RTC trigger is periodic by nature.

The MSP430FG4619 has 16 register results that the QE128 application would have to simulate by software as well as the sequence conversion modes that the MSP430FG4619 incorporates.

The MSP430FG4619 ADC module operates down to 2.2 V where the QE128 ADC continues to operate with a supply of 1.8 V.

One point to note is that the QE128 does not have a DMA module. It cannot move conversion data to RAM without CPU intervention like the MSP430FG4619. This is a useful feature in low power modes. The ADC can store data for analysis while the CPU wakes at a later time.

The internal reference on the QE128 ADC can be used as input only and software means must be used to monitor the supply with it. The MSP430FG4619 internal references can be used to power the 12-bit SAR.

Otherwise, the modules operate similarly.

3.2 Analog Comparators

Table 3 gives a quick overview of the key ACMP parameters and shows the specification of both parts modules.

Table 3. Key Analog Comparator Features

Features	MSP430FG4619	QE128
Internal reference	100%, 50%, 25% or 0% of V_{cc}	1.2 V
Internal reference accuracy	100%, -6% -8% and 100% respectively	10m V
Input options	Two pins or internal reference on either input	Two pins or internal reference on non-inverting input
RC filter on output	On chip	Off chip

The analog voltage comparator on both the MSP430FG4619 and the QE128 have interrupt capabilities to enable wake up from low power modes. The ability to turn off the modules and the internal reference voltages exist on both modules and both can be configured to connect the ACMP output to a timer input capture channel.

The internal voltage reference on the QE128 is fixed at 1.2 V ($\pm$10 mV/8.3%). The MSP430FG4619 has a selectable range of 100%, 50%, 25% or 0% of the voltage supply. The 100% and 0% settings are absolute, and the 50% setting has a range of 47–50% and the 25% setting is actually 23–25%.

The MSP430FG4619 can use either an internal reference or a pin as a signal to either of the two ACMP inputs. The QE128 ACMP module can use only the internal reference as the non-inverting input or use both inputs directly from the pin.

One of the MSP430FG4619 comparator module purposes is to use as a precision slope ADC. The module has an RC filter in the output. This is not incorporated in the QE128 module but is easily incorporated into the application board design.

3.3 Real Time Counter^{QE128} / Clock^{MSP430} (RTC)

Table 4 shows the key parameters of the RTC modules and shows the functionality of each module.

Table 4. Key RTC Features

Features	MSP430FG4619	QE128
Module	Clock	Counter
Counter bits	32	8
Interrupt intervals	/8, /16, /24 and /32 bits	According to 8-bit prescaler
Calendaring	Yes	In software
Data format	BCD or Hex	Binary
Clock sources	ACLK, SMCLK or timer	Internal Osc, LPO or crystal

The MSP430FG4619 has a basic timer that extends into a real time clock. The timer can be configured as a two 8-bit or one 16-bit counter and uses the external clock as a source. The first of the 8-bit counters is used for the LCD. The QE128 does not have an LCD module. This feature will not be described further. The second 8-bit counter can be halted to reduce power consumption and generates interrupts with varying intervals based on the modules configuration. In the 16-bit mode the counters are cascaded. In RTC mode, the basic timer extends to create a 32-bit counter with a calendar function. In counter mode four individual 8-bit counters are cascaded to provide the 32-bit counter. This provides interrupt triggers at /8, /16, /24, and /32 intervals. Each counter is individually accessible and may be read or written. The RTC has automatic counting of seconds, minutes, hours, days of the week, days of the month, month, and year (including leap year) built in the hardware calendar mode, in BCD or hex formats. The RTC does not provide an alarm function, although it can be implemented in the software if required, because the module has interrupt capabilities. The RTC module can be driven by ACLK, SMCLK, or the basic timer counter that has ACLK, ACLK/256 and SMCLK as sources.

The QE128 devices have a dedicated real time counter module. The RTC is more flexible and has the choice of three clock sources, two of which are from independent internal clock sources. The 32 kHz internal oscillator. The 1 kHz low power oscillator and the third one directly from an external crystal/resonator. The RTC is an 8-bit counter with a prescaler and a software controlled interrupt period. The prescaler feature means that the counter can count in units of 31.25 µs up to 6.25 seconds with 58 steps in between. The 8-bit modulo register allows you to multiply that interval up another 256 times. The RTC can also trigger the ADC to do a conversion when the counter matches the modulo register.

The QE128 RTC module is more flexible than the MSP430FG4619 module; however calendaring has to be done all the time in the software. This software has memory space and CPU overhead implications that contain varying effects depending on the application.

3.4 I/O and Keyboard Interrupts

3.4.1 I/O

Table 5 shows the key parameters of the general purpose I/O pin circuitry and shows the capability of the functionality on all the parts.

Table 5. Key I/O Features

Features	MSP430FG4619	QE128
Data registers	Separate input and output	Input and output shared
Slew rate control	No	Yes
Drive strength control	No	Yes
Internal pull ups	No	Yes
Port manipulation	No	Set, toggle and clear on 3 ports

The MSP430FG4619 digital I/O functions are individually controlled. Each port has two data registers, one holding input data and one holding output data. The I/O are controlled by the function select register that multiplexes the digital I/O or the peripheral to the pin.

The I/O on the MS9S08QE128 is more flexible but only has one data register for both input and output. The software must take care of saving the data if the pins directions change. The QE128 I/O has the additional features of slew rate, drive strength and internal pull ups. Ports C and E have data manipulation functions set, clear, and toggle. These registers can be loaded with a binary pattern that affect the current data for the corresponding port; therefore speeding up port manipulation processing.

The MCF51QE128, has the same features as the MC9S08QE128 and also has the Rapid GPIO module on the chip. This module means that pin toggle rates are typically 1.5–3.5x faster than comparable pins mapped onto peripherals.

3.4.2 Unused Pin Termination

TI recommended termination of unused pins on the MSP430FG4619 is output, not connected to the board.

Freescale recommends that unused pins on the QE128 devices are terminated as either pullup (available internally on chip) if inputs or outputs driving high.

3.4.3 Keyboard Interrupt (KBI)

Table 6 shows the key parameters of the KBI circuitry and shows the capability of the functionality on all parts.

Table 6. Key KBI Features

Features	MSP430FG4619	QE128
Number of	16	16
Interrupt granularity	Port	Module
Pin signal	Edge	Edge with hold option

The MSP430FG4619 can enable the KBI feature on port 1 (eight pins) or port 2 (eight pins) with individual pin control like the QE128. An edge on any pin on the selected port sets a flag for the port causing an interrupt. The edge can be set as rising or falling.

The QE128 has two KBI modules each with eight pins. The QE128 has the ability to individually select the KBI pin and individually select the polarity of the edge. The QE128 can also hold the interrupt for a level sense. The interrupts can be disabled if a polling mechanism is preferred. The individual flags can be polled to highlight the pin that triggered the event.

The KBI trigger functionality is more flexible than the MSP430FG4619 feature, due to the level hold option.

3.5 Hardware Multiplier

Table 7 gives a quick overview of the key multiply, divide parameters and shows the capability of all parts.

Table 7. Key Multiply/Divide Parameters

Parameters	MSP430FG4619	MC9S08QE128	MCF51QE128
Location	Hardware multiple module	Core	Core
Multiply	16 x 16, 16 x 8, 8 x 16, 8 x 8-bit	8 x 8- bit	16x16, 32x32 max 32-bit result
Processing time (X)	8-17 CPU cycles	5 CPU cycles	
Divide	No support	16 / 8-Bit	None
Processing time (%)	n/a	6 CPU cycles	n/a

The MC9S08QE128 has a multiply instruction (MUL) embedded in the HCS08 core. MUL multiplies the 8-bit value in the index register (X) by the 8-bit value in the accumulator to obtain a 16-bit result.The upper eight bits of the 16 bit- results are located in X and the lower eight bits in the accumulator. This operation is unsigned.

The MC9S08QE128 also has a divide instruction (DIV) embedded in the core. DIV divides a 16-bit unsigned dividend by an 8-bit unsigned divisor and places the resulting quotient in the accumulator and the remainder in the index register, H. An overflow, for instance a quotient bigger than 0xFF or a divisor of zero, sets the carry bit in the core´s condition code register.

These two basic instructions, MUL AND DIV, signed and other bit size instructions can be created with software routines, for examples on how to do this, refer to application note AN3348.

The MCF51QE128 supports 16x16(word) and 32x32(long) multiplications that result in 32-bit. Support for core divide instructions are not available on the ColdFire V1, but can be supported in the software.

The MSP430 core does not have multiply or divide support. The MSP430FG4619 has a hardware multiply module that supports 16x16-bit, 16x8-bit, 8x16-bit and 8x8-bit calculations. The MSP430 core and the hardware multiply module do not support division.

3.6 Low Voltage Detect (LVD)

Table 8 shows the key parameters in the LVD circuitry, the warning levels and the trip levels along with the specified hysteresis.

Table 8. LVD Circuit Levels and Hysteresis

Levels	MSP430FG4619	QE128
Warning levels	None	2.15 V and 2.48 V
Trip levels	1.9 V[1], 2.1 V, 2.2 V, 2.3 V, 2.4 V, 2.5 V, 2.65 V, 2.8 V, 2.9 V, 3.05 V, 3.2 V, 3.35 V, 3.5 V, 3.7 V	1.84 V and 2.15 V
Hysteresis	120 mV[1], 0.1% to 1.6% of level	80 mV

The LVD module on the QE128 has two levels of warnings and two levels of trip. It can either generate an interrupt or use polling when the warning level is reached to enable critical parameters to be stored and to place the MCU into a safe state before the trip point occurs. The MCU can be held in reset until the voltage recovers or remain the same for the power on reset (POR) circuitry to manage. The POR circuitry kicks in at 1.4 V where it causes a reset. The reset is held until the voltage recovers to the low LVD threshold.

The MSP430FG4619 has a supply voltage supervisor module that incorporates both LVD- and POR- like features. The analog supply voltage or an external source can trigger the LVD circuitry (14 levels), whereas the MCU supply triggers the optional POR circuitry. It does not cause an interrupt. The SW must use polling. It also does not support warning levels before the event occurs.

3.7 Timer

Table 9 shows the timer module key features.

Table 9. Key Timer Features

Features	MSP430FG4619	QE128
Bits	16 (Timer B can be 8, 10, 12, or 16)	16
Modes	Input capture Output compare PWM (center / edge aligned) Up, down or up-down	Input capture Output compare PWM (center / edge aligned) Free running
Clock Sources	4	3
Prescalers	4	8
Interrupts	Channel event Timer overflow	Channel event Timer overflow

The QE128 has three independent 16-bit timer modules with input capture (rising, falling, or either edge), output compare and pulse width modulation (centre or edge aligned) functionality. There are two

6-channel timers and one 3-channel timer. Each module can select one of three clock sources and have eight prescaler options. They also have a free running counter mode or a 16-bit modulus to control the counter range. Each channel has an individual interrupt and each module has an overflow interrupt, that can be enabled individually.

The MSP430FG4619 has two 16-bit timer modules a 3-channel (timer A) and a 7-channel (timer B). The MSP430FG4619 timer modules have the choice of four clock sources and four prescalers. It can run on various modes: up counter, down counter, up/down counter, input capture, output compare, and PWM.

The MSP430FG4619 timer B functionality differs from timer A. Timer B can be set as 8-, 10-, 12-, or 16-bits and the registers are buffered.

The functions of the QE128 and MSP430FG4619 are very similar although the implementation of them is slightly different and require a software change.

3.8 Interrupt Request (IRQ)

Table 10 gives a quick overview of the key IRQ features and shows the specification of both parts modules.

Table 10. Key IRQ Features

Features	MSP430FG4619	QE128
Pin signal	Edge	Edge or level
Other sources	Osc fault and flash access violation	None

IRQ is a non-maskable interrupt. This function is located on a pin shared with the reset function on all of the devices.

The MSP430FG4619 can generate an IRQ/NMI when an edge occurs on the pin, provided reset function is disabled as the pin is shared, or while an oscillator fault or flash access violation occurs.

The QE128 IRQ pin is programmable to trigger the event on a rising or falling edge or on a high or low level. Flash access violations are dealt with differently on the QE128. See Section 3.10.3, “Errors for details. The QE128 oscillator module has no loss of lock or loss of clock safeguard and no true self clock mode. In the event of an oscillator fault the application is safeguarded by the watchdog, described in Section 3.9, “Watchdog. In addition to the COP, in the event losing the external crystal/resonator, the (in FEE mode) ICS module defaults back to FEI mode, however the associated registers are not updated to reflect this change. In FLL bypassed or disabled mode the clock is lost.

The IRQ function does differ from one device to the other. Care must be taken that all required functions are rebuilt while converting the application.

3.9 Watchdog

Also known as the COP, the QE128 watchdog has two clock source options, 1 kHz LPO, or the bus and four count lengths. If the feature is enabled the circuitry causes a reset if the SRS register is not written in the required timeframe.

The watchdog module on the MSP430FG4619 has two modes. In watchdog mode the module operates like the COP but is serviced by writing a password and the data to the WDTCTL register. The interval timer mode is effectively a periodic flag generation mode that must be polled.

3.10 Flash Comparison

Table 11 gives a quick overview of the key flash parameters and shows the specification of both parts flash memory.

Table 11. Key Flash Parameters

Parameters	MSP430FG4619	QE128
Write/erase cycles	10,000 (minimum)	10,000 (minimum)
Write/erase cycles	100,000 (typical)	100,000 (typical)
Data retention at Tj = 25C	100 years	>100 years
Data retention at Tj = 85C	2 years	15 years (minimum)
Block size	64 KB	64 KB
Sector size	512 bytes	512 bytes
Small write size	1 byte	1 byte
Smallest erase size	512 bytes	512 bytes
Information memory	2 x 128 bytes	None
Programming voltage	2.7 V to 3.6 V	1.8 V to 3.6 V

The flash blocks on the QE128 are automotive qualified even though the devices are not. The devices do not follow the automotive test flow, however fab process flow and qualification data that are collected on the automotive and the non-automotive parts are essentially the same. The MSP430 has yet to achieve this qualification (as of June 2007).

3.10.1 Flash Characteristics

The MSP430FG4619 typically withstands 100,000 write/erase cycles and 100 year data retention at normal room temperature falling to a minimum of 10,000 cycles and two years at high temperature. The two years data retention at T_j = 85°C was calculated for the MSP430FG4619 flash using TI application report MSP430 flash memory characteristics by Peter Forstner – SLAA334 September 2006. The application report states an activation energy of 0.6 eV for data retention using the Arrhenius equation, 100 years at 25°C is equivalent to two years at 85°C using the stated parameters in the equation.

The QE128 devices typically withstands 100,000 write/erase cycles and over 100 years data retention at normal room temperature falling to a minimum of 10,000 cycles and 15 years at high temperature. The QE128 flash activation energy is not quoted, instead a minimum of 15 years is guaranteed.

3.10.2 Flash Design

The flash memory of the QE128 consists of two 64 Kbyte blocks each divided into 128 sectors of 512 bytes. You can read from or write to one flash block while code is executing from the other flash block.

This function helps significantly with emulating EEPROM routines. The smallest size you can program at a time is a single byte and the smallest erase size is a sector (512 Bytes).

TI MSP430FG4619 also consists of two 64 Kbyte blocks. The main memory is arranged in sectors of 512 bytes like the QE128. These sections can be erased individually and the flash is byte programmable.

The only difference between the two, from a user perspective, is that the MSP430FG4619 has information memory that is two segments of 128 bytes. These sections can be erased individually or in bulk with the main memory. These two small flash areas are useful for storing serial numbers and security keys and for storing small amount of data that is updated frequently. The fact that they are separate helps to protect them from corruption by the main program.

3.10.3 Errors

If a violation occurs in either of the QE128 flash blocks the flash access error (FACCERR) bit in the flash status register is set and suppresses further commands until the bit is cleared.

The MSP430FG4619 generates a non-maskable interrupt (NMI) also known as IRQ in the event of a flash access violation as described in Section 3.8, “Interrupt Request (IRQ)

3.10.4 Programming Voltage

The most significant advantage of the QE128 flash is the ability to program down to 1.8 V, whereas the MSP430FG4619 programs down to 2.7 V. In certain applications that run off two 1.5 V/AA/LR6 batteries the ability to program down to 1.8 V prolongs battery life. Figure 1 shows how the battery life is extended.

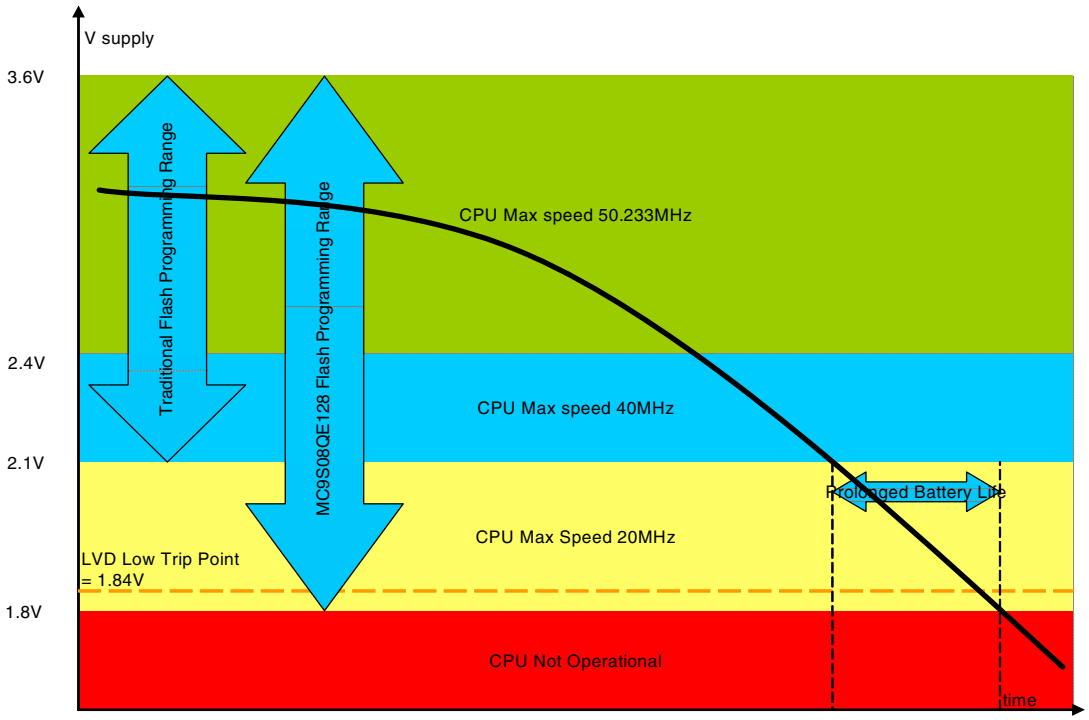

Figure 1. QE128 Flash Programming Range (axes not to scale)

If an application requires writing to the flash to store data, using the flash array to emulate EEPROM, the QE128 enables the battery life to be extended compared to the MSP430FG4619.

3.11 Communications Peripherals

The QE128 has six individual communication modules, two IIC, two SCI and two SPI. The MSP430FG4619 has three multi-mode communications modules. The first, universal synchronous asynchrounous receiver /transmitter (USART1) can be set up as an SCI or SPI, the second universal serial communication interface (USCI_A0) has three modes: SCI (IrDA option), SPI and the third USCI_B0 can be SPI or I2C. As a result the QE128 is more flexible of the two devices.

3.11.1 IIC

The IIC on the QE128 are two separate dedicated modules. Supporting the following IIC functions:

- Multi-master and slave transmit and receive modes
- General call
- Bus busy detection
- Ack generation/detection
- Start and stop generation/detection with repeated start generation
- Call address match interrupt
- Arbitration lost interrupt
- 64 frequencies selectable

The MSP430FG4619 has a very similar set of features, but the IIC is a mode of the USCI_B0 module. IIC is controlled by a state machine when selected.

3.11.2 SCI

Table 12 shows the key parameters of the SCI modules and shows the functionality of each module.

Table 12. Key SCI Features

	MSP430FG4619	QE128
Format	NRZ and IrDA (option of MSB first on USCI module)	NRZ
Baud rate	Programmable up to bus/16	Programmable up to bus/16
Parity generation	Even or odd	Even or odd
Character length	8- or 9-bit	8 or 9-bit
Break detect	10 or more	11 or 13-bit

Table 12. Key SCI Features (continued)

Buffering	Single buffer Tx and Rx	Double buffer and Tx and Rx
Wake up	Idle line or address	Idle line or address
Tx & Rx invert	No	Yes
Loop mode	Yes	Yes

The QE128 has two SCI modules on chip. They support full duplex NRZ format with programmable baud rate. The module can be interrupt driven or polled and has hardware parity generation checking along with 8-bit or 9-bit character length selection and 11-bit or 13-bit break detection. It has double buffering on the transmit and receive pins and can wake by idle line or address mark. The modules also have the option to invert the transmission and reception polarity. The SCI modules have a loop mode where the transmitter in connected internally to the receiver for error detection and can also be set for a half-duplex operation.

The SCI modules equivalent on the MSP430FG4619 is the UART_AO mode of the USART1 and USCI modules. The MSP430FG4619 UARTs also have loop mode but do not have the option to invert the transmission. The USCI UART supports IrDA communication formatting and can shift the data out MSB or LSB first, whereas the QE128 and USART shift LSB first only.

3.11.3 SPI

The SPI modules on all the devices are very similar. Table 13 highlights the main features and differences.

Table 13. Key SPI Features

	MSP430FG4619	QE128
Modes	Master or slave	Master or slave
Direction	Full duplex or bidirectional single wire	Full duplex or bidirectional single wire
Baud rate	Programmable up to CLK/2	Programmable up to bus/2
Buffering	Double buffer Tx and Rx	Single buffer and Tx and Rx
Format	MSB or LSB first	MSB or LSB first

The SPI modules on the QE128 can operate in master and slave modes in either full duplex or bidirectional single wire modes.

The bit transmission rate is programmable and like the SCI, the input and outputs are double buffered. The modules can also be set up to transmit MSB or LSB first.

The SPI modules equivalent on the MSP430FG4619 is the SPI mode of the USART and USCI modules.

The major differences are that the MSP430FG4619 SPI has separate transmit and receive control, buffer registers and separate interrupt vectors for transmit and receive, recoverable by software on QE128 as Tx and Rx not distinguished by hardware. The USCI module SPI has the functionality to run as a slave in LPM4.

3.12 Debugger

Table 14 gives a quick overview of the key debugger parameters of both parts modules.

Table 14. Key Debugger Features

	MSP430FG4619	MC9S08QE128	MCF51QE128
Type	JTAG	BDC and DBG, collectively referred to as BDM	CFI_DEBUG
Pins required	4	1	1
Fuse	Yes	None	None
Breakpoints	8	4	6

JTAG (MSP430FG4619) and BDM (QE128) are both generic real time debugging interfaces with breakpoint and trace facilities.

The BDM is a single-pin connection on the package and uses the DCOL/2 as a clock source. This means that when the FLL is disabled in FBILP or FBELP ICS modes, or the device is in stop2 or stop3 with ENBDM = 0 the debugging capabilities are not available. The BDM does not have a fuse to allow permanent disabling of the BDM. The ENBDM bit to enable the module is located in memory inaccessible by programs and therefore cannot be accessed in normal field operation.

The ColdFireV1 core supports BDM functionality using the HCS08's single-pin interface. The traditional 3-pin full-duplex ColdFire BDM serial communication protocol based on the 17-bit data packets is replaced with the HCS08 protocol where all communications are based on an 8-bit data packet using a single package pin (BKGD).

The CFV1 debug funtion supports:

- Real time debugging, with six hardware breakpoints (four PC, one address, and one data) that can be configured into a one or two level trigger with a progammable response (processor halt or interrupt).
- Capture of compressed processor status and debug data into on-chip trace buffer provides program (and optional salve bus data) trace capabilities.
- On-chip trace buffer provides programmable start/stop record conditions.
- Debug resources are accessible via single pin BDM interface or the priviliged WDEBUG instruction from the core.

JTAG requires four dedicated I/O pins on the MSP430FG4619 device as shown in Table 15. One advantage of this set up is that the JTAG is available for use as long as TCK is provided and the JTAG modules fuse is not blown.

Table 15. Standard 4-wire JTAG Signals

Pin	Direction	Usage
TMS	In	Signal to control the JTAG state machine
TCK	In	JTAG clock input
TDI	In	JTAG data input/TCLK input
TDO	Out	JTAG data output

4 Clock Generator Module

Both the ICS and the FLL+ modules on the QE128 and MSP430FG4619 respectively are based on an FLL with internal and external clock sources.

The QE128 ICS, see Figure 2, has two clock sources available at any time: the internal 32 kHz oscillator or an external reference clock that can be from 32 to 38.4 kHz (low range), or 1 to 16 MHz (high range). The internal oscillator can be in the range of 25 to 41.66 kHz if untrimmed and can be trimmed to 31.25 to 39.06 kHz. The FLL must be fed with a reference in the range of 31.25 to 39.06 kHz. The reference divider (RDIV) can be used to divide down the higher frequency external source to meet this requirement. The FLL has three digitally controlled oscillator (DCO) multipliers: low (512), medium (1024) and high (1536) and a fine tuning function to maximize the output frequency when 32.768 kHz is the reference. The ICS module can be in FLL enabled, FLL bypassed and FLL disabled modes with either the internal or external clocks as references. It can also output the internal or external clock sources directly in to the MCU for use as sources for other modules regardless of the FLL settings.

The FLL+ module on the MSP430FG4619, see Figure 3, can be configured to operate with one or two external crystals/resonators or the internal 1 MHz DCO[1]. The first crystal input can be supplied by a 32.768 kHz crystal if it is set up for LF mode. The second source does not support this mode. Both the crystal inputs have two other frequency choices: a ceramic resonator, 450 to 8000 kHz, or a 1 to 8 MHz crystal. The FLL input frequency is not limited like the HCS08 ICS version but the input range must be specified. The DCO output can be divided down by 1, 2, 4, or 8 and used as the CPU/bus clock. The FLL can be disabled and bypassed, and different clock signals from the module can be used by the peripheral modules regardless of FLL settings, like the ICS.

1. Note that the term DCO in terms of the Freescale ICS references the FLL source multiplier mechanism, whereas the term DCO in regards to the TI FLL+ references the 1 MHz oscillator and the multiplier.

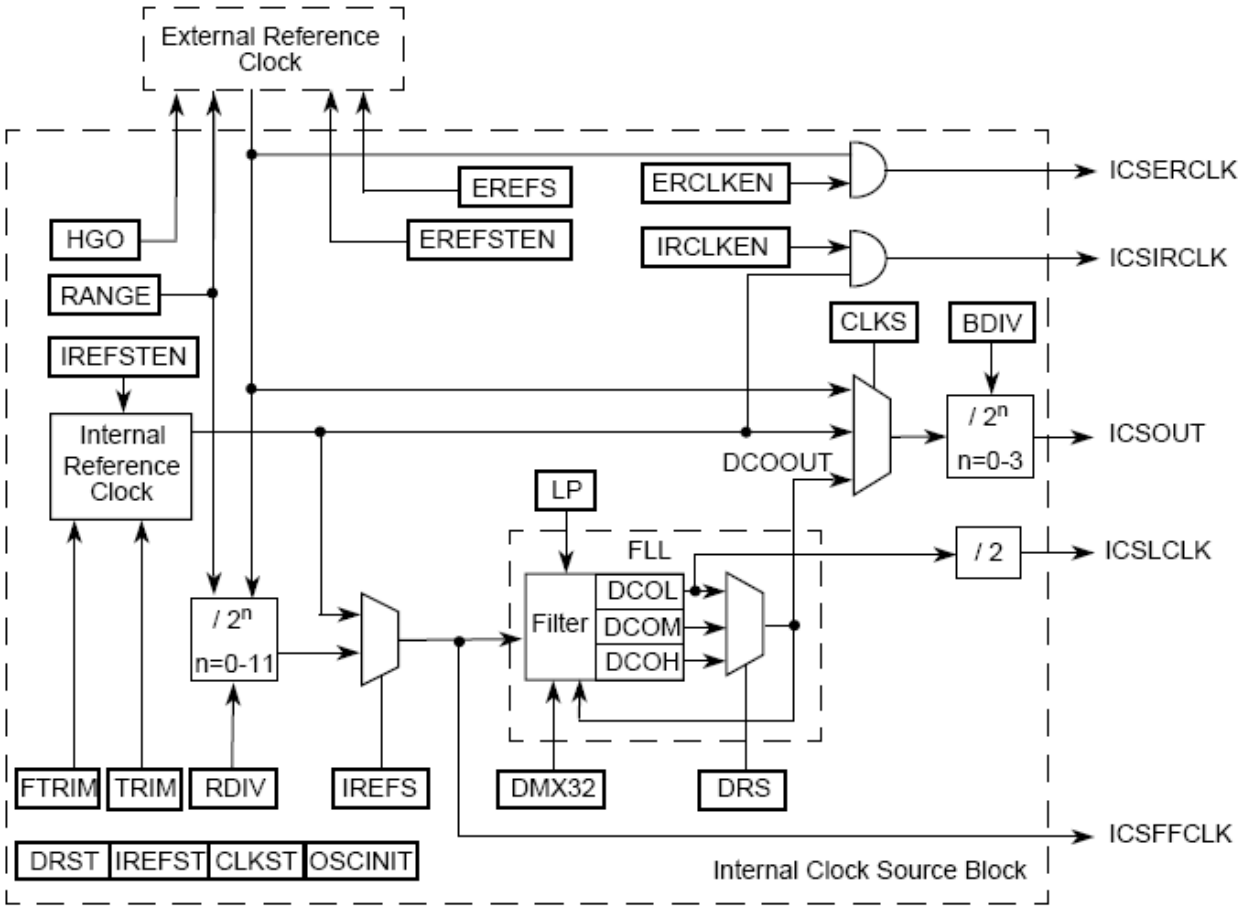

Figure 2. QE128 ICS Module Block Diagram

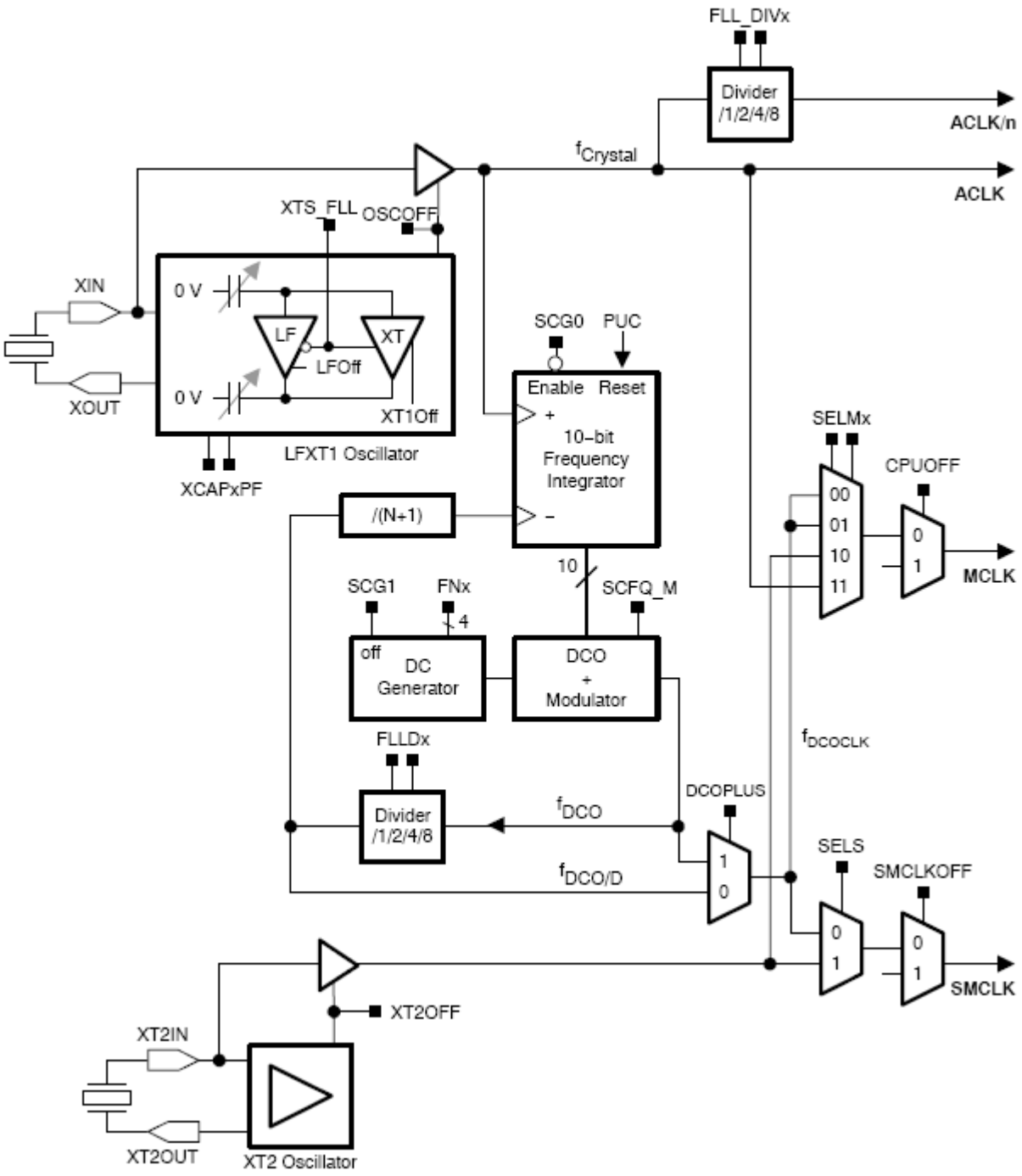

Figure 3. MSP430FG4619 FLL+ Module Block Diagram

4.1 Functional Differences

4.1.1 FLL

The FLL block in the ICS has a limited input range of 31.25 to 39.06 kHz to ensure the DCO operates around the center of the taps. The FLL+ module does not have this limitation. The DCO range can be adjusted by the FNx bits as shown in Table 16.

Table 16. FLL+ DCO Range Control Bits

FN_8	FN_4	FN_3	FN_2	Typical f_{DCO} Range
0	0	0	0	0.65—6.1
0	0	0	1	1.3—12.1
0	0	1	X	2—17.9
0	1	X	X	2.8—26.6
1	X	X	X	4.2—46

The FLL+ FLL input frequency is manipulated by the settings of FLLD (x1, x2, x4, x8) and N (seven bits in the system clock control register). The QE128 ICS module has three DCO ranges and a bus divider (BDIV) that control the ICS output frequency.

Table 17 illustrates examples of clock module output frequency ranges with 32.768 kHz and 8 MHz crystals.

Table 17. Clock Generation Ranges

Device	Source	Min CPU / MCLK	Max CPU / MCLK	Settings	Comment
QE128	32.768 kHz	4.096kHz	—	BDIV /8	FLL bypassed
		—	50.33MHz	DCOH, BDIV /1	Max CPU speed reached
	8MHz	1MHz	—	BDIV /8	FLL bypassed
		—	48MHz	RDIV /256, DCOH, BDIV /1	
MSP430FG4619	32.768 kHz	4.096kHz	—	SELM = 0X, FLLD = 8	
		—	4.194MHz	SELM = 0X, N = 127,	
	8MHz	1MHz	—	SELM = 0X, FLLD = 8, N = 0	
		—	8MHz	SELM = 11	FLL bypassed, max CPU speed reached

4.1.2 CPU Clock Disabling

The FLL+ module has a bit, CPUOFF that can disable the CPU/MCLK clock signal effectively placing the MCU into a low power state. The QE128 CPU controls this feature using STOP and WAIT instructions.

4.1.3 FLL Disabling

If the FLL is disabled on the ICS the DCOOUT frequency is zero. The FLL+ module continues to run at previous frequency if disabled, but it is not stabilized.

This feature is available on some HCS08 devices with the internal clock generator (ICG) module integrated rather than the ICS (see www.freescale.com for details) but the internal or external reference can be used with the FLL bypassed by changing the CLKS and BDIV settings a clock signal. This can be maintained at all times with careful consideration to the software routine.

4.2 Clock Modes

Table 18 shows the six ICS modes and their equivalent FLL+ setting, if applicable.

Table 18. Clock Generation Module Mode Comparison

Characteristic/Function	MSP430FG4619 FLL+ Mode	QE128 ICS Mode
FLL on, using internal oscillator to supply CPU and bus clocks	Not supported	FLL engaged internal (FEI)
FLL on, using external oscillator supplying CPU and bus clocks	SELMx = 0X SCG0 = 0 SCG1 = 0	FLL engaged external (FEE)
FLL on, but CPU and bus clocks supplied directly from internal oscillator	FLL+ loop control off, N used to multiply	FLL bypassed internal (FBI)
FLL off, BDC disabled, CPU and bus clocks supplied directly from internal oscillator	Not supported	FLL bypassed internal low power (FBILP)
FLL on, but CPU and bus clocks supplied directly from external oscillator	SELMx = 1X SCG0 = X SCG1 = X	FLL bypassed external (FBE)
FLL off, BDC disabled, CPU and bus clocks supplied directly from external oscillator	SELMx = 1X SCG0 = 1 SCG1 = X	FLL bypassed external low power (FBELP)
FLL off, BDC disabled, internal/external clocks can be enabled/disabled in software	SCG0 = 1 SCG1 = 1 OSCOFF = 1 CPUOFF = 1	Stop2
FLL disabled, but DCOOUT running.	SELMx = 0X SCG0 = 1 SCG1 = 1	Self clock mode (not available on ICS)

4.3 Clock Gating

The QE128 has a very flexible clock gating feature controlled by two simple registers, SCGC1 and SCGC2 as shown in Figure 4. By gating off the clock to unused modules precious micro amps (μA) can be saved in the MCU run and wait modes. This feature is especially important because of the numerous communications modules and timers incorporated in the QE128. Applications are unlikely to use all of them. Benefits can be found by only gating the modules in the section of the application that needs them and by gating them off when the job is done.

	7	6	5	4	3	2	1	0
R W	TPM3	TPM2	TPM1	ADC	IIC2	IIC1	SCI2	SC1
Reset	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
R W	DBG	FLS	IRQ	KBI	ACMP	RTC	SPI2	SPI1
Reset	1	1	1	1	1	1	1	1

Figure 4. System Clock Gating Registers

The MSP430FG4619 does not have such a register. MCLK, SMCLK an ACLK(/n) can be disabled individually but as many modules can use these clock sources. This is not a very flexible solution.

5 CPU Cores

The MSP430 core, the HCS08 core and the ColdFire V1 core are very different and therefore hard to compare. The HCS08 is an 8-bit CPU with a CISC instruction set, the MSP430 is a 16-bit RISC core and ColdFireV1 is a 32-bit variable length (VL) RISC core.

5.1 CPU Performance

Benchmarking results depend heavily on the type of application running and the C compiler efficiency. In very general terms ColdFire V1 is the highest performance core, followed by the MSP430 and then followed very closely by the HCS08.

The relative performance per MHz for these cores may be similar, but the absolute performance for the QE128 is considerably higher because of the sizable difference in maximum operating frequency. Both QE128 parts provide a very distinct maximum performance advantage versus the MSP430FG4619.

5.2 CPU Modes

The QE128 and the MSP430FG4619 have six modes of operation each.

- Run mode of the QE128 is the equivalent of active mode on the MSP430FG4619.
- Low power run (LPR) mode on the QE128 is the equivalent of a low speed active mode with the FLL disabled.
- Wait mode on the QE128 is equivalent to LPM0 as the CPU is not clocked but the FLL is enabled.
- Low power wait (LPW) mode is the equivalent of LPM1 as the CPU is not clocked and the FLL is disabled.

- Stop3 mode on the QE128 devices is equivalent to LPM2 or LPM3 depending on the stop3 settings. Stop3 and LPM3 have wake up times of 6µs.
- Stop2 mode is equivalent to LPM4.

5.2.1 CPU Modes and Clock Availability

Table 19 illustrates which clock sources can be used by which modules. The QE128, IRCLK, ERCLK and the LPO are available in all modes of operation. The ICSOUT and XCLK are available in run and wait, including low power. The ICSLCLK is available in run, wait and stop3, if BDM is enabled.

On the MSP430FG4619, the MCLK is directly dependant on the CPUOFF bit and is only available in active mode. The ACLK is available in active and LPM0–LPM3. The SMCLK depends upon the availability of the second oscillator and if so, runs in active and LPM0–LPM1.

Table 19. Module Clock Sources

Module	MSP430FG4619				QE128				
	MCLK	ACLK	SMCLK	Other	ICSOUT	IRCLK	ERCLK	LPO	Other
ACMP	X				/2		X		
ADC	X	X	X	Internal ADC 5 MHz osc	/2		X		
COP	X	X	X		/2			X	
CPU	X				/1				
Debugger	X			TCK					ICSLCLK
Flash	X	X	X		/2				
IIC		X	X	Master	/2				
RTC		X	X	Timer		X		X	OSCOUT
SCI		X	X	Master	/2				
SPI		X	X	Master	/2				
TPM		X	X	External source	/2				XCLK or external source

5.2.2 CPU Mode Transitions and Exits

The QE128 devices have a clear map of allowable mode transitions as shown in Figure 5.

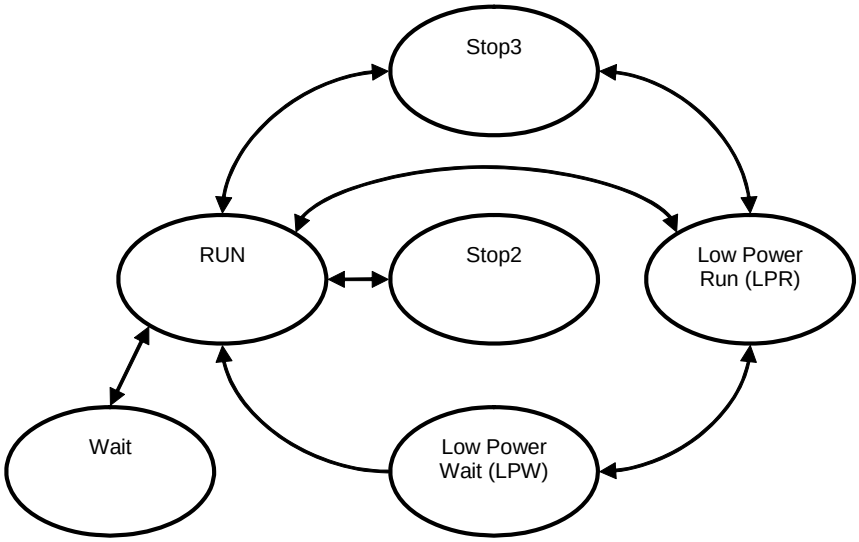

Figure 5. HCS08 and ColdFireV1 CPU Mode Transitions

The MCU can be put into and out of LPR mode by the single LP bit in the ICS module provided that all the required conditions are met.

Exit from wait and LPW can be achieved through any enabled interrupt, therefore any module can place the MCU back into run or LPR mode.

Entry into stop3 and stop2 is governed by the setting of the PPDC bit in the SPMSC2 register and the setting on the BDM and LVD modules. The RTC, LVD/LVW, ADC, ACMP, IRQ, SCI and KBI modules bring the MCU out of stop3 as well as a reset. RTC, IRQ or RESET are the only paths out of stop2. Stop2 mode exists as if a POR was executed.

The mode selections chapter in the QE128 reference manuals describes these mode transitions in full. The MSP430FG4619 moves through modes via active mode as shown in Figure 6.

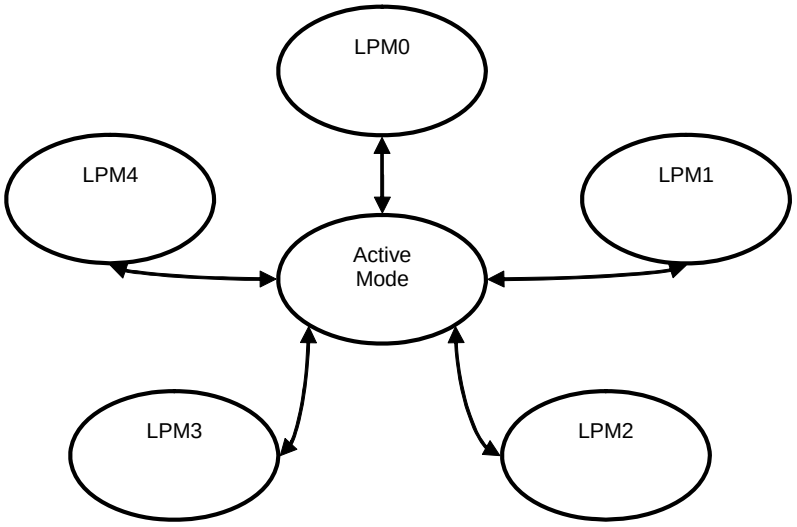

Figure 6. MSP430x4xx CPU Mode Transitions

The setting of the SCG0, SCG1, OSCOFF and CPUOFF bits in the CPU status register, govern the mode transitions. Any enabled interrupt can bring the MCU out of the low power modes.

The watchdog modules on the QE128 and the MSP430FG4619 devices cause a reset which after the startup routine, place the device back in to run/active mode.

6 Conclusion

The MSP430FG4619 and the QE128 are not identical parts in terms of pin count or features but are reasonably similar and are targeted at similar applications. The common modules, although implemented differently are more often than not similar in terms of features, but have different results in terms of power consumption.

The second in this series of application notes (available early 2008) comparing the MSP430FG4619 and the QE128 concentrate on showing, by example, how to convert a typical MSP430FG4619 application in to a QE128 application.

7 Bibliography

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