Application Note

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Generating Clocks for HC908 MCU Families

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Introduction

This document shows how to generate clock signals for each the following HC908 Motorola 8-bit MCU Families:

HC908JK/JL
HC908KL
HC908JB
HC908BD
HC908GT
HC908KX
HC908EY
HC908RF/RK
HC908AB/AS/AZ/MR
HC908GZ
HC908GP/GR
HC908LJ
HC908LD
HC908SR
HC908QT/QY

The figures in the first section are illustrations of clock distribution for each group of MCUs. They depict main sections of the MCU, clock generation, and distribution blocks and define the main clocks' limits, their respective control bits, and values. In the final sections are descriptions of methods of programming the phase-locked loop (PLL) modules, with several example values.

NOTE: *With the exception of mask set errata documents, if any other Motorola document contains information that conflicts with the information in the device data sheet, the data sheet should be considered to have the most current and correct data.*

HC908JK/JL

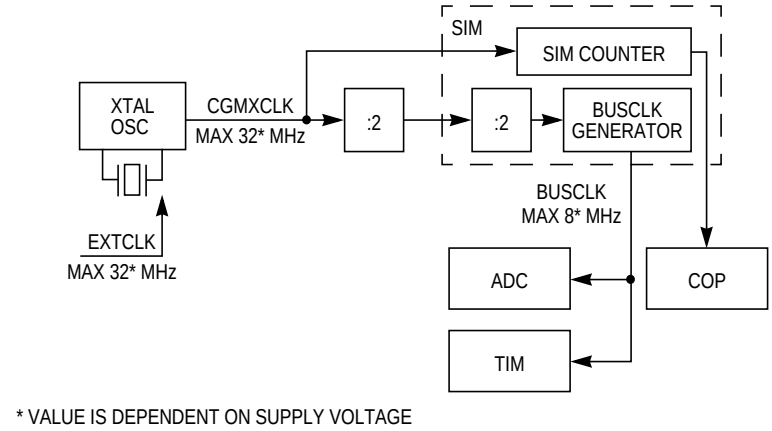

Figure 1. Distribution Clock Signals in the JK/JL Families

The frequency of a crystal element is determined by the following equation:

$$f_{BUSCLK} = f_{CGMXCLK}/4$$

Maximum bus frequency for 3-V operation is 4 MHz; for 5-V operation, it is 8 MHz. Either the external crystal or the external clock source frequency can be used as the clock source.

NOTE: *The analog-to-digital converter (ADC) clock should be set to approximately 1 MHz as recommended in the data sheet.*

For example, for an 8-MHz bus clock, the ADICLK register should be set to $60; for a 4-MHz bus clock, it should be set to $40.

HC908KL

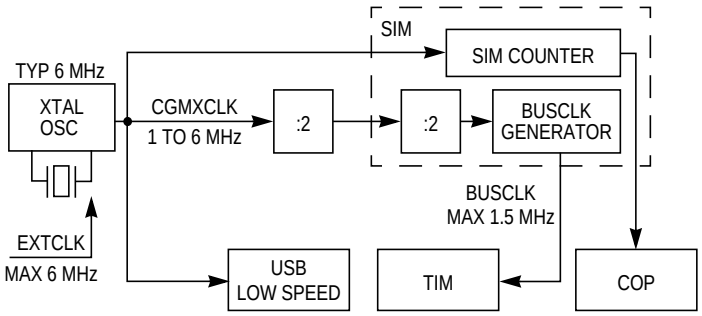

Figure 2. Distribution Clock Signals in the KL Family

The frequency of a crystal element is determined by the following equation:

$$f_{BUSCLK} = f_{CGMXCLK}/4$$

The low-speed USB data rate is nominally 1.5 Mbps. The CGMXCLK signal driven by the oscillator circuit is the clock source for the USB module. It requires a 6-MHz oscillator circuit connected to the OSC1 and OSC2 pins.

HC908JB

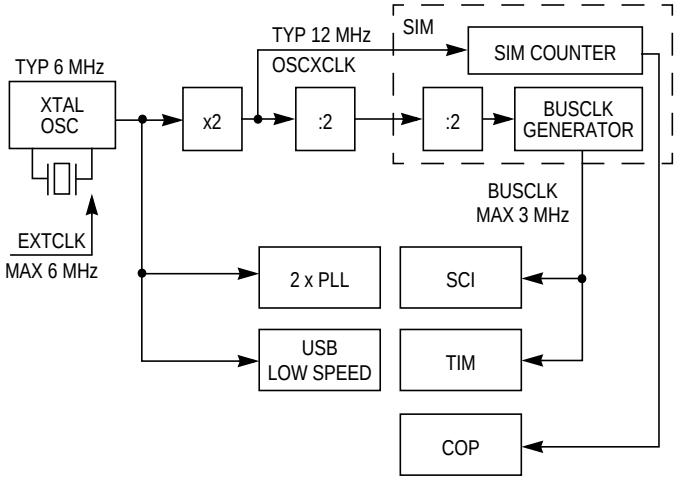

Figure 3. Distribution Clock Signals in the JB Family

The frequency of a crystal element is determined by the following equation:

$$f_{BUSCLK} = f_{OSCXCLK}/4$$

The low-speed USB data rate is nominally 1.5 Mbps. The signal driven by the oscillator circuit is the clock source for the USB module. It requires a 6-MHz crystal element connected to the OSC1 and OSC2 pins.

There are two identical PLL frequency generator modules, which are designed as two independent, fully programmable clock generators, intended for 27-MHz RF applications. Each module contains all the function blocks for the PLL internal voltage controlled oscillator (VCO) control and are designed to be used with a crystal reference.

HC908BD

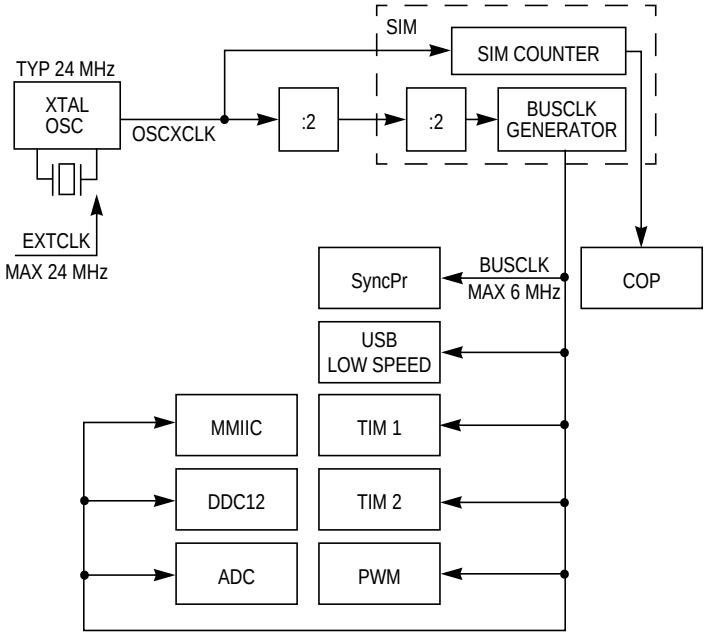

Figure 4. Distribution Clock Signals in the BD Family

The low-speed USB data rate is nominally 1.5 Mbps. The clock source for the USB module is the bus clock. It requires a 24-MHz crystal element connected to the OSC1 and OSC2 pins.

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet.

If the crystal frequency is equal to 24 MHz, the ADICLK register should be set to $60. In this case, the ADC clock is equal to 0.75 MHz.

The recommended working bus clock frequency of the sync processor is 6 MHz. This module is designed to detect and process sync signals from separated Hsync and Vsync inputs, or from a composite sync input signal inside a digital monitor system.

HC908GT

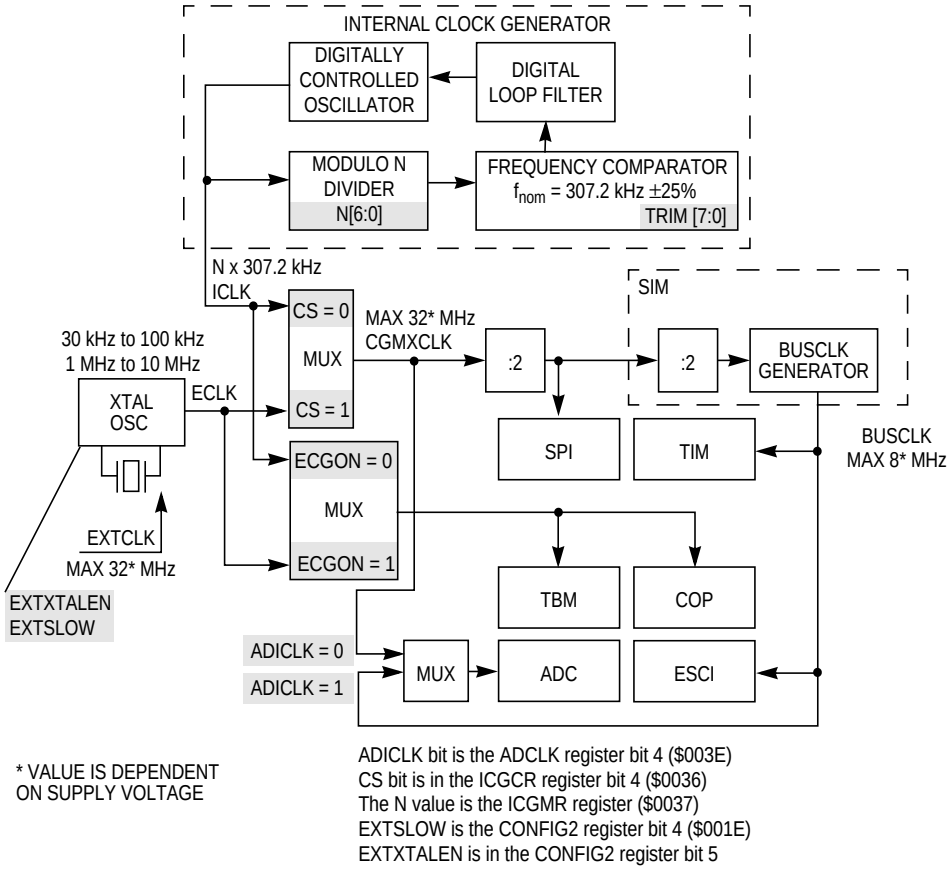

Figure 5. Distribution Clock Signals in the GT Family

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the bus clock can be used as the clock source for the ADC.

If an 8-MHz bus clock provides the clock source for the ADC module, the ADICLK register should be set to $60. If the bus clock is equal to 4 MHz, the ADICLK register should be set to $40.

The internal oscillator is free-running at a standard frequency of 307.2 kHz ±25% and can be trimmed to max ±5% by setting the value of the TRIM register.

The internal clock generator (ICG) provides the internal clock source (ICLK), which is an integer multiple N of the internal oscillator frequency.

Programming the Internal Clock Generator (ICG) shows detailed information on programming the PLL and gives several examples.

HC908KX

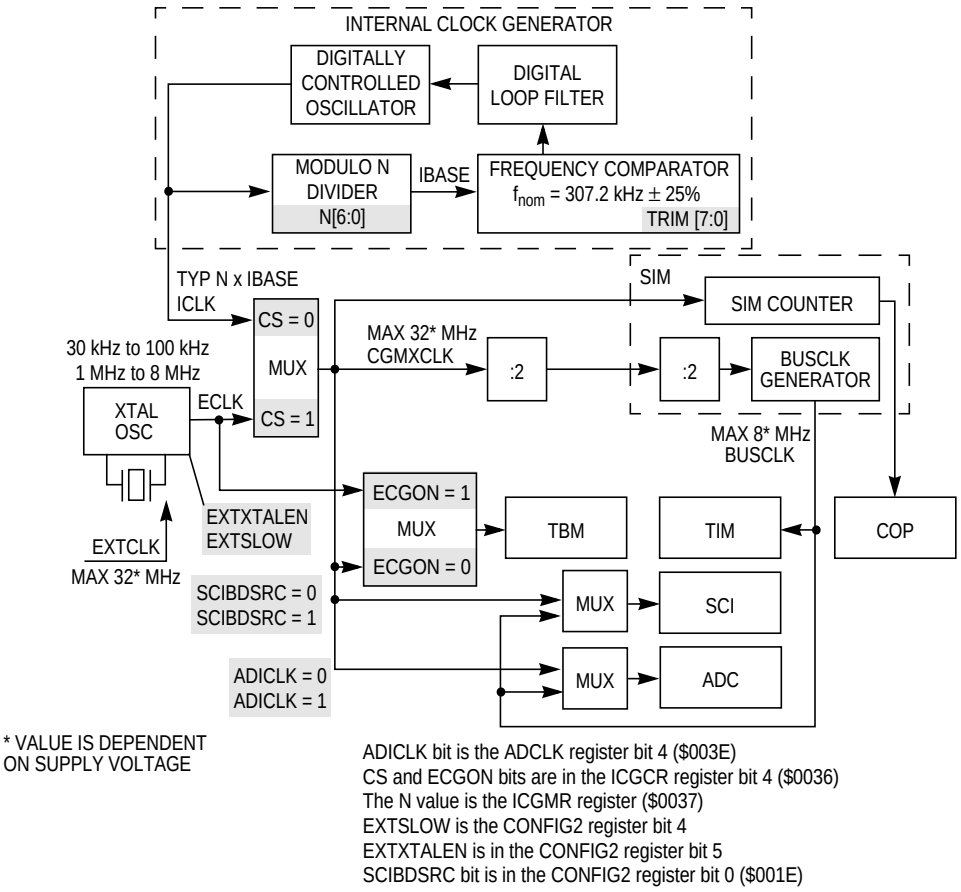

Figure 6. Distribution Clock Signals in the KX Family

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the bus clock can be used as the ADC clock source.

The baud rate for the SCI is determined by this formula:

$$\text{baudrate} = \frac{\text{InputCLK}}{64 \times \text{PD} \times \text{BD}}$$

- PD (prescaler divisor) — SCP[1:0] in the SCBR register
- BD (baud rate divisor) — SCR[2:0] in the SCBR register
- The recommended XTAL frequency (for SCI) is 4.9152 MHz

Programming the Internal Clock Generator (ICG) shows detailed information on programming the PLL and gives several examples.

HC908EY

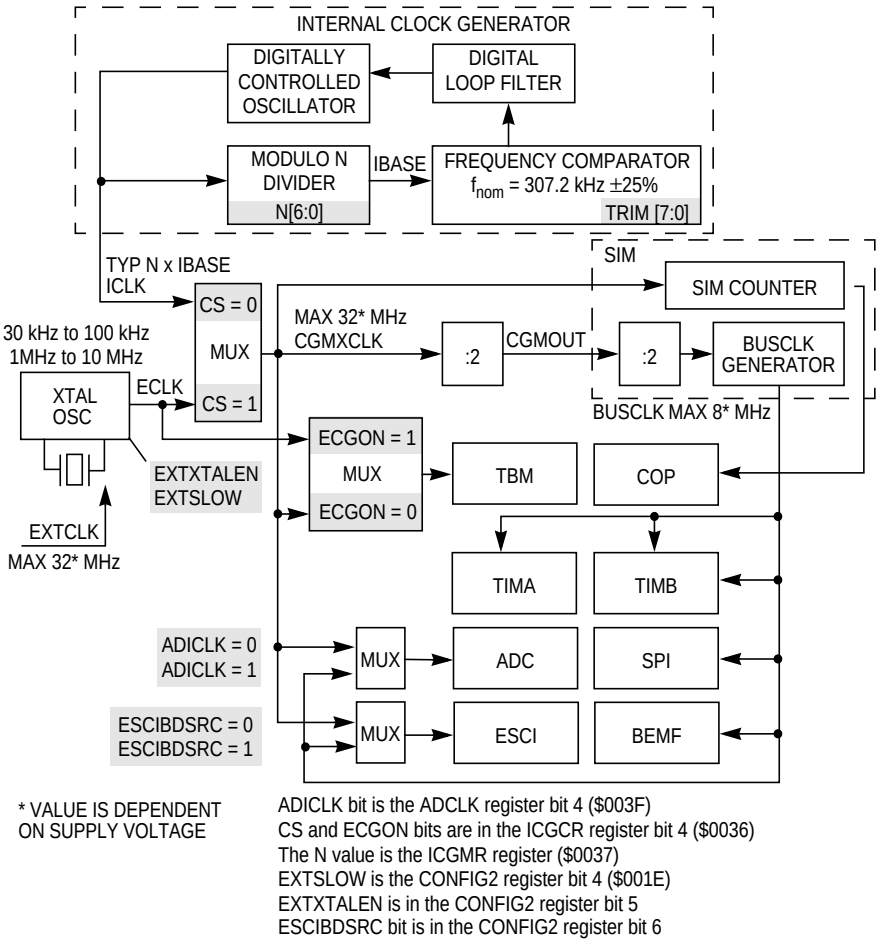

Figure 7. Distribution Clock Signals in the EY Family

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the bus clock can be used as the clock source for the ADC.

The internal oscillator is free-running at a standard frequency of 307.2 kHz ±25% and can be trimmed to max ±5% by setting the value of TRIM register.

The ICG provides the internal clock source (ICLK), which is an integer multiple N of the internal oscillator frequency.

Programming the Internal Clock Generator (ICG) shows detailed information on programming the PLL and gives several examples.

HC908RF/RK

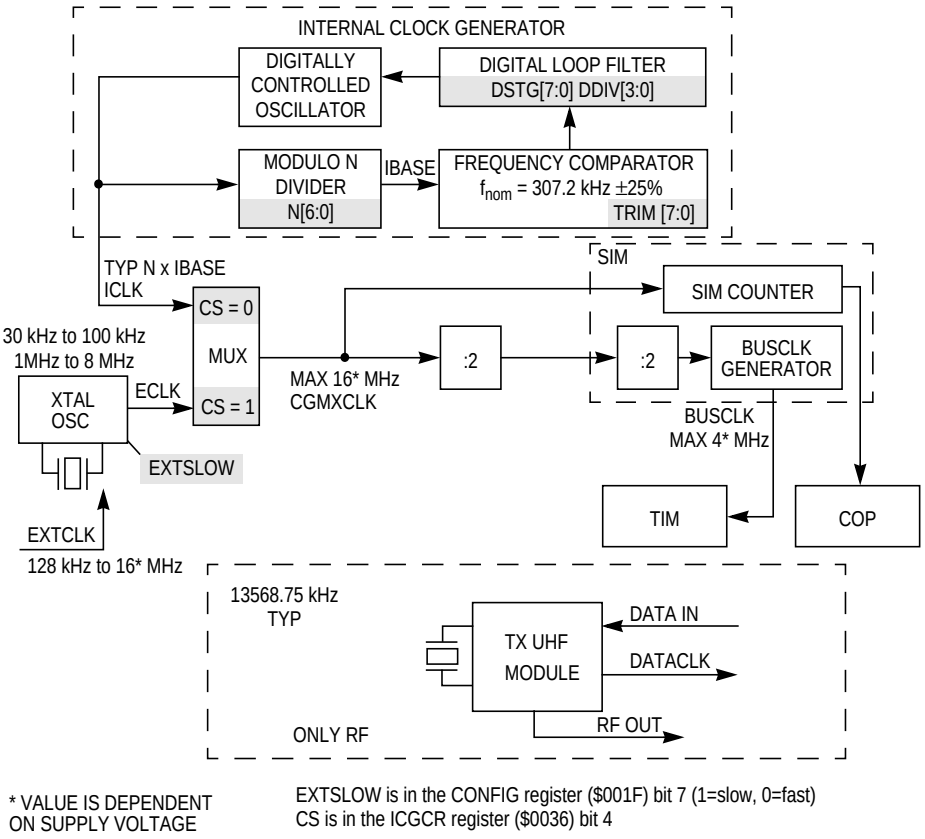

Figure 8. Distribution Clock Signals in the RF/RK Families

The internal oscillator is free-running at a standard frequency of 307.2 kHz ±25%, and can be trimmed to max ±5% by setting the value of TRIM register.

The ICG provides the internal clock source (ICLK), which is an integer multiple N of internal oscillator frequency.

The ultra high frequency (UHF) transmit module is integrated into the RF Family MCUs. The UHF module can operate in the 315 MHz, 434 MHz, and 868 MHz industrial, scientific, and medical (ISM) bands, with on/off keying (OOK) and frequency shift keying (FSK) modulation.

Programming the Internal Clock Generator (ICG) shows detailed information on programming the PLL and gives several examples.

HC908AB/AS/AZ/MR

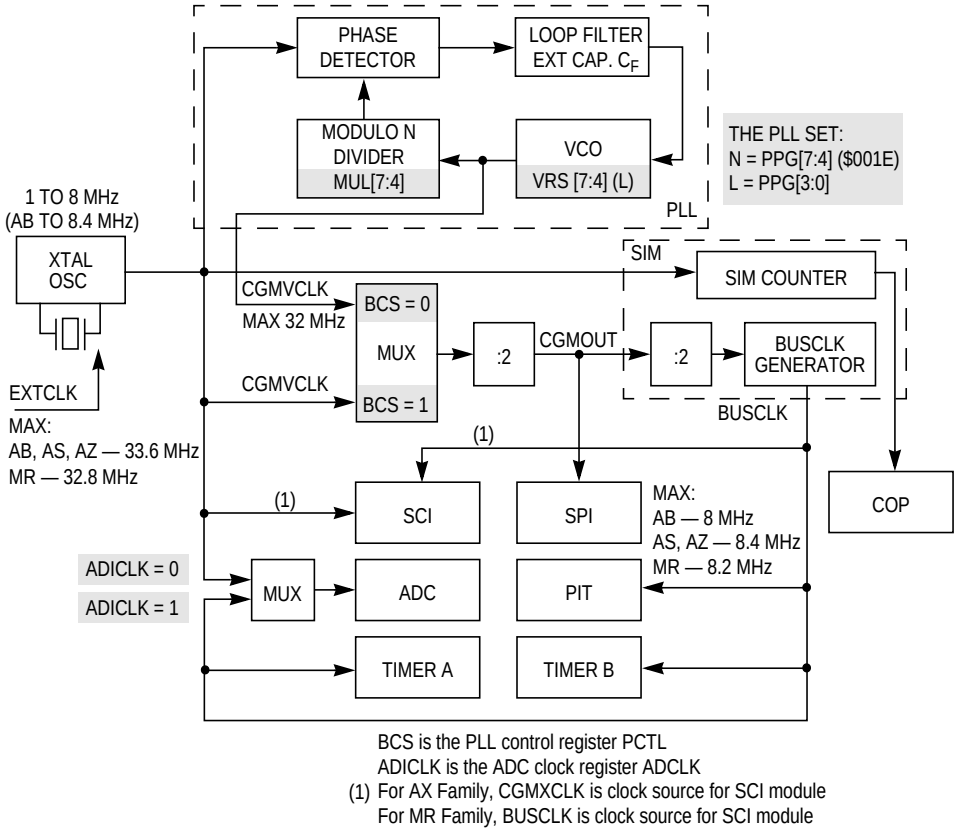

Figure 9. Distribution Clock Signals in the AB/AS/AZ/MR Families

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the BUSCLK can be used as the clock source for the ADC. In this case, the PLL module can be used to generate the internal BUSCLK.

Baud rate for the SCI is determined by this formula:

$$\text{baudrate} = \frac{f_{CLK}}{64 \times PD \times BD}$$

- PD (prescaler divisor) — SCP[1:0] in the SCBR register
- BD (baud rate divisor) — SCR[2:0] in the SCBR register

Programming the PLL-1 shows detailed information on programming the PLL and provides several examples.

HC908GZ

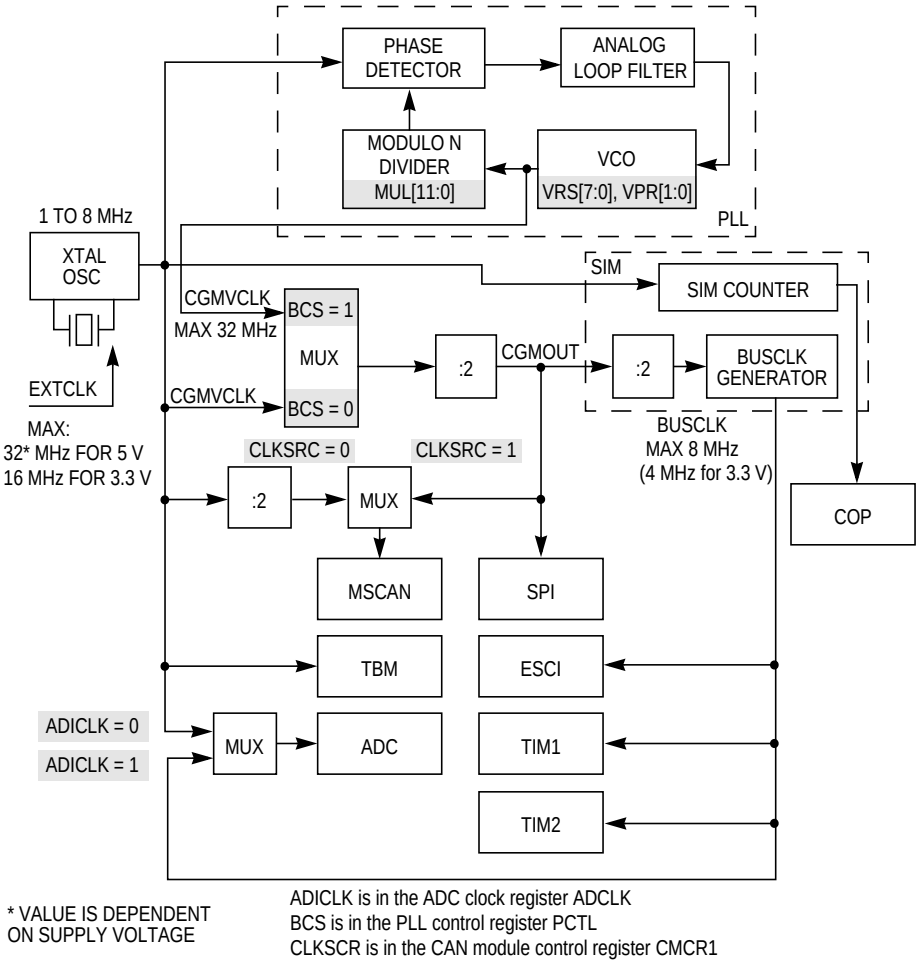

Figure 10. Distribution Clock Signals in the GZ Family

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the BUSCLK can be used as the clock source for the ADC. In this case, the PLL module can be used to generate the internal BUSCLK.

Programming the PLL-2 shows detailed information on programming the PLL and provides several examples.

The MSCAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH specification dated September 1991. The programmable bit rate is up to 1 Mbps.

HC908GP/GR

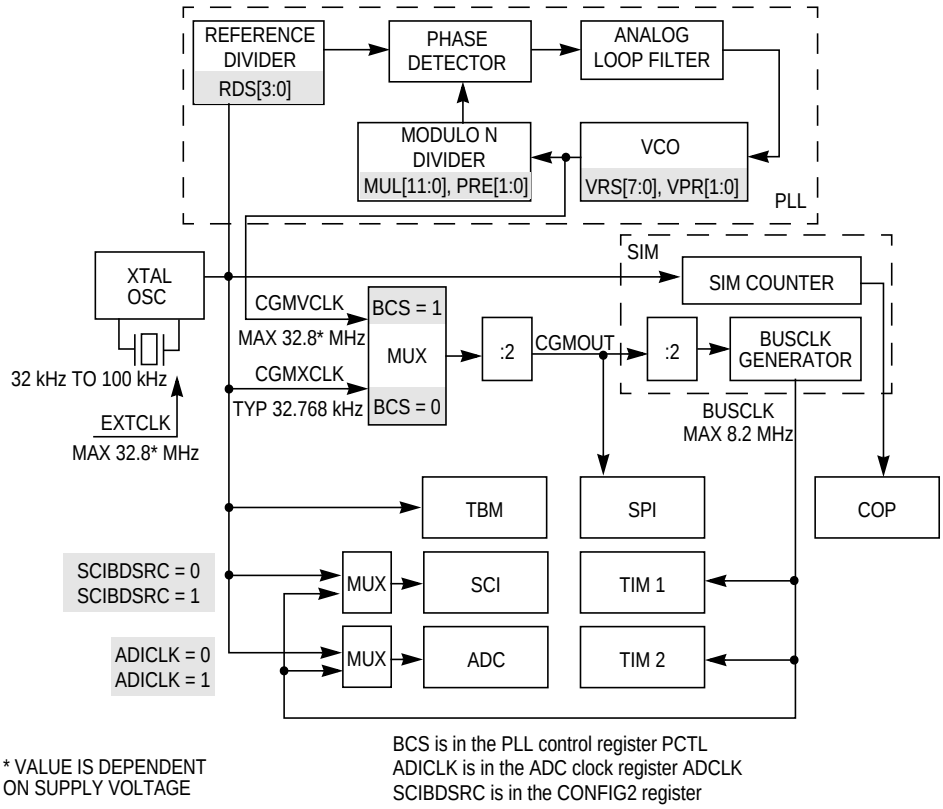

Figure 11. Distribution Clock Signals in the GP/GR Families

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the BUSCLK can be used as the clock source for the ADC. In this case, the PLL module can be used to generate the internal BUSCLK.

Baud rate for the SCI is determined by this formula:

$$\text{baudrate} = \frac{\text{InputCLK}}{64 \times \text{PD} \times \text{BD}}$$

- PD (prescaler divisor) — SCP[1:0] in the SCBR register
- BD (baud rate divisor) — SCR[2:0] in the SCBR register
- The Recommended clock frequency for SCI is 4.9152 MHz

Programming the PLL-3 shows detailed information on programming the PLL and provides several examples.

HC908LJ

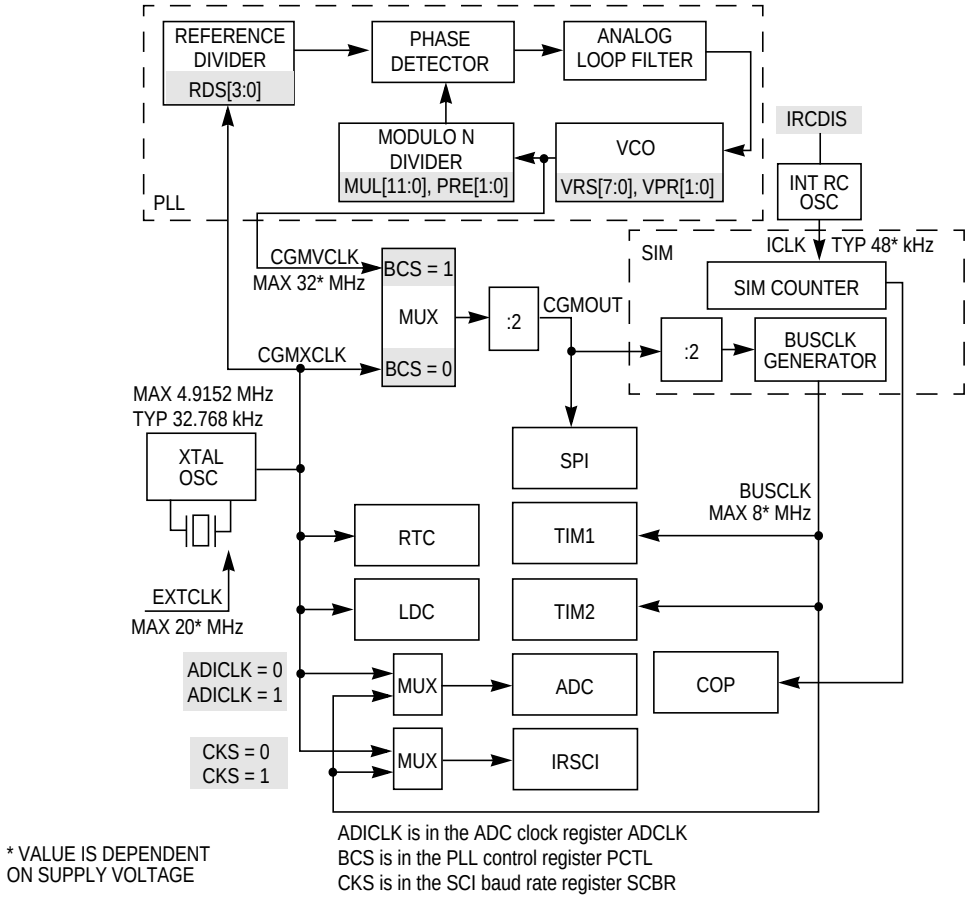

Figure 12. Distribution Clock Signals in the LJ Family

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the BUSCLK can be used as the clock source for the ADC. In this case, the PLL module can be used to generate the internal BUSCLK.

The internal RC oscillator is free-running at a typical frequency of 48 kHz and drives the SIM counter and COP module in sequence. This frequency decreases to 44 kHz with decreasing the supply voltage to 3 V.

Programming the PLL-3 shows detailed information on programming the PLL and provides several examples.

HC908LD

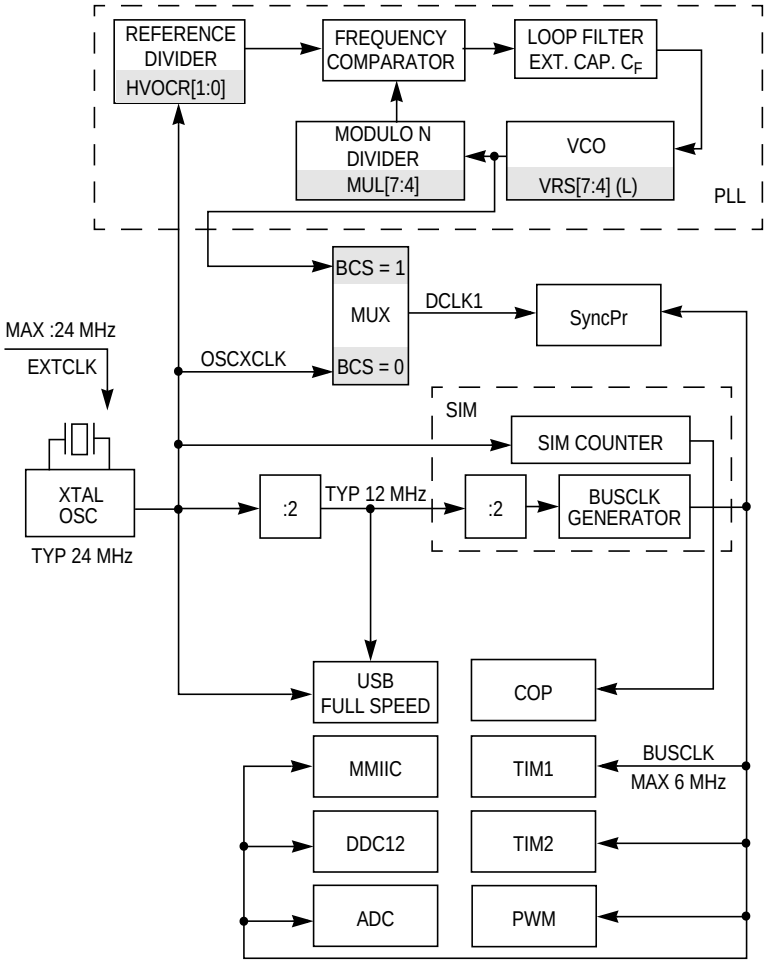

Figure 13. Distribution Clock Signals in the LD Family

The high-speed USB data rate is nominally 12 Mbps. The clock source for the USB module is the OSCXCLK. It requires a 24-MHz oscillator circuit connected to the OSC1 and OSC2 pins. This USB module supports both embedded full speed device and hub functions and contains one upstream port and four downstream ports.

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet.

Programming the PLL-4 shows detailed information on programming the PLL and provides several examples.

HC908SR

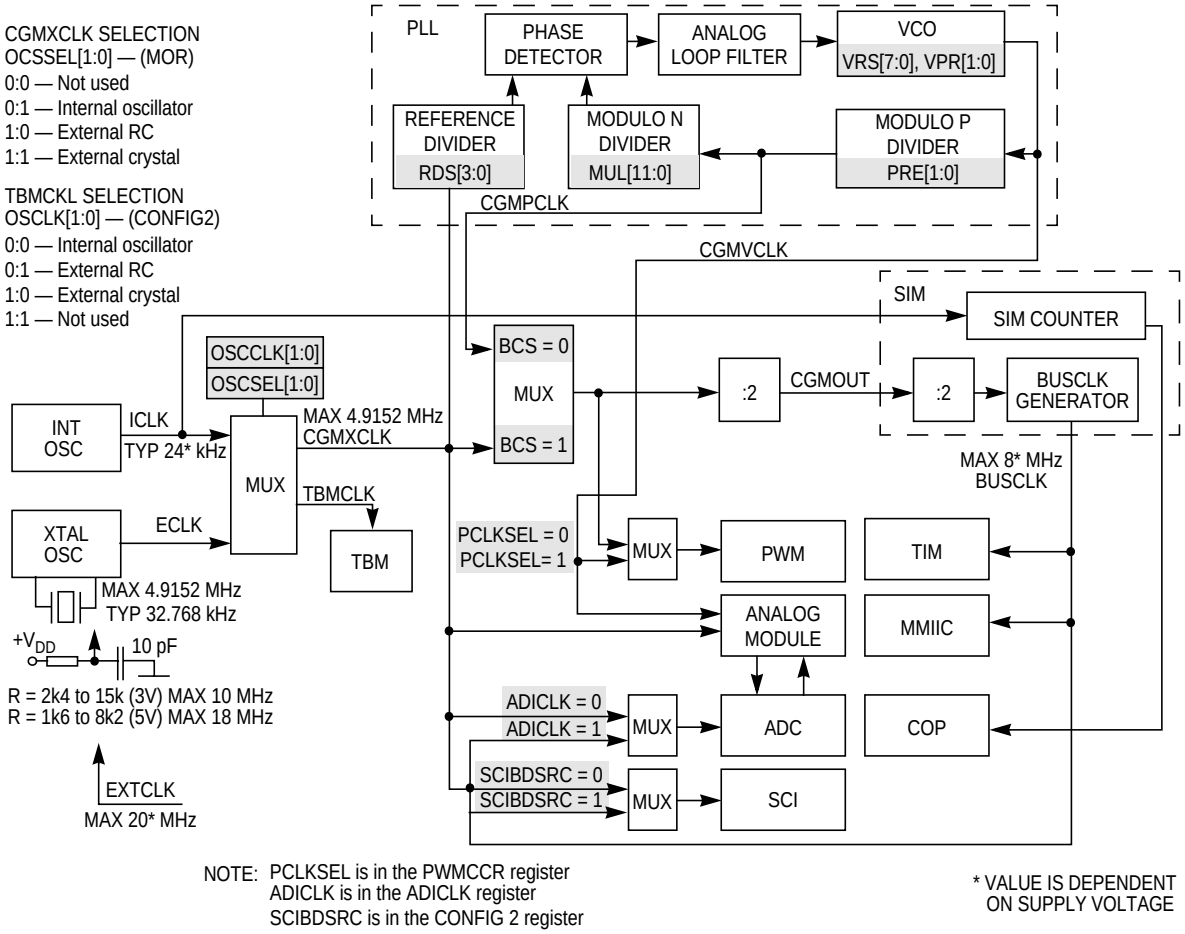

Figure 14. Distribution Clock Signals in the SR Family

The internal RC oscillator is free-running at a typical frequency of 24 kHz. This frequency decreases to 17 kHz with decreasing the supply voltage to 3 V.

The ADC clock should be set to approximately 1 MHz as recommended in the data sheet. Either the CGMXCLK or the BUSCLK can be used as the clock source for the ADC. In this case, the PLL module can be used to generate the internal BUSCLK.

Baud rate for SCI is determined by this formula:

$$\text{baudrate} = \frac{\text{InputCLK}}{64 \times \text{PD} \times \text{BD}}$$

- PD (prescaler divisor) — SCP[1:0] in the SCBR register
- BD (baud rate divisor) — SCR[2:0] in the SCBR register
- The recommended clock frequency for the SCI is 4.9152 MHz

Programming the PLL-3 shows detailed information on programming the PLL and provides several examples.

HC908QT/QY

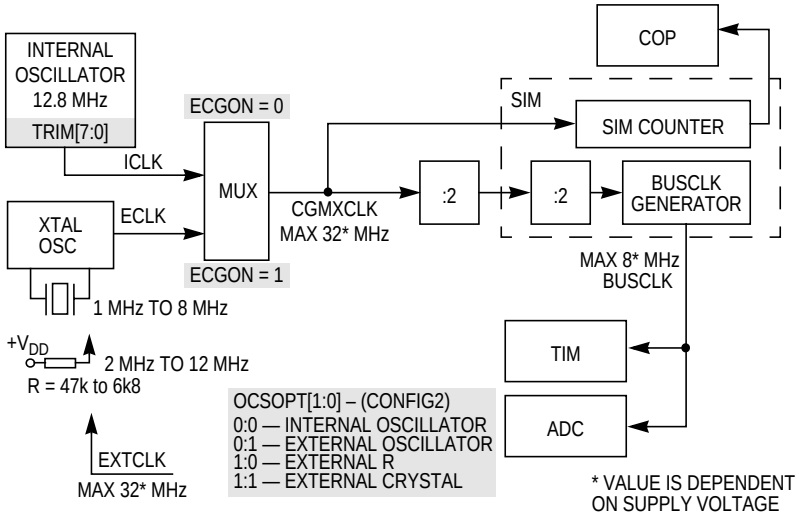

Figure 15. Distribution Clock Signals in the QT/QY Families

The internal oscillator is free-running at a standard frequency of 12.8 MHz. After a RESET function, the TRIM register is set to $80. This provides a bus clock frequency of 3.2 MHz. The internal oscillator runs with a wide tolerance of ±25%, but it is possible to trim this to a tolerance ±5% by setting the OSCTRIM register at address $0038.

The values saved in the FLASH memory at address $FFC0 (for 5.0V supply) and $FFC1 (for 3.0V supply) by the manufacturer makes it possible to set the bus clock to 3.2 MHz ±5%. It is possible to change the bus clock in the full range from 2.4 MHz to 4.0 MHz by writing the appropriate value to the OSCTRIM register. The value of the OSCTRIM register can vary from $00 to $FF. A lower value produces a higher frequency.

Standard Setting

After a RESET, the default setting is the internal oscillator because the clock source is running at a nominal frequency approximately 12.8 MHz. The bus-frequency is 3.2MHz ±25% (default value of the OSCTRIM = $80). For correct functionality of ADC, the ADICLK register (address $003F) must be set to value $40.

Programming the Internal Clock Generator (ICG)

This example uses the GT Family of MCUs.

Internal clock generator (ICG) module — Used to create stable clock source (ICLK) for the MCU without using any external components.

Digitally controlled oscillator (DCO) — Generates the internal clock (ICLK). The clock period of ICLK is dependent on the digital loop filter outputs (DSTG[7:0] and DDIV[3:0]). The long-term precision of the output ICLK is restricted to the approximate range of ±0.202% to ±0.368%.

Modulo N divider — Creates the low-frequency base clock (IBASE) by dividing the internal clock (ICLK) by the ICG multiplier factor N contained in the ICG multiplier register (ICGMR).

Frequency comparator — effectively compares the low-frequency base clock (IBASE) to a nominal frequency f_{nom}. The comparator's outputs are fed to the digital loop filter.

Digital loop filter (DLF) — uses the outputs of the frequency comparator to adjust the internal clock (ICLK) period. DLF generates the DCO control bits (DDIV[3:0]) and the stage control bits (DSTG[7:0]), which are fed to the DCO. The DLF first concatenates the DDIV and DSTG registers and then adds or subtracts a value, depending on the relative error in the low-frequency base clock period.

Standard Setting for the GT Family

The clock generation module is set to the following values after a RESET:

- Internal clock generation with TRIM register = $80
- In the FLASH memory at address $FF80 and $FF81 is the manufacturer's recommended trim value for the 5-V supply and the 3-V supply, respectively.
- Internal bus frequency f_{Bus} = 1.613 MHz (25% under max f_{Bus} for 3-V operation) by the setting the ICGMR register (address $0037) to $15.

Standard Setting for EY, KX, and RF Families

The clock generation module is set to the following values after a RESET:

- Internal clock generation with TRIM register = $80
- Internal bus frequency f_{Bus} = 1.613 MHz (25% under max f_{Bus} for 3-V operation) by the setting the ICGMR register (address $0037) to $15.

Programming the PLL-1

This example uses the AB Family of MCUs.

The following instruction shows how to program the PLL.

1. Choose the desired bus frequency f_{Busdes}
2. Calculate the desired VCO frequency:

$$f_{CLKdes} = 4 \times f_{Busdes}$$

3. Choose the partial PLL reference frequency f_{RCLK}.
4. Select the VCO frequency multiplier, N:

$$N = \text{round}\left(\frac{f_{CLKdes}}{f_{RCLK}}\right)$$

NOTE: *The **round** function means that the real number should be rounded to the nearest whole number.*

5. Calculate and verify the adequacy of the VCO and bus frequencies f_{VCLK} and f_{Bus}:

$$f_{VCLK} = N \times f_{RCLK}$$

$$f_{Bus} = \frac{f_{VCLK}}{4}$$

6. Select the linear VCO multiplier L:

$$L = \text{round}\left(\frac{f_{VCLK}}{f_{nom}}\right)$$ where f_{nom} = 4.9152 MHz.

7. Calculate and verify the adequacy of the VCO programmed center-of-range frequency f_{VRS}.

$$f_{VRS} = (L) \cdot f_{nom}$$

8. Verify and choose N and L by comparing f_{VCLK} to f_{VRS} and $f_{VCLKdes}$. For proper operation, f_{VCLK} must be within the application's tolerance of $f_{VCLKdes}$, and f_{VRS} must be as close as possible to f_{VCLK}.

9. Program the PLL registers (in **Figure 16**) accordingly:
   - In the upper four bits of the PLL programming register (PPG)($001E), program the binary equivalent of N.
   - In the lower four bits of the PLL programming register (PPG), program the binary equivalent of L.

CAUTION: *Exceeding the recommended maximum bus frequency or VCO frequency can cause damage to the MCU.*

To set the desired bus frequency, you must program the content of several PLL registers. They are shown in **Figure 16**.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001C	PLL Control Register Register Low (PCTL)	Read:	PLLIE	PLLF	PLLON	BCS	1	1	1	1
		Write:					R	R	R	R
		Reset:	0	0	1	0	1	1	1	1
$001D	PLL VCO Bandwidth Control Register (PBWC)	Read:	AUTO	LOCK	$\overline{ACQ}$	XLD	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001E	PLL Programming Register (PPG)	Read:	MUL7	MUL6	MUL5	MUL4	VRS7	VRS6	VRS5	VRS4
		Write:								
		Reset:	0	1	1	0	0	1	1	0

N L

= Unimplemented R = Reserved

NOTES:
1. When AUTO = 0, PLLIE is forced clear and is read-only.
2. When AUTO = 0, PLLF and LOCK read as clear.
3. When AUTO = 1, $\overline{ACQ}$ is read-only.
4. When PLLON = 0 or VRS7:VRS0 = $0, BCS is forced clear and is read-only.
5. When PLLON = 1, the PLL programming register is read-only.
6. When BCS = 1, PLLON is forced set and is read-only.

Figure 16. PLL Registers for the HC908AB/AS/AZ/MR Families

Standard Settings

MCU default after reset function:

- External crystal element 4.9152 MHz
- Internal bus frequency of 7.3728 MHz
- For ADC, it is recommended setting ADCLK register ($003A) to $70
- For SCI, baud rate scale is from 600 to 76.800 bps (for setting: PD = 1 and BD is set from 1 to 128) in the SCBR register ($0019)
  - For [SCBR] = $00 baud rate is 76.8 kbps
  - For [SCBR] = $02 baud rate is 19.2 kbps
  - For [SCBR] = $03 baud rate is 9.6 kbps

Programming the PLL-2

This example uses the GZ Family of MCUs.

The following instruction shows how to program the PLL.

1. Choose the desired bus frequency f_{Busdes}
2. Calculate the desired VCO frequency:

$$'CLKdes = 4 \times f_{Busdes}$$

3. Choose the partial PLL reference frequency f_{RCLK}. Typically the reference crystal is 1 to 8 MHz.
4. Select the VCO frequency multiplier, N:

$$N = round\left(\frac{f_{VCLKdes}}{f_{RCLK}}\right)$$

NOTE: *The **round** function means that the real number should be rounded to the nearest whole number.*

5. Calculate and verify the adequacy of the VCO and bus frequencies f_{VCLK} and f_{Bus}:

$$f_{VCLK} = N \times f_{RCLK}$$

$$f_{Bus} = \frac{f_{VCLK}}{4}$$

6. Select the VCO's power-to-two range multiplier E, according to **Table 1**:

Table 1. VCO Range Multiplier

Frequency range	E
$0 < f_{VCLK} < 8$ MHz	0
$8 \text{ MHz} \leq f_{VCLK} < 16$ MHz	1
$16 \text{ MHz} \leq f_{VCLK} < 32$ MHz	2

NOTE: *Do not program E to a value of 3.*

7. Select a VCO linear range of multiplier L, where f_{nom} =71.4 kHz

$$L = \text{round}\left(\frac{f_{VCLK}}{2^E \times f_{nom}}\right)$$

8. Calculate and verify the adequacy of the VCO programmed center-of-range frequency f_{VRS}. The center-of-range frequency is the midpoint between the minimum and maximum frequencies attainable by the PLL.

$$f_{VRS} = (L \times 2^E) f_{nom}$$

for proper operation:

$$\left|f_{VRS} - f_{VCLK}\right| \leq \frac{f_{nom} \times 2^E}{2}$$

9. Verify and choose N, E, and L by comparing f_{VCLK} to f_{VRS} and $f_{VCLKdes}$. For proper operation, f_{VCLK} must be within the application's tolerance of $f_{VCLKdes}$, and f_{VRS} must be as close as possible to f_{VCLK}.
10. Program the PLL registers accordingly:
    - In the VPR bits of the PLL control register (PCTL), program the binary equivalent of E.
    - In the PLL multiplier select register low (PMSL) and the PLL multiplier select register high (PMSH), program the binary equivalent of N.
    - In the PLL VCO range select register (PMRS), program the binary equivalent of L.

NOTE: *Exceeding the recommended maximum bus frequency of VCO frequency can cause damage to the MCU.*

Table 2. Example PLL Register Values

f_{BUS} [MHz]	f_{RCLK} [MHz]	N [PMSH:L]	E [PCTL]	L [PMRS]
0.500	1	$002	$A0	$1B
1.25	1	$005	$A0	$45
2.0	1	$008	$A0	$70
2.5	1	$00A	$A1	$45
3.0	1	$00C	$A1	$53
4.0	1	$010	$A1	$70
5.0	1	$014	$A2	$46
7.0	1	$01C	$A2	$62
8.0	1	$020	$A2	$70

In the programming of the PLL registers there are two exceptions:

- A 0 value for N is interpreted exactly the same as a value of 1.
- A 0 value for L disables the PLL and prevents its selection as the source for the base clock.

Programming the PLL-3

This example uses the GP Family of MCUs.

The following instruction shows how to program the PLL.

1. Choose the desired bus frequency f_{Busdes}.
2. Calculate the desired VCO frequency:

$$f_{VCLKdes} = 4 \times f_{Busdes}$$

3. Choose the practical PLL (crystal) reference frequency f_{RCLK}, and the reference clock divider R. Typically the reference crystal is 32.768 kHz and R = 1.

Frequency errors to the PLL are corrected at the rate of f_{RCLK}/R. For stability and lock time reduction this rate must be as fast as possible. The VCO frequency must be an integer multiple of this rate.

The relationship between the VCO frequency and the reference frequency is:

$$f_{VCLK} = \frac{2^P N}{R}(f_{RCLK})$$

where P and N are integers.

4. Select a VCO frequency multiplier N:

$$N = \text{round}\left(\frac{R \times f_{VCLKdes}}{f_{RCLK}}\right)$$

Reduce N/R to the lowest possible R.

5. If $N < N_{max}$, use P = 0. If $N > N_{max}$, choose P using this table

Table 3. Relationship Between N and P

Current N value	P
$0 < N \leq N_{max}$	0
$N_{max} < N \leq N_{max} \times 2$	1
$N_{max} \times 2 < N \leq N_{max} \times 4$	2

Then re-calculate N:

$$N = \text{round}\left(\frac{R \times f_{VCLKdes}}{f_{RCLK} \times 2^P}\right)$$

6. Calculate and verify the adequacy of the VCO and bus frequencies f_{VCLK} and f_{Bus}

$$f_{VCLK} = (2^P \times N/R) \times f_{RCLK}$$

$$f_{BUS} = \frac{f_{VCLK}}{2^P \times 4}$$

7. Select the VCO's power-to-two range multiplier E, according to **Table 4**.

Table 4. VCO Range Multiplier

Frequency range	E
$0 < f_{VCLK} < 9{,}830400$	0
$9{,}830400 \leq f_{VCLK} < 19{,}660800$	1
$19{,}660800 \leq f_{VCLK} < 39{,}321600$	2

NOTE: *Do not program E to a value of 3.*

8. Select a VCO linear range of multiplier L, where f_{nom} = 38.4 kHz.

$$L = \text{round}\left(\frac{f_{VCLK}}{2^E \times f_{nom}}\right)$$

9. Calculate and verify the adequacy of the VCO programmed center-of-range frequency f_{VRS}. The center-of-range frequency is the midpoint between the minimum and maximum frequencies attainable by the PLL.

$$f_{VRS} = (L \times 2^E) f_{nom}$$

for proper operation:

$$\left|f_{VRS} - f_{VCLK}\right| \leq \frac{f_{nom} \times 2^E}{2}$$

10. Verify and choose P, R, N, E and L, by comparing f_{VCLK} to f_{VRS} and $f_{VCLKdes}$. For proper operation, f_{VCLK} must be within the application's tolerance of $f_{VCLKdes}$, and f_{VRS} must be as close as possible to f_{VCLK}.

11. Program the PLL registers (in **Figure 17**) accordingly:
    - In the PRE bits of the PLL control register (PCTL), program the binary equivalent of P.
    - In the VPR bits of the PLL control register (PCTL), program the binary equivalent of E.
    - In the PLL multiplier select register low (PMSL) and the PLL multiplier select register high (PMSH), program the binary equivalent of N.
    - In the PLL VCO range select register (PMRS), program the binary equivalent of L.
    - In the PLL reference divider select register (PMDS), program the binary coded equivalent of R.

NOTE: *Exceeding the recommended maximum bus frequency of VCO frequency can cause damage to the MCU.*

Table 5. Example PLL Register Values

f_{Bus} [MHz]	f_{RCLK} [kHz]	R [PMDS]	N [PMSH:L]	P,E [PCTL]	L [PMRS]
8.192	32.768	$1	$3E8	$A2	$D5
8	32.768	$1	$3D1	$A2	$D0
4	32.768	$1	$1E9	$A1	$D1
2	32.768	$1	$F4	$A0	$D0
1	32.768	$1	$7A	$A0	$68
7.3728	32.768	$1	$384	$A2	$C0
4.9152	32.768	$1	$258	$A2	$80
2.4576	32.768	$1	$12C	$A1	$80

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	PLL Control Register (PTCL)	Read:	PLLIE	PLLF	PLLON	BCS	PRE1	PRE0	VPR1	VPR0
		Write:								
		Reset:	0	0	1	0	0	0	0	0
$0037	PLL Bandwidth Control Register (PBWC)	Read:	AUTO	LOCK	$\overline{ACQ}$	0	0	0	0	R
		Write:								
		Reset:	0	0	0	0	0	0	0	
$0038	PLL Multiplier Select Register High (PMSH)	Read:	0	0	0	0	MUL11	MUL10	MUL9	MUL8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0039	PLL Multiplier Select Register Low (PMSL)	Read:	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
$003A	PLL VCO Range Select Register (PMRS)	Read:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
		Write:								
		Reset:	0	1	0	0	0	0	0	0
$003B	PLL Reference Divider Select Register (PMDS)	Read:	0	0	0	0	RDS3	RDS2	RDS1	RDS0
		Write:								
		Reset:	0	0	0	0	0	0	0	1

= Unimplemented R = Reserved

NOTES:
1. When AUTO = 0, PLLIE is forced clear and is read-only.
2. When AUTO = 0, PLLF and LOCK read as clear.
3. When AUTO = 1, $\overline{ACQ}$ is read-only.
4. When PLLON = 0 or VRS7:VRS0 = $0, BCS is forced clear and is read-only.
5. When PLLON = 1, the PLL programming register is read-only.
6. When BCS = 1, PLLON is forced set and is read-only.

Figure 17. PLL Registers of the HC908GR/GP/LJ/SR Families

Standard Setting: 5.0 V Supply

If a crystal element of frequency 32.768 kHz is in use, desired bus frequency is 8 MHz, it is necessary to set these values in the respective registers:

- $A2 to address $0036 (PCTL register) — P, E
- $80 to address $0037 (PBWC register) — Auto BW
- $F4 to address $0039 (PMSL register) — N
- $D0 to address $003A (PMRS register) — L
- $70 to address $003E (ADCLK register)

Standard Setting: 3.0 V Supply

If a crystal element of frequency 32.768 kHz is in use, desired bus frequency is 4 MHz, it is necessary to set these values in the respective registers:

- $A1 to address $0036 (PCTL register) — P,E;
- $80 to address $0037 (PBWC register) — Auto BW
- $7A to address $0039 (PMSL register) — N
- $D0 to address $003A (PMRS register) — L
- $50 to address $003E (ADCLK register)

Programming the PLL-4

This example uses the LD Family of MCUs.

In this family, the PLL is used to generate output frequency CGMVCLK in integer multiples of the crystal reference OSCXCLK. The base selector circuit (the software controlled circuit) selects either CGMVCLK or OSCXCLK as the clock source DCLK1 for the sync processor. The sync processor derives other display clocks from DCLK1.

The basic setting of relevant PLL registers is shown in **Table 6**.

Table 6. PLL Registers Setting

Register Settings			Output Pin Frequency			DE Video Mode
HVOCR [1:0]	MUL [7:4]	VRS [7:4]	HOUT	VOUT	DCLK1	
00	3	3	31.45 kHz	59.91 Hz	24 MHz	640 x 480
01	5	3	37.87 kHz	60.31 Hz	40 MHz	800 x 600
10	8	6	48.37 kHz	60.31 Hz	64 MHz	1024 x 768
11	9	9	64.32 kHz	60.00 Hz	108 MHz	1280 x1024

HVOCR[1:0] — These two bits determine the prescaler of the PLL reference clock in the CGM module. When HVOCR[1:0] = 11, the prescaler is 2; for other values the prescaler is 3.

The relevant PLL registers are shown in **Figure 18**.

LD Family default settings after a reset:

- External crystal element 24 MHz
- Internal bus frequency of 6.0 MHz
- Sync processor use the CGMXCLK (frequency of external crystal element) as a reference to generate sync composition (video mode is 640 x 480).

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0038	PLL Control Register (PCTL)	Read:	PLLIE	PLLF	PLLON	BCS	1	1	1	1
		Write:								
		Reset:	0	0	1	0	1	1	1	1
$0039	PLL Bandwidth Control Register (PBWC)	Read:	AUTO	LOCK	$\overline{ACQ}$	XLD	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$003A	PLL Programming Register (PPG)	Read:	MUL7	MUL6	MUL5	MUL4	VRS7	VRS6	VRS5	VRS4
		Write:								
		Reset:	0	1	1	0	0	1	1	0
					N			L		
$003F	H&V Sync Output Control Register (HVOCR)	Read:				DCLKPH1	DCLKPH0	R	HVOCR1	HVOCR0
		Write:								
		Reset:				0	0		0	0

= Unimplemented R = Reserved

NOTES:
1. When AUTO = 0, PLLIE is forced clear and is read-only.
2. When AUTO = 0, PLLF and LOCK read as clear.
3. When AUTO = 1, $\overline{ACQ}$ is read-only.
4. When PLLON = 0 or VRS7:VRS0 = $0, BCS is forced clear and is read-only.
5. When PLLON = 1, the PLL programming register is read-only.
6. When BCS = 1, PLLON is forced set and is read-only.

Figure 18. PLL Registers of the HC908LD Family

Table 7. HC908 Clock Selector

Family	Supply Voltage (V)	BUSCLK Min (Hz)	BUSCLK Max (Hz)	Crystal Min (Hz)	Crystal Max (Hz)	Crystal Typ (Hz)	Ext Clock Min (Hz)	Ext Clock Max (Hz)	VCO/DCO Min (Hz)	VCO/DCO Max (Hz)	Int/RC Osc. Min (Hz)	Int/RC Osc. Max (Hz)	Int/RC Osc. Typ (Hz)
AB	5	DC	8 M	1 M	8,4 M	4,9152 M	DC	33,6 M	4,9152 M	32 M	—	—	—
AS/AZ	5	—	8,4 M	1 M	8 M	4,9152 M	—	8 M	4,9152 M	32,8 M	—	—	—
MR/MP	5	—	8,2 M	1 M	8 M	4,9152 M	DC	32,8 M	4,9152 M	32,8 M	—	—	—
GZ	5	—	8 M	1 M	8 M	4 M	DC	32 M	—	32 M	—	—	—
	3	—	4 M	1 M	8 M	4 M	DC	16 M	—	16 M	—	—	—
GP/GR	5	—	8,2 M	32 k	100 k	32,768 k	DC	32,8 M	—	39 M	—	—	—
	3	—	4,1 M	32 k	100 k	32,768 k	DC	16,4 M	—	—	—	—	—
LD	3	—	6 M	—	—	24 M	—	24 M	24 M	108 M	—	—	—
BD	5	—	6 M	—	24 M	24 M	DC	24 M	—	—	—	—	—
JB	5	—	3 M	1 M	6 M	6 M	DC	6 M	—	—	—	—	—
KL	5	—	1,5 M	1 M	8 M	—	DC	32 M	—	—	—	—	—
EY	5	—	8 M	32 k	8 M	32,768 k	DC	16 M	—	32 M	–25%	25%	307,2 k
GT	5	—	8 M	32 k	10 M	32,768 k	60 k	32 M	—	32 M	–25%	25%	307,2 k
	3	—	4 M	32 k	10 M	32,768 k	60 k	16 MS	—	16 M	–25%	25%	307,2 k
KX	5	—	8 M	32 k	8 M	—	DC	32 M	—	32 M	–25%	25%	307,2 k
	3	—	4 M	32 k	8 M	—	DC	16 M	—	16 M	–25%	25%	307,2 k
RF/RK	3	32 k	4 M	32 k	8 M	—	128 k	16 M	—	—	–25%	25%	307,2 k
	2	32 k	2 M	32 k	8 M	—	128 k	8 M	—	—	–25%	25%	307,2 k
LJ	5	—	8 M	—	4,9152 M	32,768 k	DC	20 M	38,4 k	40 M	46 k	48 k	47 k
	3	—	4 M	—	4,9152 M	32,768 k	DC	16 M	38,4 k	40 M	42,8 k	44 k	43,4 k
SR	5	—	8 M	—	4,9152 M	32,768 k	DC	20 M	—	—	19,2 k	28,8 k	24 k
	3	—	4 M	—	4,9152 M	32,768 k	DC	16 M	—	—	13,8 k	20,6 k	17,2 k
JL/J k	5	—	8 M	—	32 M	10 M	DC	32 M	—	—	2 M	12 M	10 M
	3	—	4 M	—	16 M	8 M	DC	16 M	—	—	2 M	12 M	8 M
QT/QY	5	—	8 M	1 M	32 M	—	DC	32 M	—	—	2 M	12 M	12,8 M*
	3	—	4 M	1 M	16 M	—	DC	16 M	—	—	2 M	12 M	12,8 M*

Note: * frequency of the internal oscillator

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