Application Note

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Interfacing to the HCS12 ATD Module

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Introduction

Many of the HCS12 family of 16-bit microcontrollers include support for Analog-to-Digital conversion.

The HCS12 ATD converter is modular in design. At the time of publishing, 8-channel and 16-channel implementations exist.

The ATD is available on devices with automotive, industrial and consumer temperature ranges. All of the examples in this document are based on VDDA = 5V but the module is also used on devices that can operate at 3.3V.

The HCS12 Analog-To-Digital converter (ATD) module is highly autonomous with an array of flexible conversion sequences. It provides all of the timing and controls for both sample and conversion periods.

Programmable conversion sequences control

- at which analog source to start conversion
- how many conversions to perform
- whether conversions should be on the same or multiple input channels

Any conversion sequence can be selected to continuously repeat without MCU overhead.

Sequences can be started by a write to a single register or by a valid signal on an external trigger input (to synchronize the ATD conversion process with external events).

Conversions in each sequence can be configured for sample time, resolution and data format of the results.

The Digital-to-Analog Converter (DAC) is a unipolar, successive-approximation converter selectable for 8- or 10-bit resolution and accurate to ± 1 Least

Significant Bit (LSB). Typical total unadjusted error is ± 2 counts (VDDA = 5V). Monotonicity is guaranteed for both 8- and 10-bit conversions.

With a 2MHz ATD module clock, an 8-bit single sample can be performed in 6μs or a 10-bit single conversion in 7μs (including sample times).

A charge distribution technique is used, removing the need for external sample and hold circuits.

Unused analog inputs can be used as digital inputs. Each port pin has an associated digital input buffer that can be enabled on a pin-by-pin basis. On some devices, digital output functionality is also supported.

This document sets out to provide guidelines for interfacing hardware to the HCS12 ATD module with a detailed look at avoiding possible inaccuracies that may be introduced. For a more detailed description of the HCS12 ATD functionality, refer to Freescale Application Note AN2428, “An Overview of the HCS12 ATD Module”.

All specification parameters used in this document should be validated against the current specification electrical parameters for any target device(s).

Figure 1 shows a functional block diagram of the ADC module. The module is made up of an analog subsystem consisting of:

- An input multiplexer
- A sample amplifier
- A sample capacitor
- A resistor-capacitor digital-to-analog converter (RC DAC) array
- A high-gain comparator

and a digital control subsystem containing registers and logic to control the conversion process and conversion sequences.

Figure 2 shows a model of an analog input pin, including the external signal, source impedance (R_s) and filter capacitor (C_f).

Figure 3 shows the timing of a typical conversion sequence.

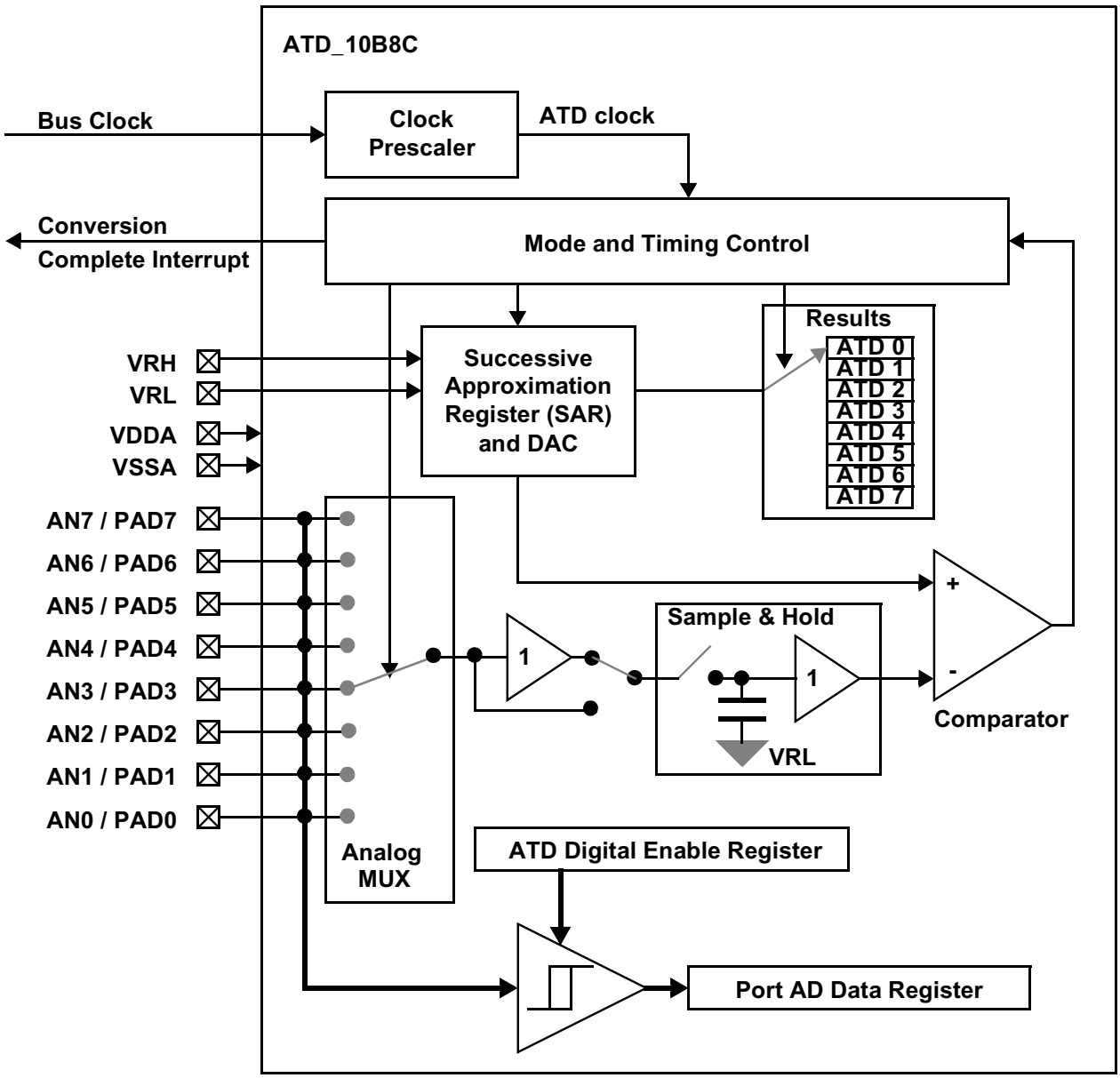
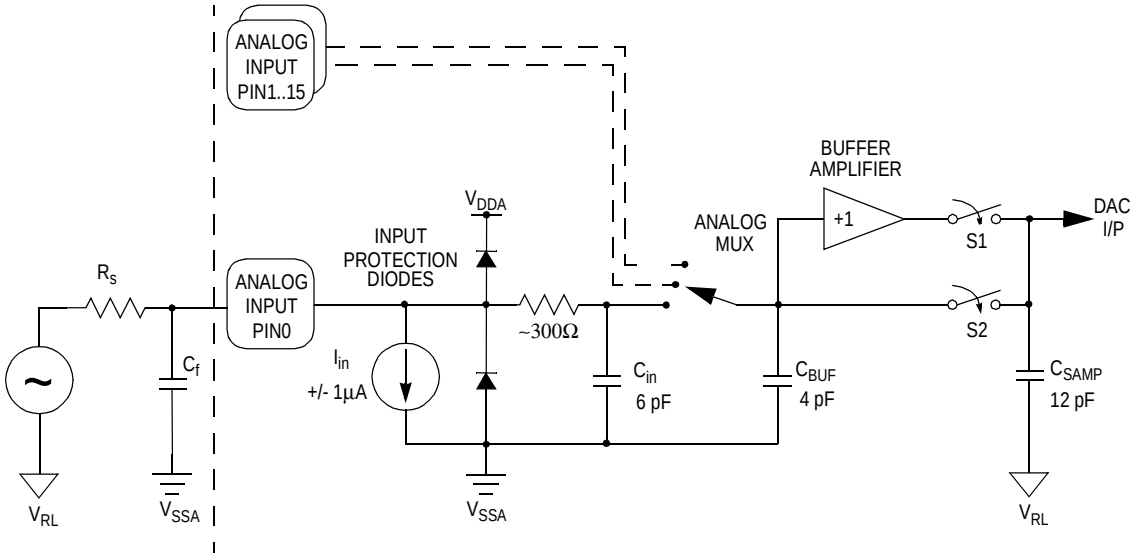


Figure 1. ATD_10B8C Block Diagram



Switch 1 is closed only for the first, fixed 2 cycles of the sample period.

Switch 2 is closed only for the final, programmable 2/4/8/16 cycles of the sample period.

Figure 2. Electrical Model of an A/D Input Pin

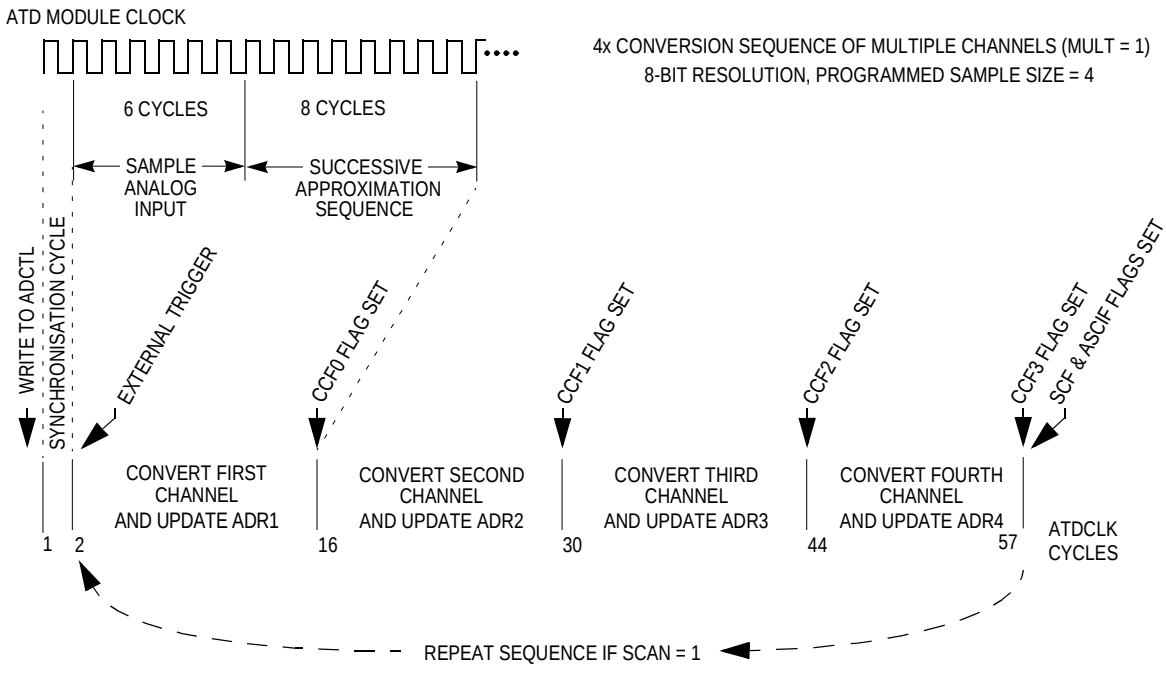


Figure 3. Conversion Sequence Timing Example

Analog Power Supplies and Voltage References

VDDA and VSSA are the power supply and ground input pins for the analog to digital converter and also the voltage reference for the on-chip voltage regulator. Having separate power supply pins allows the supply voltage to the ATD and the regulator reference voltage to be bypassed independently of the MCU core. They are also the supply pins for any digital I/O ports associated with the ATD inputs. VDDA and VDDS should always be connected to an appropriate supply on the PCB irrespective of whether the ATD module is being used in an application.

VRH and VRL are the supplies for the analog conversion reference. If an application does not perform analog conversions, tie VRH to VDDA and VRL to VSSA. On lower pin count devices, VRL may be connected internally.

As the ATD's comparator and RC DAC array are referenced to VRL, analog conversion results are generated with reference to VRL.

The following constraint must be met to obtain full-scale, full range results:

$$VSSA \leq VRL \leq VIN \leq VRH \leq VDDA.$$

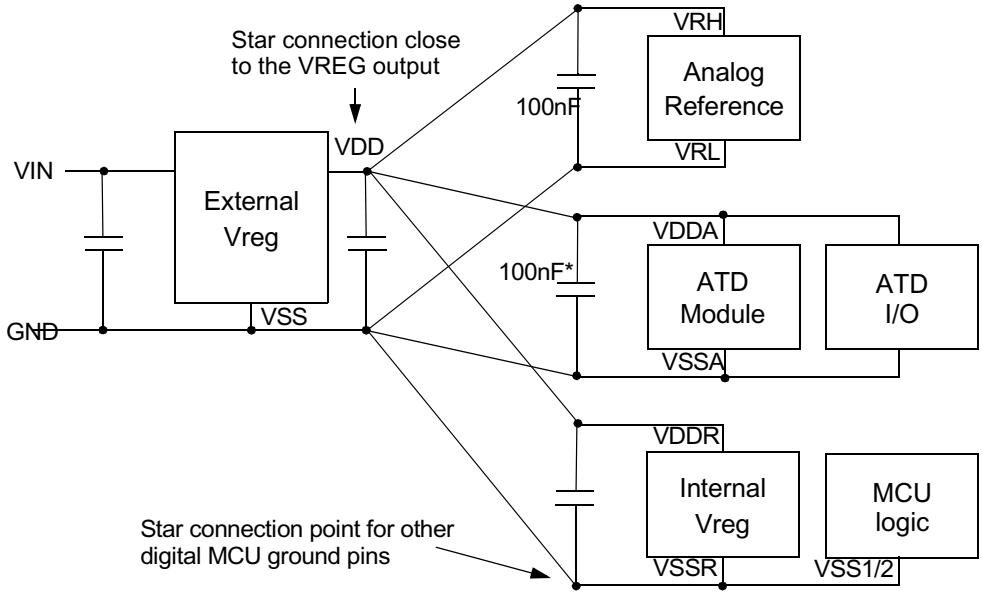
If the input level goes outside of this range it will effectively be clipped.

VRH should always be ≤VDDA to maintain conversion accuracy.

The A/D converter's accuracy is limited by the accuracy of the reference potentials. Noise on the reference potentials will result in noise on the digital output data stream; the reference potential lines do not reject reference noise. This is a key area of hardware implementation; no matter what error you get on each channel due to conversion timing or external input circuitry, any disturbances on the reference will be directly reflected in the conversion results.

The reference potential pins must have a low AC impedance path back to the source, although for the most part the load it presents is fairly static. A large decoupling capacitor (100nF or larger) will suffice in most cases. Avoid tracking the reference potential through digital supply planes and do not connect external digital pull devices to VRH or VRL. In extreme cases, where high frequency system noise is present, adding low ESR series inductors and/or ferrite beads to the VRH line may help reduce noise from being coupled onto the conversion reference. Series resistance should be avoided since each ATD reference draws ~375μA from the reference supply (VRH=5V). A potential drop across any series impedance will result in gain and offset errors in the digital data output stream unless the reference potential is sensed at the reference input pin and any potential drop compensated for.

Where possible, avoid connecting external pull-devices or logic to VDDA/VSSA tracks.



* Where ATD I/O are configured as outputs, increase from 100nF as appropriate.

Figure 4. Power supply layout guidelines

General Purpose Digital Port Operation

A number of HCS12 ATD implementations, such as the D, A and B families, share the analog inputs with digital input buffers only. On other implementations, such as the C and E families, the analog input pins support both digital input and output functionality. Considerations for each implementation are discussed below.

Input Only Implementations

For each 8 analog input channels there is a digital, 8-bit, input port associated with the ATD module. These ports are accessed through Port Data Registers (PORTADx) in the ATD register map. Since the port pins are input only, no data direction register is available for these ports.

The input channel pins can be used to read analog or digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply input data buffers that can be accessed through the digital port registers in the ATD module.

A Digital Input Enable (ATDDIEN) register allows each digital input buffer to be enabled on a per pin basis. It is not recommended to have the digital buffer

enabled on a pin while simultaneously using it as an analog port. If a digital input buffer is enabled while the pin is simultaneously being used as an analog port, the digital input buffer may be driven into the linear region with a corresponding increase in current consumption. Internal pull devices, if enabled, will conflict with the analog source.

External digital input circuits should meet the Current Injection requirements.

As the ATD digital inputs can be enabled on a pin-by-pin basis, there is no logical restriction on the allocation of digital and analog input pins on a port. Care should be taken when mixing fast switching digital signals with analog signals to avoid ‘crosstalk’ on the pcb from introducing error into the analog signal.

Care should be taken when tracking digital signals close to analog signals (including the reference inputs); it is recommended to keep analog and digital inputs separated. Where possible use alternative IO ports for digital signals and/or add series filtering to slow down the digital edges and reduce switching noise.

Input/Output Implementations

For each analog module there is a digital IO port associated. These ports are accessed through Port Data Registers (PORTADx) in the ATD register map and a set of IO control registers in the Port Integration Module (PIM).

Digital port control registers (located in the ATD)

- ATD Port Data Register (PORTADx)
- ATD Port Digital Input Enable Register (ATDDIENx)

Associated Port AD control registers (located in the PIM)

- Port AD IO Register (PTAD)
- Port AD Input Register (PTIAD)
- Port AD Data Direction Register (DDRAD)

The Port AD pins can be used to read analog signals or read / write digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply input data buffers that can be accessed through the digital port registers. As digital outputs they drive to VSSA (‘0’) or VDDA (‘1’). Overall digital functionality is device dependent, for instance the E-family PortAD has wake-up interrupt capability.

Bits in the Digital Input Enable (ATDDIEN) register(s) allow each digital input buffer to be enabled on a per pin basis. It is not recommended to have the digital buffers enabled on a pin while simultaneously using it as an analog input. If a digital input buffer is enabled while the pin is simultaneously being used as an analog input the digital input buffer may be driven into the linear region with a corresponding increase in current consumption. Internal pull devices or output drivers, if enabled, will conflict with the analog source.

The Data Direction Register (DDRAD) configures port pins as either input or output. If a data direction bit is 0 (input), the value read in PORTAD, PTAD & PTIAD depends on the corresponding ATDDIEN bit. If the ATDDIEN bit is enabled as input, the value read on PTAD will be the value on the pin, otherwise it will always be 1. If a data direction bit is 1 (output), the value on the pin will be the value written to PTAD.

For digital inputs enabled in an ATDDIEN register, reading of the PTIAD register in the PIM reads the actual level on the appropriate pin and is equivalent to reading the PORTAD register in the ATD module.

External digital input circuits should meet the device Current Injection requirements.

As the ATD digital functionality can be enabled on a pin-by-pin basis there is nothing to prevent interleaving digital input, digital output and analog input pins, however, care should be taken mixing fast switching digital signals with analog signals to avoid ‘crosstalk’ on the pcb introducing error in to the analog signal.

Care should be taken when tracking digital signals close to analog signals (including the reference inputs); keep analog and digital signal separated. Wherever possible, use alternative IO ports for digital signals.

Where unused analog port pins are required for digital signals, if possible, constrain the digital functionality to inputs and use alternative IO ports for digital output.

For digital inputs on Port AD, consider adding series filtering to slow down the digital edges to reduce switching noise.

When using the digital outputs on Port AD, extra care should be taken with decoupling VDDA/VSSA as ripple on this supply from switching/loading these output pins may degrade the ATD performance. Avoid switching any of these outputs during analog conversion sequences.

Analog Input Allocation

An analysis of the ATD sources being converted can help utilise the flexibility of the ATD control and conversion structure. Sources with similar requirements can then be grouped onto adjacent ATD inputs and the ATD configured appropriately to use the most effective conversion sequences.

Evaluation of key information on each analog source can be evaluated:

- Period of conversion (how often is the conversion required)?
- Is continuous scanning required?
- Source impedance? – this can affect the required sample time or ATD clock frequency

- Required conversion resolution?
- Is absolute accuracy critical?
- Is the conversion time critical?
- Is the sample time critical?
- What is the signal voltage range (to minimise possible ‘crosstalk’ and charge sharing effects).

The input multiplexer ‘wraps around’ after converting the last channel on the ATD to select channel AD0. When grouping similar signals for conversion onto adjacent inputs it can be useful to consider the pin connected to the last input channel as adjacent to that connected to AD0. See the Input Channel Wrap Around section in AN2428.

As explained in the previous section, avoid mixing digital and analog input pins wherever possible.

Sample and Hold Stage

A Sample-and-Hold (S/H) stage accepts analog signals from the input multiplexer and stores them as charge on the sample capacitor. This charge redistribution method eliminates the need for external Sample-and-Hold circuitry. The analog sample phase can be seen clearly in **Figure 3**.

The sample process has two stages:

1. Initially a sample amplifier (of unity gain) is used to buffer the input analog signal for two cycles to charge the sample capacitor almost to the input potential. This stage prevents charging and discharging of the sample capacitor via the source impedance
2. The sample buffer is then disconnected and the input signal is connected directly to the storage node for a programmable 2, 4, 8 or 16 cycles

The **Source Impedence** and **Charge Sharing** sections examine the implications of the sample and hold implementation in detail.

Current Injection

The internal structure of the analog input pins is similar to the digital IO pins. The internal protection clamping diodes are present (See **Figure 2**) and the general current injection limits for IO pins specified in the device user guide should be observed, i.e. the current at a pin should be limited to maximum 25 mA transient (I_{ICP}), 2.5mA steady state (I_{ICS}). The source impedance (R_S) that meets this limitation will depend on the total system.

For example, suppose the worst-case scenario for a particular system results in an analog source accidentally shorting to –12V. The inherent internal diodes to V_{SS} will clamp the voltage at the pin to about –0.7V. This clamp voltage means 11.3V dropped across a series-limiting resistance must cause a maximum current of 2.5mA to flow, which calculates to an Rs > 4.5KΩ. Some guard band should be allowed for tolerances on the clamped voltage, the source voltages, the resistor, etc.

There are additional considerations of the effects of current injection for the analog channels

- *where current is injected into the channel being converted.*
  The conversion will generate a maximum conversion value for analog inputs greater than V_{RH} and $000 for values less than V_{RL}.
- *where current is injected into pins in the neighborhood of the channel being converted (either into an adjacent pin or an adjacent ATD channel).*

  A portion of the injected current will be picked up by the channel being converted. This additional current impacts the accuracy of the conversion depending on the converting channel's source resistance. $V_{ERR,}$ the additional input voltage error on the converted channel is defined in the electrical parameters section of the device data sheet.

Filter Capacitor, C_f

Each analog input should have a capacitor with good high frequency characteristics between the input pin and V_{SSA} (shown as C_f in **Figure 2**).

This analog source capacitor performs two functions:

- It provides a low AC impedance at the pins to shunt unwanted high frequency components of the input signal away from the A/D input.
- It smooths out the effect of charge sharing when the input is switched onto buffer amplifier and then onto the sample capacitor.

This capacitor will help prevent errors due to system 'noise', but it is important to size it properly for the way the A/D converter is being used in a particular system.

Factors affecting the size of these capacitors are:

- Source impedance of the analog signal
- Rate of change of the analog signal
- Electrical model of the A/D inputs
- Frequency of A/D conversion requests to the particular channel

During the initial sample period (see **Figure 3**), the sample buffer input capacitance is connected to the input for two ATD clock cycles. The sample capacitor (which will already be charged almost to the input signal level by the buffer amplifier) is then connected to the input for the programmable sample time. Charge sharing between the external and the internal capacitances can cause a small voltage drop. The size of the external source capacitance will be application dependent; a good guideline for minimising the effect of this charge sharing is to keep the external capacitor greater than C_f as defined in the Electrical Characteristics section of the specific Device User Guide.

For example, on the MC9S12Dx64:

For a maximum 10-bit sampling error of the input voltage ≤ 1LSB, the external filter capacitor (C_f) should be ≥ 1024 * (C_{INS}-C_{INN}) or ≥ 12 nF.

For an 8-bit conversion, 1LSB is 4 times larger so the minimum source capacitance for ≤ 1LSB error will be 256 * (C_{INS}–C_{INN}) or ≥ 3nF.

Source Impedance, R_s

The source impedance of the signal driver, must also be considered when choosing the capacitor size (shown as Rs in **Figure 2**). Optimising the source impedance can be a compromise:

- External source impedance along with the input capacitor will create a low pass anti-aliasing filter which can be used to attenuate unwanted frequency components and noise. Higher source impedance can result in rolling off higher frequency components of interest in input signals.
- Higher source impedance reduces current injection when the input exceeds the rail voltages.
- Lower source impedance avoids and reduces the error generated by input leakage (I_{in}). The maximum external source impedance of an analog signal is limited by the leakage into the pin (see **Figure 2**). On newer HCS12 devices the worst-case input leakage is specified as ± 1μA and this is the value guaranteed by Motorola's test procedure. The typical value is in fact much lower and decreases significantly with temperature. For applications running at lower temperatures, it may be possible to use a higher value of R_s without degrading accuracy.

A good guideline for minimising the effect of input leakage is described in the data sheets. When VREF = VRH – VRL = 5.12V, one 8 bit count = 20mV and one 10 bit count = 5mV

- For a maximum 10-bit error of <1/2LSB, R_s should be ≤2.5KΩ (=2.5mV/1μA)
- For a maximum 8-bit error of <1/2LSB, R_s should be ≤10KΩ (=10mV/1μA)

Larger R_s values can be used with an associated reduction in accuracy. It may be that a particular signal in an application only requires to be converted to 6-bit accuracy (for example). In this case, the source impedance can be up to 40KΩ (= 40mV / 1µA).

Where the source impedance of a signal is too high to achieve the desired accuracy, it may be necessary to buffer the signal externally with a low output impedance buffer.

Two of the most common application errors with this type of A/D are either too much source impedance, resulting in higher-than-expected errors, or too little source impedance, resulting in permanent (**Current Injection**) damage to A/D inputs.

A closer look at the effects of charge sharing

For most applications, the above component guidelines will be satisfactory. However, if the input to the convertor changes significantly between successive samples in a sequence of conversions, it can be useful to understand a secondary charge-share mechanism that can have a minor effect on the sample accuracy. This effect is primarily of consideration in multiple-channel, continuous-scan conversion sequences, where two adjacent channels are connected to grossly different analog levels.

This analysis is based on the ATD input model shown in **Figure 2**. The model contains all of the key components but does not take into account any tolerances for on-chip capacitances, parasitic capacitances or signal path impedances. For this reason, results from the following calculations should only be considered as typical values.

The converter input capacitance (C_{BUF}) is shared by all conversions. On the HCS12 this capacitance is only 4pF due to the sample buffer charging and discharging the hold capacitor rather than this being done via the input pin. This results in the initial voltage on C_{BUF}, just before a sample period, being approximately equal to the voltage on the last channel converted.

Consider what happens when the following conversion sequence occurs with a 2 MHz ATD clock:

- convert two sequential channels
- continuous-scan
- 8-bit conversion
- 2 final sample cycles

Each of the two channels is sampled once every 12µs. During each sample period a small amount of charge is removed from or added to the external

capacitance (C_f). This charge is restored by charging or discharging through the external source impedance (R_s).

For some values of C_f and R_s, the charge added during the sample time cannot be fully discharged through R_s before the next sample time occurs. This will cause a stair-step building of charge in C_f until an equilibrium is reached, in which the amount of charge added during a sample time is exactly offset by the charge lost during the period between samples.

Due to the small size of the switched capacitance (4pF) for reasonable values of C_f this is highly unlikely to result in a significant error. Errors due to this effect can be minimised by

- careful choice of the R_s and C_f values
- avoiding channel assignments resulting in significantly different levels on adjacent critical channels
- avoiding multiple-channel, continuous-scan conversion modes and short sample times when a high-frequency ATD clock is used.

The following paragraphs describe the cases of interaction of an external filter with an analog input.

1. Where the external time constant is small compared to the length of the sample period. In this case, all residual charge on the internal DAC capacitance is dissipated and the pin settles at the expected voltage before the end of the sample time. In this case, no errors result.
2. Where the external time constant is long compared to the sample period but is relatively short compared to the period between samples. In this case, the residual charge on C_{BUF} is redistributed to the external capacitance during the sample, but this charge is not dissipated through the external resistance before the end of the sample time.

   The voltage change due to redistribution of the residual charge on the converter input capacitance, which is left from conversion of the previous channel, is written as:

$$\Delta V_{SAMP} = (V_2 - V_1)[C_{BUF} \div (C_f + C_{in} + C_{BUF})]$$

   The worse case is where two adjacent inputs are ~ 5V apart, e.g. V_1 = 0V and V_2 = 5.12, and therefore ΔV on the CBUF is ~5V.

$$\Delta V_{SAMP} = (V_2 - V_1)[4pF \div (10nF + 6pF + 4pF)]$$

$$\Delta V_{SAMP} \approx 5.12(4pF \div 10nF)V$$

$$\Delta V_{SAMP} \approx 2mV$$

   This is < 0.5 LSB. Some of this will actually be dissipated before the end of the sample period by the external R_sC_f time constant, so the real error

will be slightly less than this.

Using a slower ATDCLK, selecting a longer sample time and increasing the value of C_s can all help to reduce this error (increasing C_f to 100nf reduces ΔV_{SAMP} to 0.2mV).

This mechanism is unlikely to cause noticeable errors and, in this case, as the charge is dissipated before the next sample of this channel, no accumulated error occurs.

Note that as the value of C_f is reduced ΔV_{SAMP} increases.

3. Where the external time constant is very long compared to the time between samples, and the residual charge redistributed during a sample is not completely dissipated before the next sample, an accumulation of charge can occur.

   This accumulation causes increasing errors on successive samples until equilibrium is reached between the charge added during a sample and the charge dissipated between samples.

   Consider this example:

   - V_{RH} = 5.12 V,
   - V_{RL} = 0.0 V,
   - channel AN1 is connected to a 5.12V analog level (V_1),
   - channel AN2 is connected to a 0V analog level (V_2).
   - external series resistance (R_s) is 2.4 kΩ.
   - external capacitance (C_s) is 100 nF.

   The following pseudo-code is executed to initiate continuous scanned conversion of channels AN1 and AN2.

```
ATDCLT2 = (ADPU | AWAI);
ATDCTL3 = (S2C);                                    /* sequence = 2 conversions */
ATDCTL4 = (PRS2 | PRS0);                            /* Prescaler = 12, 24MHz bus = 2MHz ATDCLK
                                                    (programmable sample clocks = 2)*/

{Delay 20us from setting ADPU to first conversion}

ATDCTL5 = (DJM | SCAN | MULT | CA);                 /* start conversion sequence,
                                                    left justify results,
                                                    continuously repeat sequence,
                                                    convert multiple channels,
                                                    starting at channel 1 */
```

With an ATDCLK of 2MHz, sample time = 2µs, 10-bit conversion time = 5µs and the period from one sample to the next sample of the same channel is 14µs.

The voltage change during the sample is controlled by the ratio of the internal C_{BUF} capacitance to the external capacitance (as in the previous case), but the external R_sC_f time constant is assumed to be so long that it produces no significant effect until after the sample time ends. The voltage change between samples results from a simple RC exponential decay.

$$\Delta V_{HOLD} = (V_{EQ} - V_2)(1 - e^{-t/RsCf})$$

Where V_{EQ} is the equilibrium voltage

$$\Delta V_{HOLD} = (V_{EQ})(1 - e^{-14\mu s/(4.7K \text{ x } 100nF)})$$

$$\Delta V_{HOLD} = V_{EQ}(1 - e^{-0.06})$$

$$\Delta V_{HOLD} = 0.06 V_{EQ}$$

When equilibrium is reached, the voltage gained during a sample is equal to the voltage lost between samples. Therefore, we can set V_{HOLD} equals V_{SAMP} and solve for V_{EQ}:

$$0.06 V_{EQ} = 0.2mV$$

$$V_{EQ} = 0.2mV / 0.06 = \sim 3.6mV$$

This value amounts to approximately 0.75 LSB of error.

In this case, it is not practical to make a general statement about the impact of the value of the external capacitance as it affects both sides of the equation at different rates: First, the time constant of the external RC changes; second, the ratio of the external capacitance to the convertor input capacitance changes.

For external series resistances not exceeding the recommended limit of 2.5KΩ or 10KΩ, the errors attributable to this effect should be very small.

Avoid large values of R_s and small values of C_f. If the external series resistance is increased and small capacitance values are used, the errors can become significant. For example, in the previous example an external RC of 100 KΩ and 1nF would cause errors of about 150 mV (about 30 LSB counts). The extra leakage effects could also be as much as 100 mV.

[redacted]

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