AN13698

PCA9451A application note

Rev. 2.0 — 26 May 2023 **Application note**

Document Information

Information	Content
Keywords	PCA9451A, I.MX 93x, PMIC
Abstract	This application note discusses the critical items needed in designing the PMIC PCA9451A in portable devices with an i.MX 93x application processor, and provides a guideline for component selection, placement, and trace routing.

Revision history

Rev	Date	Description
v.2.0	20230526	• Updated Figure 1, Figure 2, Figure 3, and Figure 7
v.1.0	20220830	Initial version

1 Introduction

The PCA9451A is a single chip Power Management IC (PMIC) specifically designed to support i.MX 93x family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5 V adapter non-portable applications.

The device provides six high-efficiency step-down regulators, three LDOs, one 400 mA load switch, 2-channel level translator, and 32.768 kHz crystal oscillator driver. Three buck regulators support dynamic voltage scaling (DVS) feature along with programmable ramping up and down time; the buck regulators support remote sense to compensate IR drop to load. This device is characterized across -40 °C to 105 °C ambient temperature range.

Six step-down regulators are designed to provide power for i.MX 93x application processor and DRAM memory. One LDO (LDO1) feature very low quiescent current to provide power for Secure Non-Volatile Storage (SNVS) since this LDO is always ON when input voltage is valid.

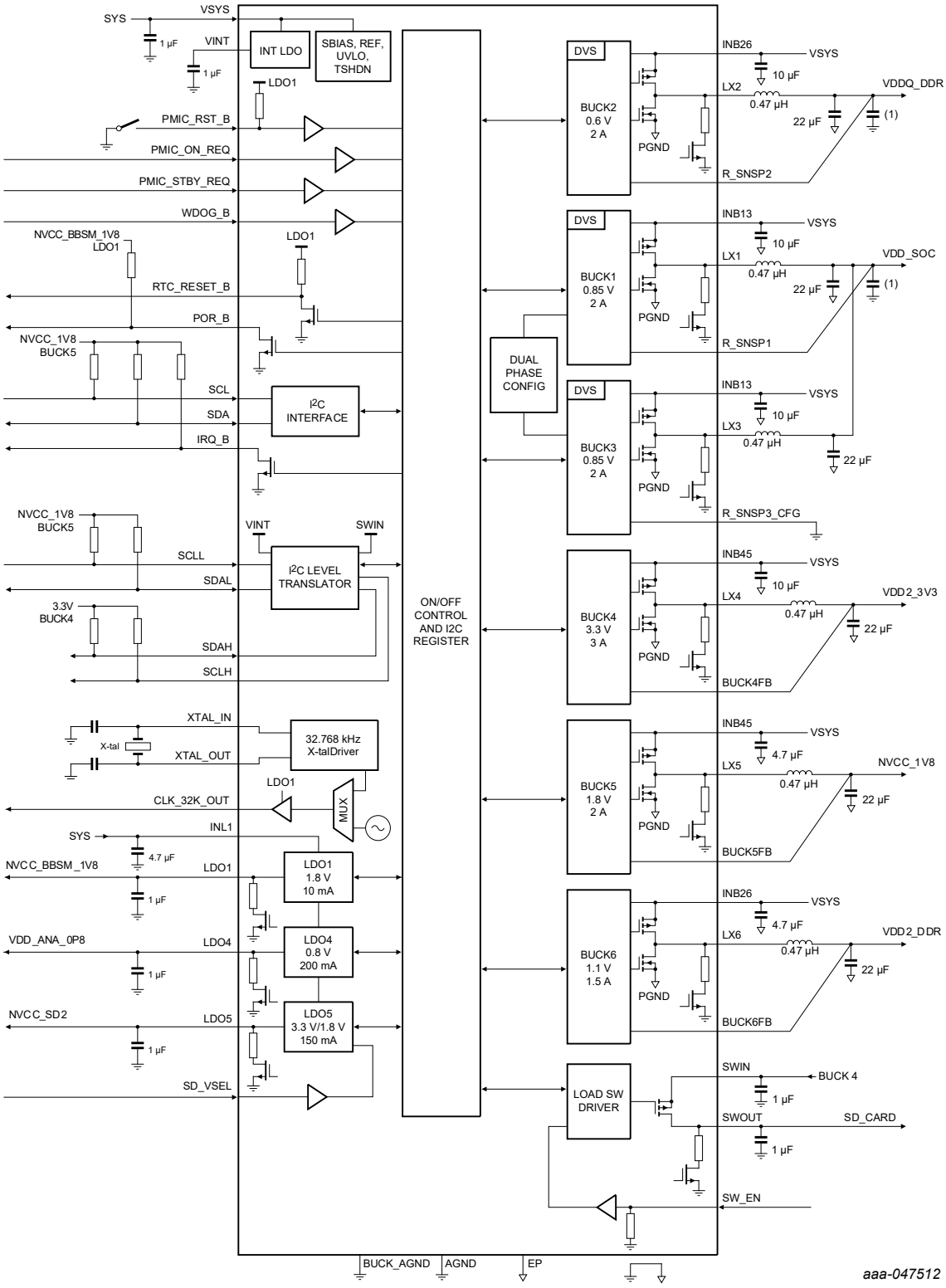
PCA9451A integrates logic translator which is a 2-bit, dual supply translating transceiver with auto direction sensing. It enables bidirectional voltage level translation and can be used as an I^2C level translator. A 400 mA load switch is to supply 3.3 V power supply to SD card, which has an internal discharge resistor.

The PCA9451A is offered in 56-pin HVQFN package, 7 mm x 7 mm, 0.4 mm pitch.

2 Features and benefits

- Six high-efficiency step-down regulators
  - 4 A dual phase buck regulator with DVS feature and remote sense
  - 2 A buck regulator with DVS feature and remote sense
  - 3 A buck regulator
  - 2 A buck regulator
  - 1.5 A buck regulator
- Three linear regulators
  - One 10 mA LDO
  - One 150 mA LDO
  - One 200 mA LDO
- 400 mA load switch with built-in active discharge resistor
- Two channel logic level translator
- 32.768 kHz crystal oscillator driver
- Power control IO
  - Power ON/OFF control
  - Standby/run mode control
- Fm+ 1 MHz I^2C-bus interface
- ESD protection
  - Human Body Model (HBM): ±2000 V
  - Charged Device Model (CDM): ±500 V
- 7 mm x 7 mm, 56-pin HVQFN with 0.4 mm pitch

3 Block diagram



(1) Decoupling capacitor in MCU side.

Figure 1. Block diagram

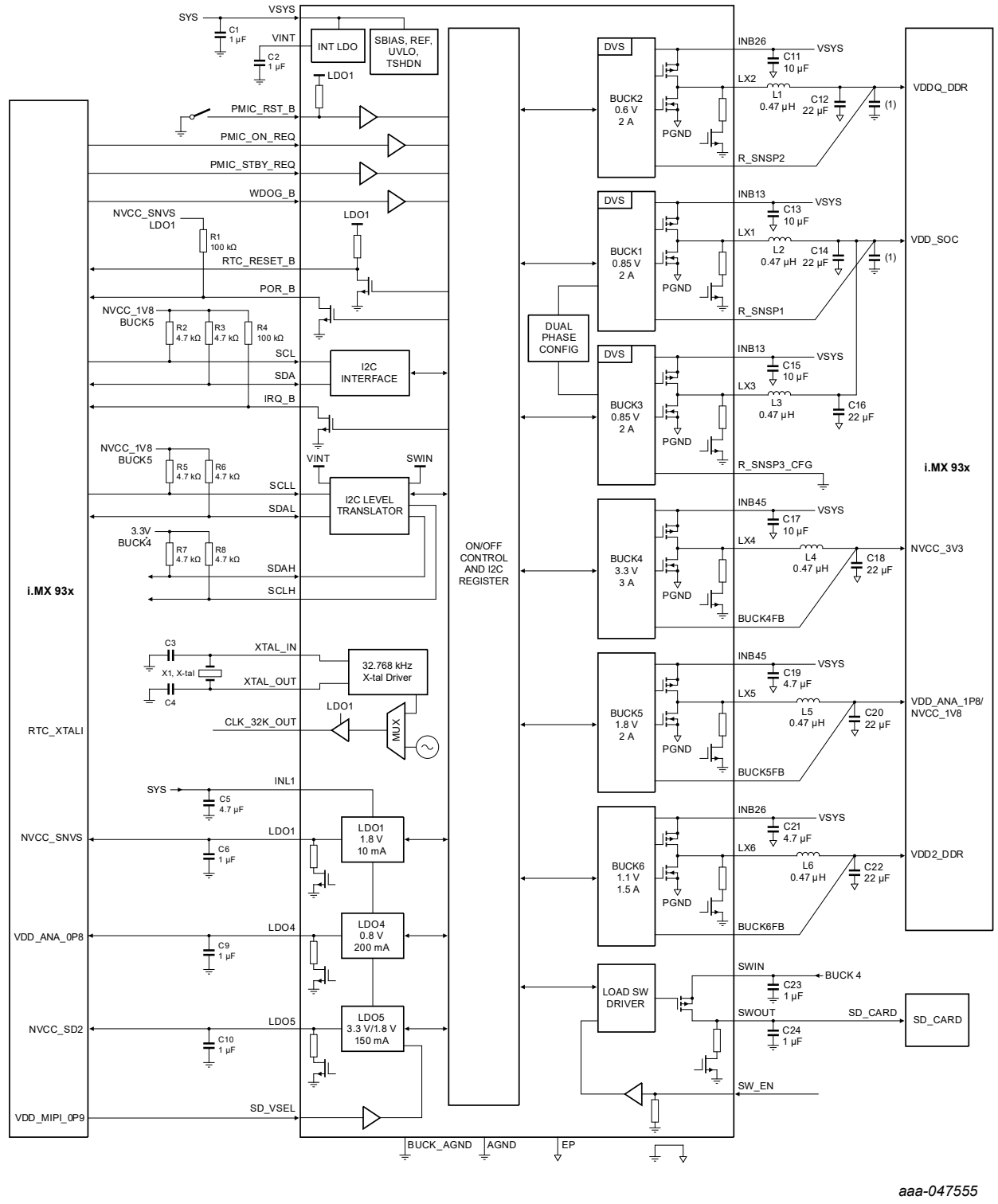
4 Application design-in information

4.1 Reference schematic

PCA9451A reference schematic with i.MX 93x + LPDDR4X is illustrated in Figure 2.

The schematic serves as a guide on how the output voltage rails on PCA9451A would be typically connected to the corresponding voltage domains on i.MX 93x, and external components such as the memories (DDR and or EMMC/SDHC). This configuration is not mandatory and the customer can make adjustments as long as the voltage and sequencing requirements for the processor are respected and are supported by PCA9451A.

Please refer to the corresponding i.Mx 93x EVK for detailed design information and schematic/layout source files.



aaa-047555

(1) Decoupling capacitor in MCU side.

Figure 2. PCA9451A + i.MX93x + LPDDR4X application schematic

4.2 Typical application

The PCA9451A device has only a few design requirements, as follows:.

- 1 µF bypass capacitor on VINT and VSYS, located as close as possible to those pins to ground
- If using INB and INL supplies, input capacitors must be present
- Output inductors and capacitors must be used on the outputs of the BUCK converters if used
- Output capacitors must be used on the outputs of the LDOs

4.2.1 Inductor selection for buck converters

Each of the converters in the PCA9451A typically use a 0.47 µH output inductor which has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 2. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1-\frac{Vout}{Vinmax}}{L \times f} \quad (1)$$

$$I_{L.max} = I_{out.max} \times \frac{\Delta I_L}{2} \quad (2)$$

Where

f = switching frequency (2 MHz)

L = Inductance

ΔI_L = Peak to peak inductor ripple current

$I_{L.max}$ = Maximum inductor current

A conservative approach is to select the inductor current rating just for the maximum switch current of the PCA9451A

Table 1 shows possible inductors list.

Table 1. Tested inductor list

Buck	Vendor	Part number	Inductance [uH]	Size [mm]	DCR [mΩ]	Isat [A]	Irat [A]
BUCK1, BUCK2, BUCK3, BUCK4	Sunlord	WPN252012 HR47MT	0.47	2520	29	5.6	4.0
	Murata	1239AS-H-R47M	0.47	2520	39	3.8	3.7
	Cyntec	HMLB25201 B-R47MSR	0.47	2520	26	4.55	4.0
BUCK5, BUCK6	Sunlord	WPN201610 UR47MT	0.47	2016	28	5.0	4.1
	Murata	1286AS-H-R47M	0.47	2016	52	3.4	3.2
	Cyntec	HTEP20120 H-R47MSR	0.47	2012	29	4.3	3.7

4.2.2 Output capacitor selection for buck converters

The fast response adaptive constant ON time control scheme of the buck converters implemented in the PCA9451A allows the use of small ceramic capacitors with a typical value of 22 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 2 for recommended capacitor.

Table 2. Recommended capacitor

BUCK	Vendor	Part number	Capacitance [µF]	Size [mm]	Voltage [V]
BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, BUCK6	TDK	C1608X5R1A226M080AC	22	0603	10
	TDK	C1608JB1A226M080AC	22	0603	10
	Murata	GRT21BC81A226ME	22	0805	10

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 3.

$$I_{RMS.COUT} = \text{Vout} \times \frac{1-\frac{\text{Vout}}{\text{Vin}}}{\text{L} \times \text{f}} \times \frac{1}{2\sqrt{3}} \quad (3)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta\,\text{Vout} = \text{Vout} \times \frac{1-\frac{Vout}{Vin}}{\text{L} \times \text{f}} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \quad (4)$$

Where:

- The highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PFM mode and the output voltage ripple is dependent on the output capacitor value.The internal comparator delay and the external capacitor set the output voltage ripple, which is less than 1 % of the nominal output voltage.

4.2.3 Input capacitor selection for buck converters

Low ESR input capacitor is highly recommended for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes because of the nature of buck converter. Each DC-DC converter requires a 10 µF ceramic input capacitor on its input pins. The input capacitor could be increased without any limit for better input voltage filtering. See Table 3 for recommended capacitor.

Table 3. Recommended capacitor

BUCK	Vendor	Part number	Capacitance [µF]	Size [mm]	Voltage [V]
BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, BUCK6	Murata	GRM188R60J106ME	10	1608	6.3
	Samsung	CL10A106MQ8NN	10	1608	6.3
	Murata	GRM188Z71A106KA73D	10	1608	10

4.2.4 VSYS, VINT, LDO1, LDO4, LDO5, SWIN and SWOUT capacitor selection

Internal power input, internal power supply output, LDOs, and load switch pins are all required to be bypassed by a low ESR 1 µF ceramic capacitor. Table 4 shows the recommended capacitor.

Table 4. Recommended capacitor

PIN	Vendor	Part number	Capacitance [µF]	Size [mm]	Voltage [V]
VINT, VSYS, LDO1, LDO4, LDO5, SWIN, SWOUT	Murata	GRM188R60J106ME	1	1005	16
	Samsung	CL10A106MQ8NN	1	1005	16
	Murata	GRM155C71A105KE11D	1	1005	10

5 Design guidelines

5.1 Package

The PCA9451A device is intended for use in commercial and industrial applications and is offered in a 56-pin HVQFN package, 7mm x 7mm, 0.4mm pitch. Refer to Application Note AN1902 (https://www.nxp.com/docs/en/application-note/AN1902.pdf) for guidelines on the handling and assembly of NXP QFN packages during PCB assembly, guidelines for PCB design and rework, and package performance information (such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical, and thermal resistance data).

Package dimensions are provided in package drawings. To find the most current package outline drawing, refer to the package link: SOT949-6 (nxp.com)

5.2 Placement

All components related to the power stage should be kept as close to the PMIC as possible, especially decoupling input and output capacitors.

Place these components in order of priority:

- Input capacitor of the buck regulators
- LDO capacitors
- VSYS and VINT capacitors
- Buck regulator inductors
- Buck regulator output capacitors

Layout guide is shown in Figure 3.

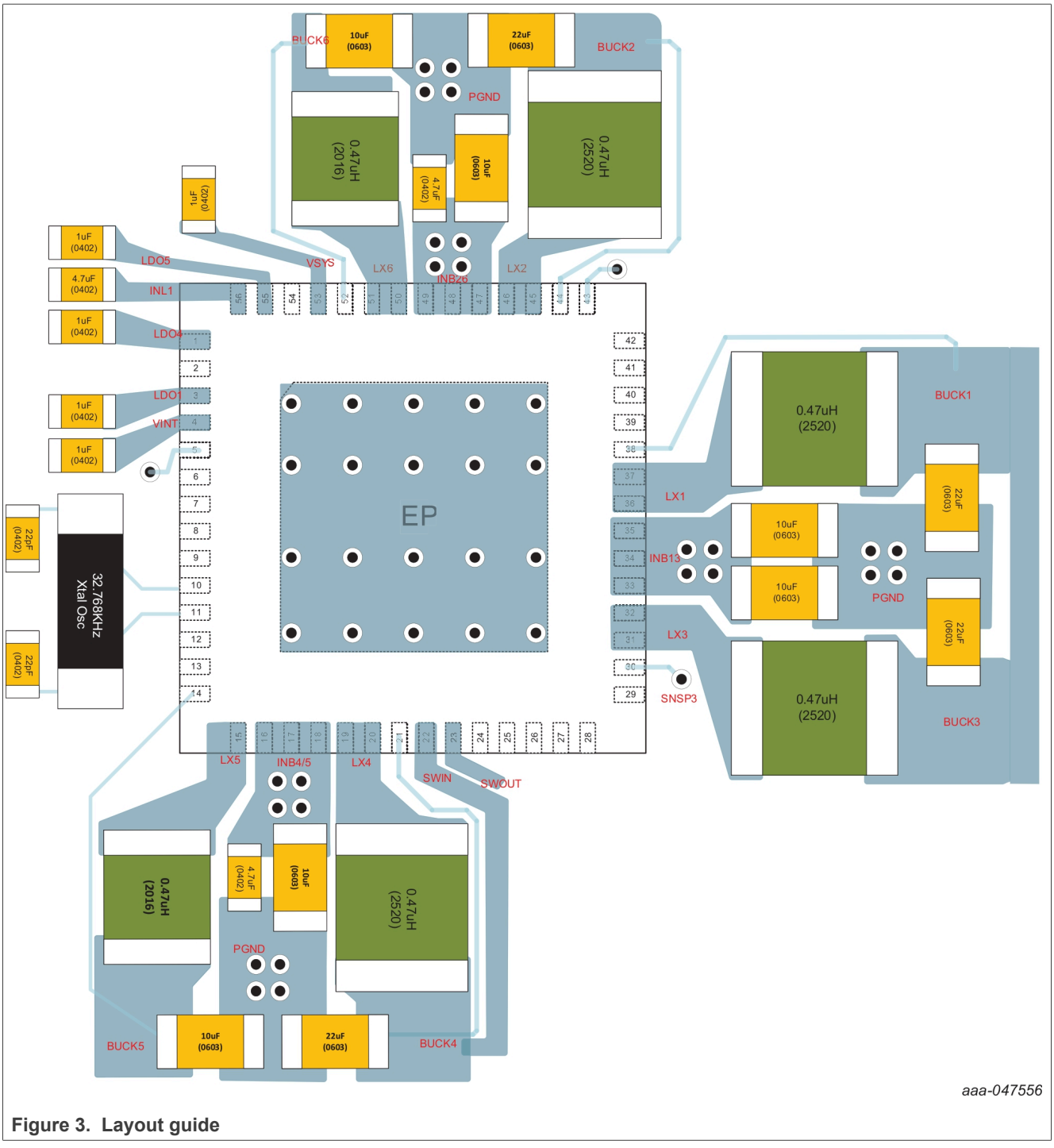


Figure 3. Layout guide

5.3 Switching regulator schematic recommendations

Figure 4 shows the critical path in buck converter which has high di/dt.

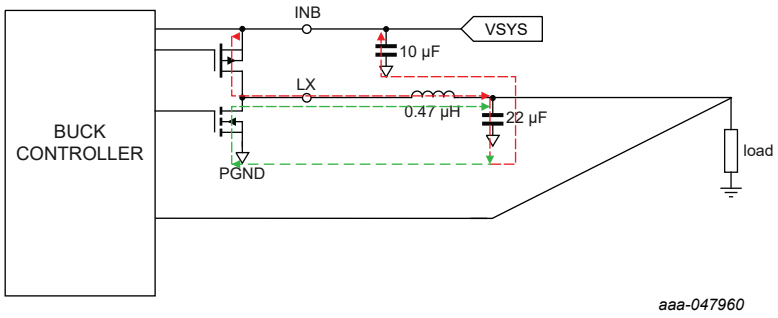


Figure 4. Buck schematic

The biggest challenge in buck layout is EMI. To minimize the EMI requires the minimum loop area of two high di/dt paths as shown in Figure 4. The area in red is input power charging the inductor when high side FET is on; the area in green is inductor discharge energy to output capacitor (load) when low side FET is on.

5.4 Layout guidelines

5.4.1 General routing requirements

1. Some recommended things to keep in mind for manufacturability:
   - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
   - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
   - Minimum allowed spacing between line and hole pad is 3.5 mils
   - Minimum allowed spacing between line and line is 3.0 mils
2. Care must be taken with BUCKxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the INBxx, and LXx pins. They could be also shielded.
3. Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
4. Make sure all components related to a specific block are referenced to the corresponding ground.
5. Use the shortest path to route the trace including the return path (ground).
6. Make sure that the trace is capable of handling the maximum current in the application.
7. Keep enough vias to connect the ground pad to main ground; this not only reduces the parasitic inductance but also helps with heat dissipation.

5.4.2 Parallel routing requirements

- I^2C signal routing
  1. SCL is one of the fastest signals of the system, so it must be given special care.
  2. To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length, as shown in Figure 5
  3. These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
  4. Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

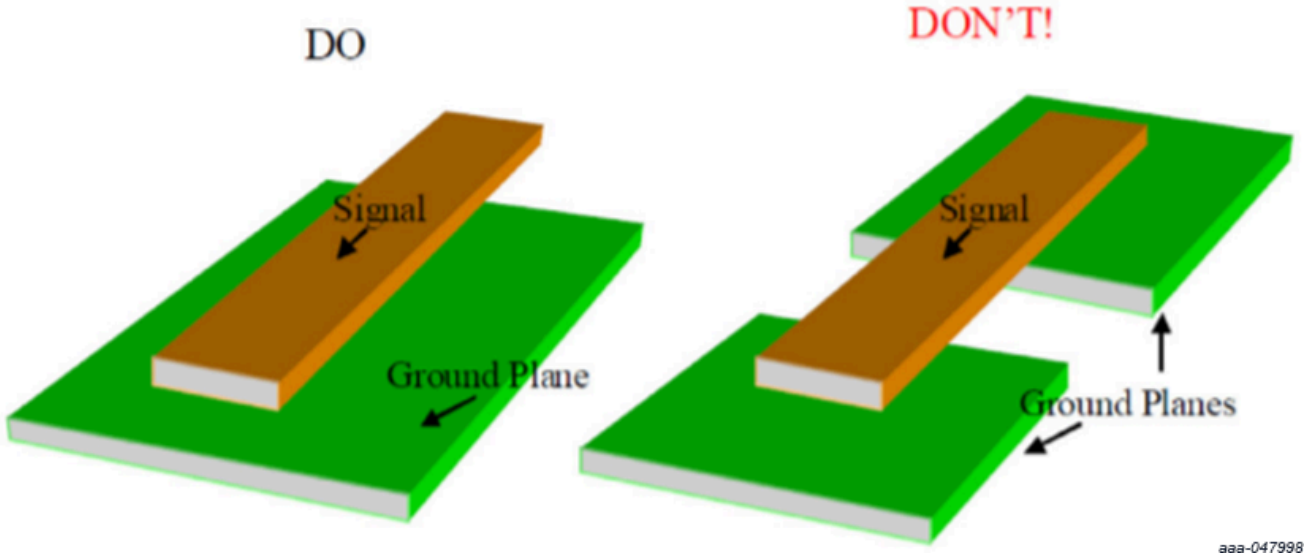


Figure 5. Recommended shielding for critical signals

5.4.3 Switching regulator layout recommendations

1. Put the input/output capacitor and inductor as close to chip as possible to minimize the loop area. If using the high frequency bypass capacitor to filter the EMI, make sure this high frequency capacitor is close to the chip.
2. Make high-current ripple traces low-inductance (short, high W/L ratio).
3. Make high-current traces wide or copper islands.
   a. Maximum current on Lx pin to inductor is around 1.4 times maximum loading current by quick estimation.

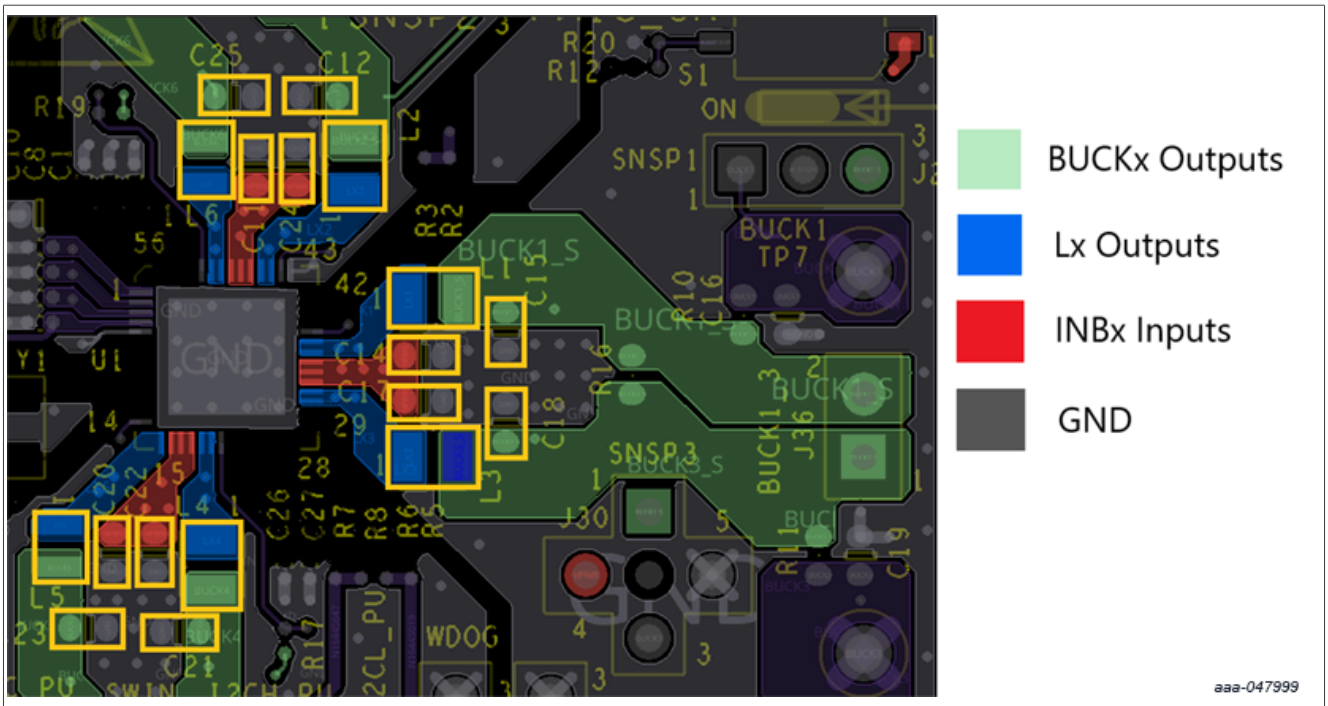


Figure 6. Layout example for buck regulators

5.4.4 BUCK1/BUCK3 dual-phase buck

BUCK1 and BUCK3 are configured as dual phase buck. R_SNSP3_CFG pin should be connected to ground. This dual phase buck regulator is controlled through BUCK1 registers. All BUCK3 registers are not responsive under dual-phase configuration.

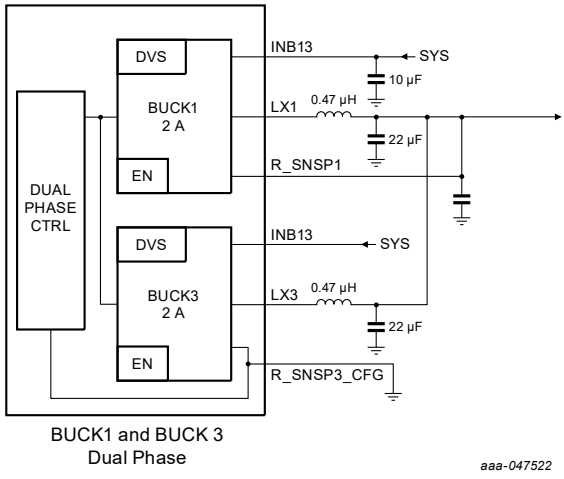


Figure 7. BUCK1 and BUCK3 configuration

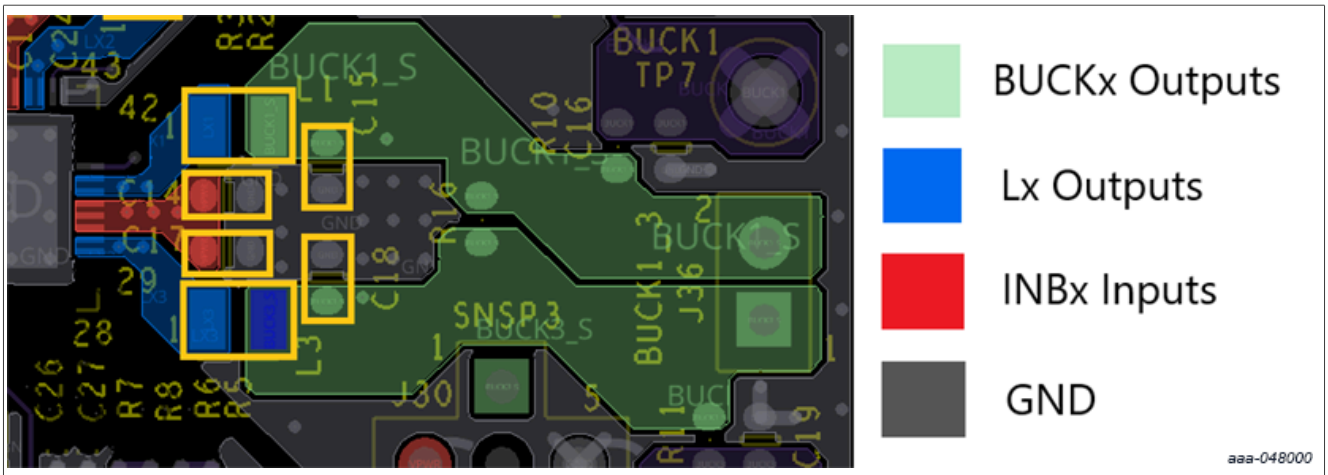


Figure 8. Layout example for BUCK1 and BUCK3

5.4.5 LDO

PCA9451A integrates three LDOs with different output current capability for different purposes. The output capacitor needs to be as close as possible to the chip. Make sure the trace is wide enough to carry the maximum current in the application.

Table 5. LDO summary

LDO#	Default VOUT [V]	VOUT range [V]	Step size [mV]	Default ON/OFF	Current rating [mA]
LDO1	1.8	1.6 - 1.9 / 3.0 - 3.3	100	ON	10
LDO4	0.8	0.8 – 3.3	100	ON	200
LDO5	3.3 / 1.8[1]	1.8 – 3.3	100	ON	150

[1] Voltage selection through SD_VSEL pin

5.4.6 Ground

The exposed pad (EP) is the power ground of all bucks which is relatively noisy. AGND is the analog ground. Do not connect AGND to EP on the top layer. Connect AGND to main ground by via. Avoid separating the main ground under PCA9451A which may increase the return path. Make sure there are enough vias to connect EP to system main ground.

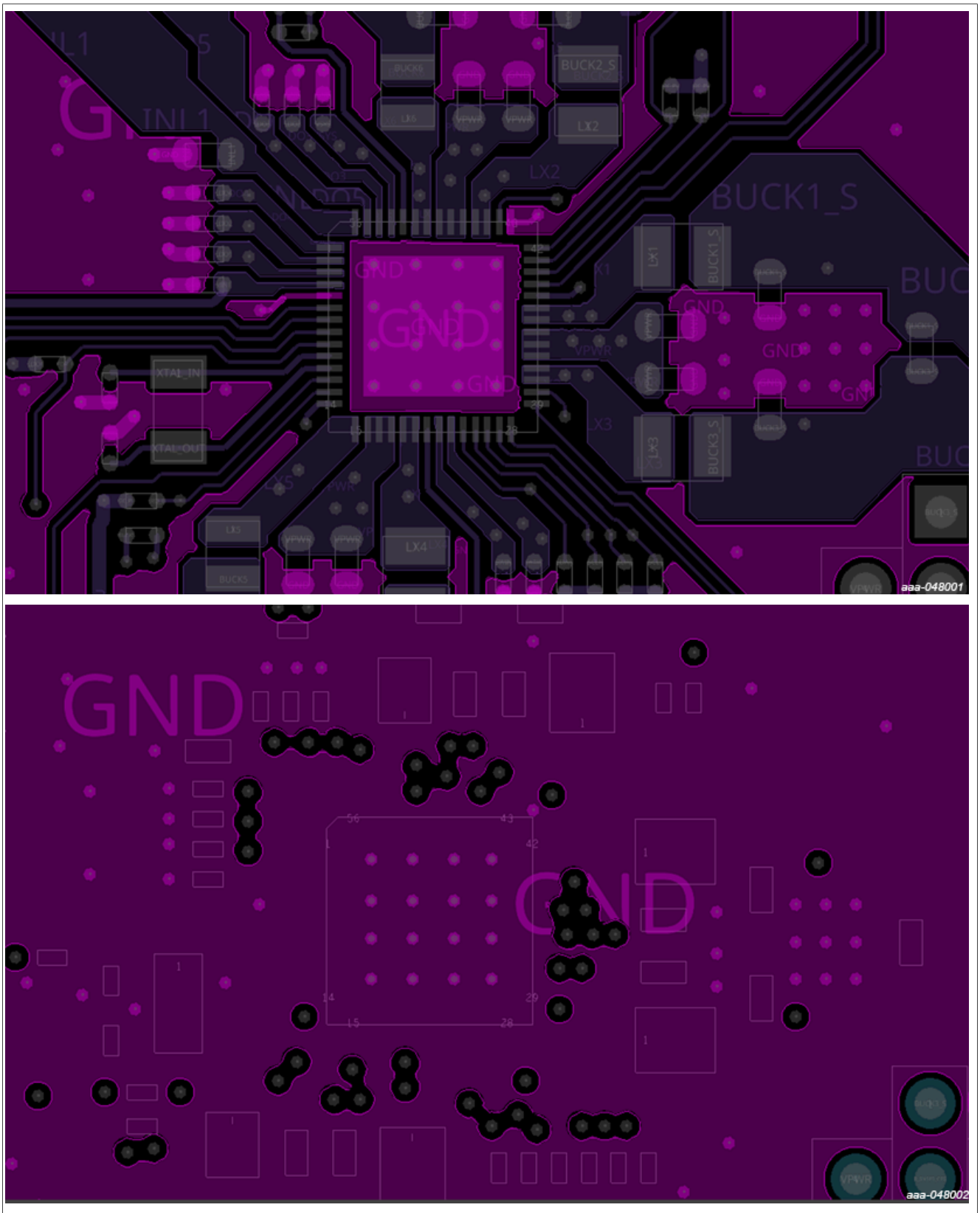


Figure 9. Ground layout example

6 Thermal analysis

6.1 Rating data

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol RθJA or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. RθJMA or θJMA (ThetaJMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org/.

6.2 Estimation of junction temperature

An estimation of the chip junction temperature TJ can be obtained from Equation 5:

$$TJ = TA + \left(R\theta JA \times PD\right) \quad (5)$$

Where:

- TA = Ambient temperature for the package in °C
- RθJA = Junction to ambient thermal resistance in °C/W
- PD = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board RθJA and the value obtained on a four layer board RθJMA. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

7 PCB design guidelines

7.1 Package dimensions

Package dimensions are provided in package drawings. The latest package outline drawing can be found at the package link: SOT949-6 (nxp.com)

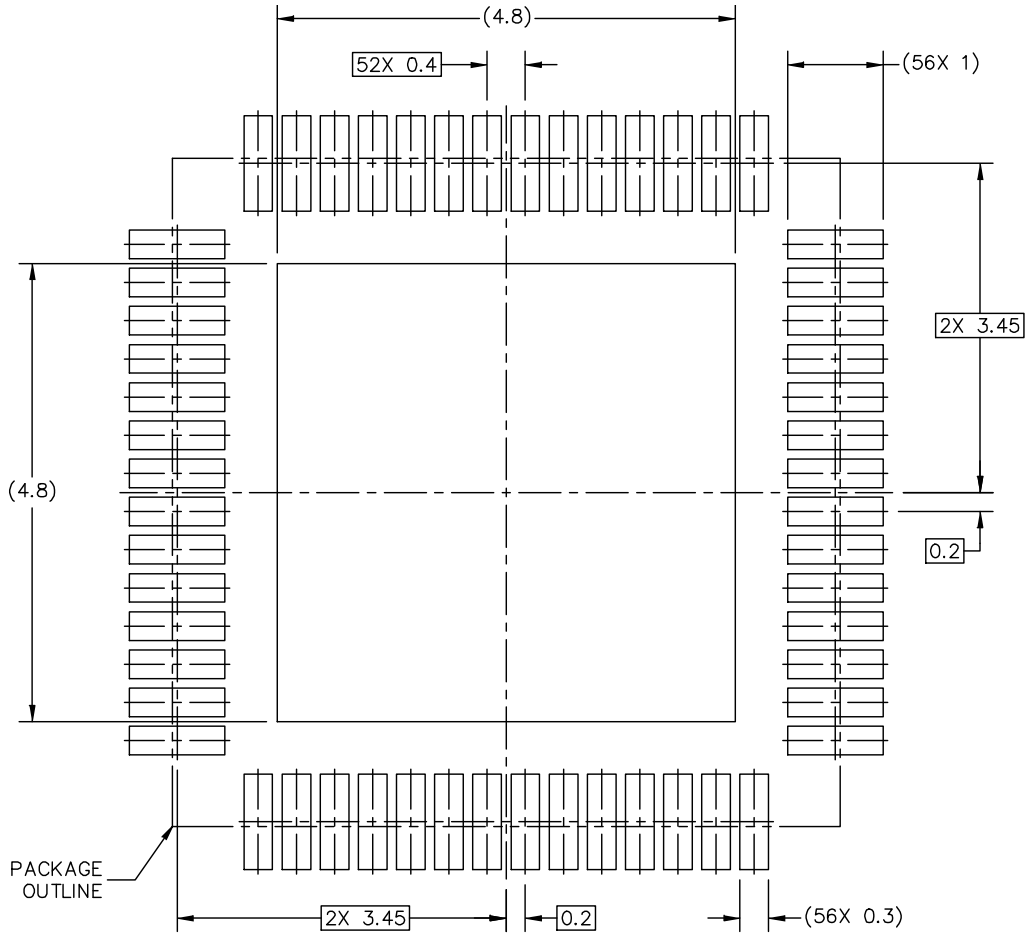


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Figure 10. PCB design guidelines for HVQFN56 (SOT949-6); solder mask opening pattern

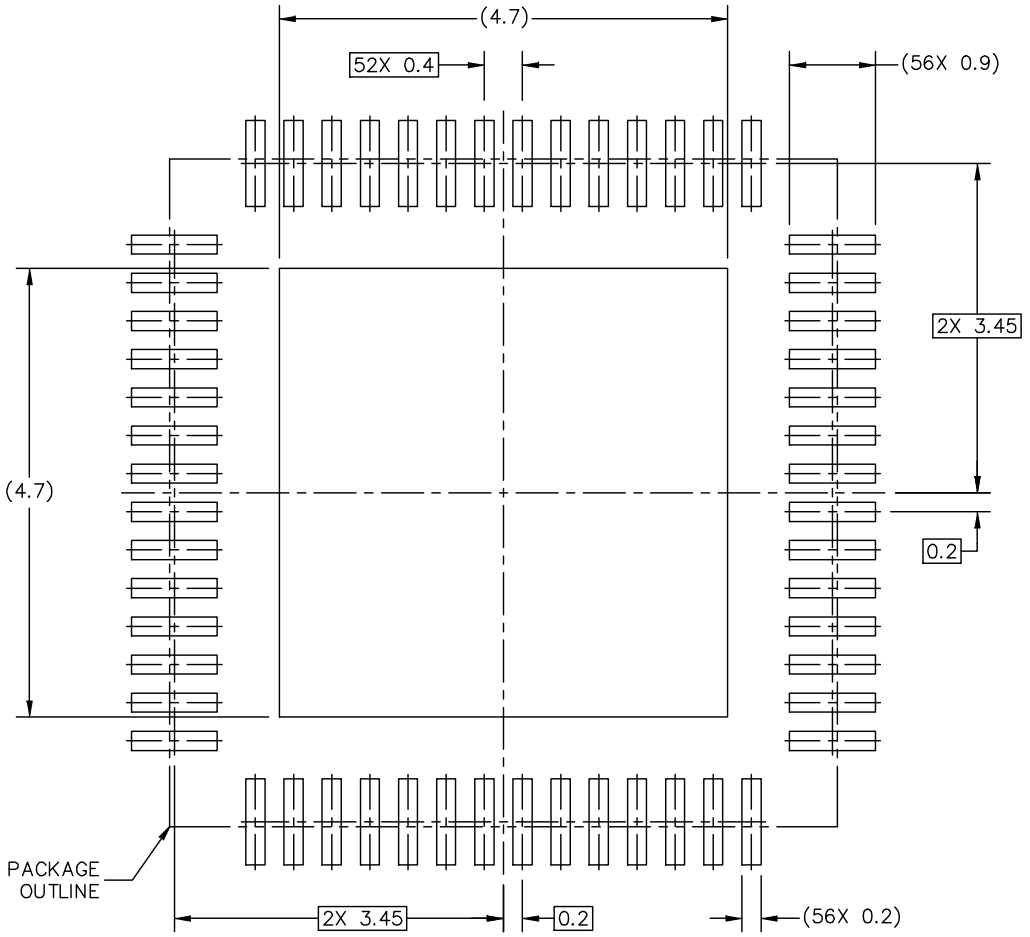

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Figure 11. PCB design guidelines for HVQFN56 (SOT949-6); I/O pads and solderable area

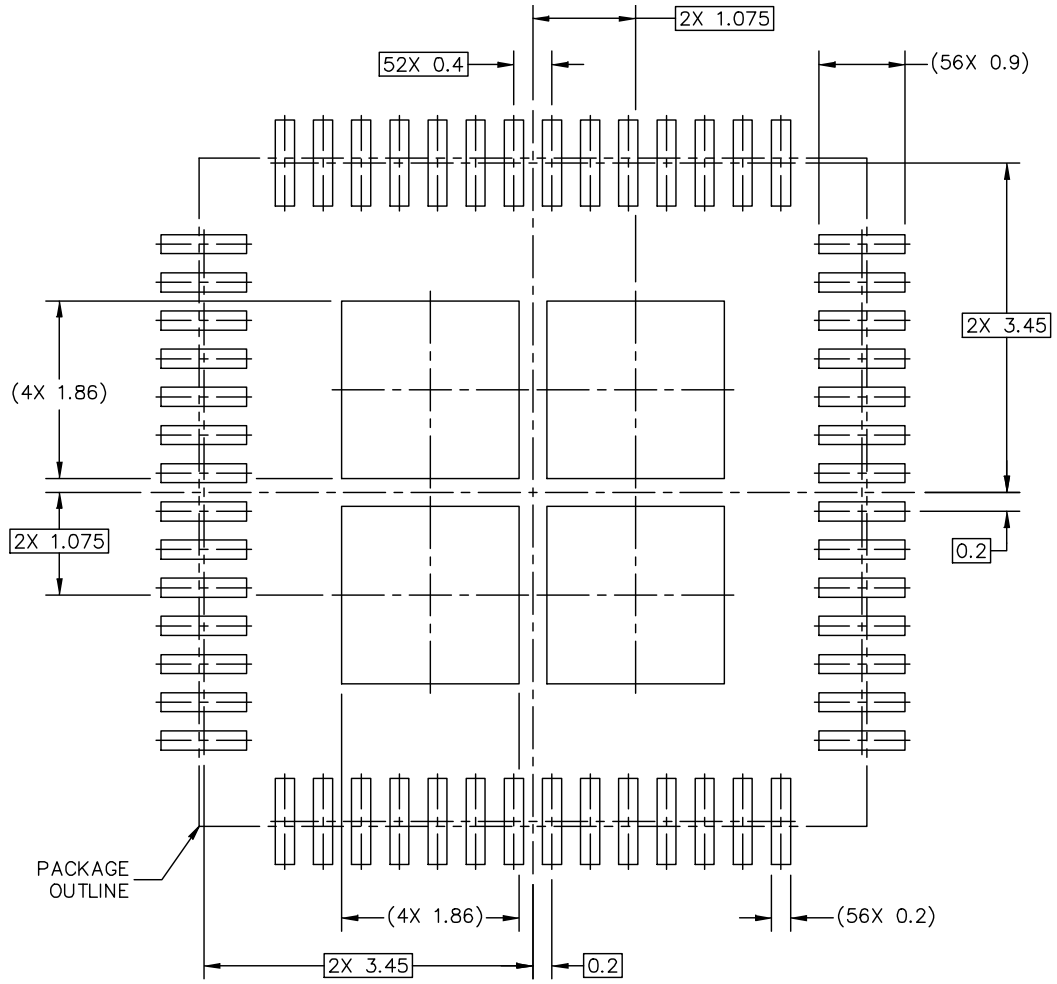

Figure 12. PCB design guidelines for HVQFN56 (SOT949-6); solder paste stencil

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