

# AN11392

## Guidelines for full-speed USB on NXP's LPC microcontrollers

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Application note

### Document information

Info	Content
<b>Keywords</b>	Full-speed USB, Full-speed USB device, Full-speed USB host, USB PCB layout, LPC11Uxx, LPC13xx, LPC17xx, LPC2xxx
<b>Abstract</b>	This document describes some of the issues that you may encounter when developing a full-speed USB application on NXP's LPC microcontrollers. Possible solutions are detailed.



**Revision history**

Rev	Date	Description
1.1	20140219	Updated Section 2.7, second paragraph, second sentence.
1	20130820	Initial version.

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## 1. Introduction

Full-speed USB operates at 12 Mb/s, and although this is not a high data rate, observing some basic rules or guidelines will usually guarantee successful operation. This application note highlights some of the more important issues that you need to be aware of for a typical full-speed USB application.

## 2. Typical full-speed USB schematics

### 2.1 Termination resistors

In [Fig 1](#), there are two 33  $\Omega$  resistors (R1 and R2) that are required for proper USB operation. The USB specification requires that the USB device have a 45  $\Omega$  single-ended or 90  $\Omega$  differential impedance. This impedance includes the impedance of the USB transceiver. The impedance of the USB transceiver is lower than the requirement of the USB specification, so the 33  $\Omega$  resistors are required to bring the device impedance within the required specification limits. At this time, all NXP microcontrollers with a full-speed USB peripheral use 33  $\Omega$  resistors, but please check the device data sheet or reference schematics as this value may change.

These resistors should be placed as close to the microcontroller as possible.

### 2.2 USB\_Connect

A full-speed USB device requires a 1.5 k $\Omega$  resistor between the USB\_DP pin and 3.3 V. A USB host controller has 15 k $\Omega$  resistors on both the USB\_DP and USB\_DM signal lines, which holds them in a low state. When the USB device is plugged into a USB host controller, the host detects the device when it senses that the USB\_DP line has been pulled high through the 1.5 k $\Omega$  resistor.

The USB\_Connect circuit is shown in [Fig 1](#). It uses a PNP transistor and a base transistor (a Resistor Equipped Transistor (RET) may also be used to minimize the component count) to allow the user to connect or disconnect the 1.5 k $\Omega$  pull-up resistor from USB\_DP. When the USB\_Connect signal goes low, the PNP transistor turns on and the 1.5 k $\Omega$  resistor pulls up the USB\_DP signal. This indicates to the USB host that a USB device has been inserted into the USB connector.

It is not required that you use USB\_Connect in a bus-powered application. If USB\_Connect is not used, then the 1.5 k $\Omega$  pull-up resistor can be directly connected between USB\_DP and the 3.3 V supply voltage.

When using the microcontroller in a self-powered application, you are required to use USB\_Connect. The reason it is needed is due to the USB back-voltage test requirement. The USB specification states that a maximum of 400 mV may be measured on the VBUS, USB\_DP, or USB\_DM when the device is not plugged into a USB port. In a self-powered application, if the 1.5 k $\Omega$  resistor was connected directly between the 3.3 V supply and the USB\_DP line, then the voltage on USB\_DP would exceed the 400 mV limit imposed by the USB specification, and you would fail compliance testing. Implementing USB\_Connect ensures that USB\_DP will not exceed the 400 mV requirement, since the microcontroller will automatically place USB\_Connect in a high state when VBUS is not detected (when it is not connected to a USB host controller). See the "Universal Serial Bus Implementers Forum Full and Low Speed Electrical and Interoperability Compliance Test Procedure" that can be downloaded from the [usb.org](http://usb.org) website for further details.

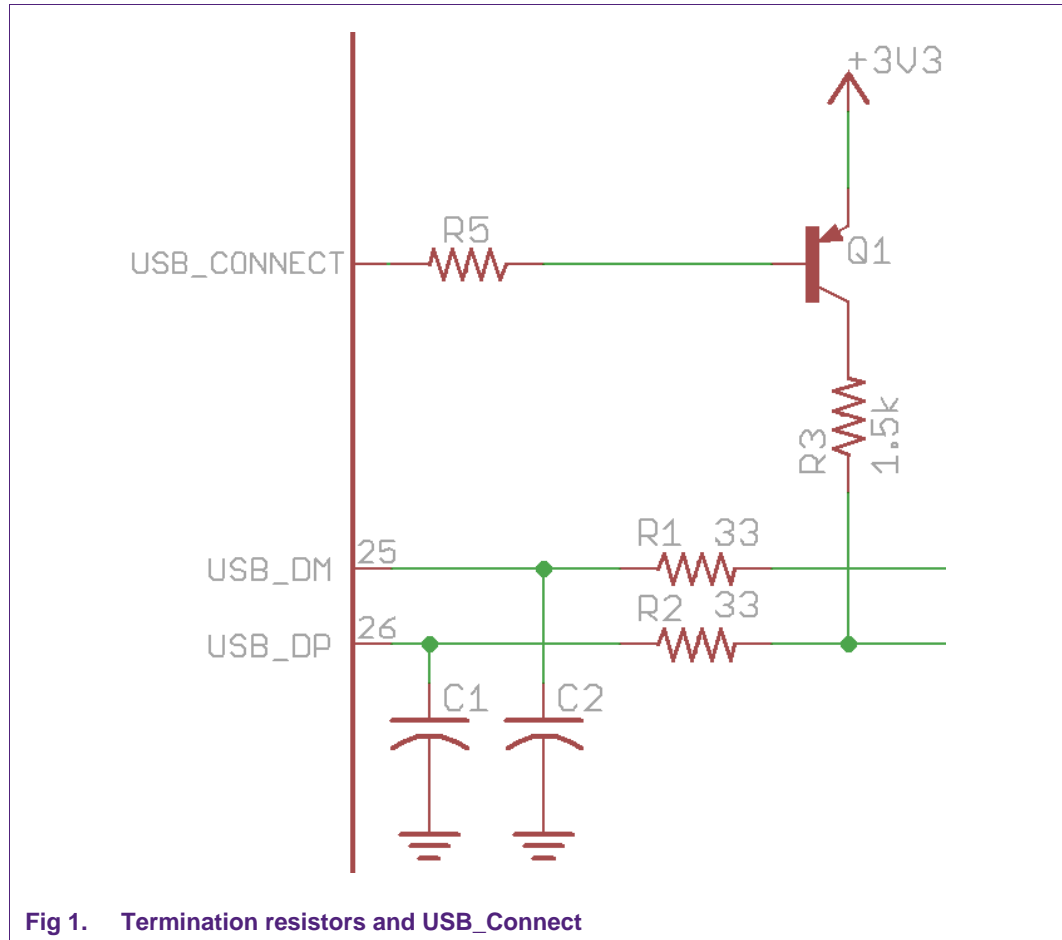


Fig 1. Termination resistors and USB\_Connect

### 2.3 VBUS

The VBUS pin on the microcontroller should be connected to the VBUS pin on the USB connector. A series resistor between the connector and the VBUS pin can be included to minimize the chance of a noise spike causing damage to the VBUS pin.

The VBUS pin is 5 V tolerant as long as there is a voltage applied to the microcontroller's supply pins. If there is no voltage on the supply pins, then the voltage applied to the VBUS pin must be limited to a maximum of 3.6 V. You may encounter this situation in a self-powered application where you power-down the supply to the microcontroller while the USB device is still plugged into a USB port.

If there is a possibility that the microcontroller could be unpowered while voltage is still applied to VBUS, then a resistor divider network should be placed between the connector and VBUS to ensure the maximum voltage is 3.6 V. In Fig 2, a voltage divider made of 24 kΩ and 39 kΩ resistors is used to limit the voltage at pin USB\_VBUS. The value of the resistors is not critical, however, if they are too low they will consume excess current through the voltage divider.

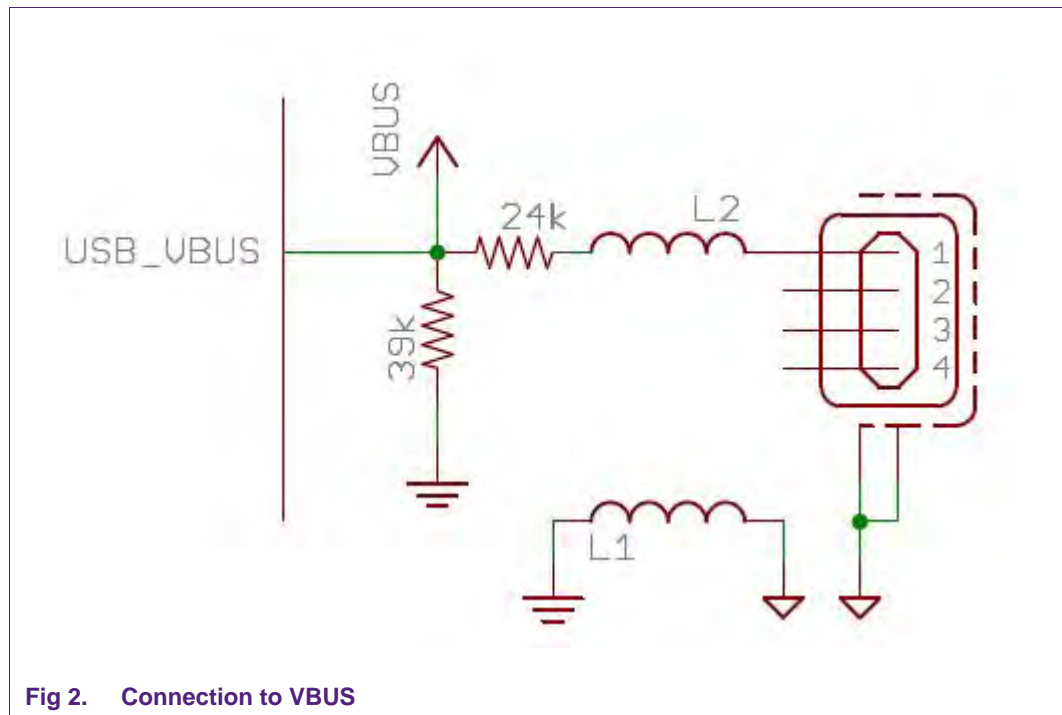


Fig 2. Connection to VBUS

## 2.4 Bypass capacitors

It is important to use a decoupling capacitor on each supply pin. A recommended value to start with is 0.1  $\mu\text{F}$ .

## 2.5 Inrush current limiting

A USB device has a capacitance between VBUS and ground. If this capacitance is too high, an excessive current will flow when it is first plugged into the USB host port. This will cause the voltage on VBUS to droop more than the maximum allowable 330 mV dictated by the USB specification. In order to ensure that the VBUS voltage does not drop below the allowable limit, the maximum load at the end of a USB cable is defined by the USB specification to be 10  $\mu\text{F}$  in parallel with 44  $\Omega$ . The 10  $\mu\text{F}$  represents the capacitance directly connected to the VBUS line, in addition to any capacitance that is visible through the voltage regulator. The 44  $\Omega$  resistance is equivalent to one unit load drawn by the device.

Care must be taken to avoid exceeding the inrush current since this parameter is monitored during USB compliance testing, and is one of the frequent reasons for failing USB testing.

## 2.6 EMI/ESD considerations

Cables for full-speed USB must include an integrated shield. A properly designed cable offers significant EMI suppression on the conductors inside the shield. The challenge for USB compliance is preventing the high frequency energy from the PCB from being coupled to the shield. A ferrite bead may be used between the USB connector shield and PCB ground to improve the EMI from the PCB from being coupled to the cable shield. This is shown as component L1 in [Fig 2](#).

Noise from VBUS and ground may be improved by using ferrite beads.

Although it is possible to use ferrite beads on the USB\_DP and USB\_DM signal lines in a full-speed application, it is not recommended.

Capacitors C1 and C2 in [Fig 1](#) may be used for edge rate control and to bypass high frequency energy to ground. These capacitors should be limited to a maximum of 50 pF and should be located as close to the microcontroller as possible. The capacitors are not required for the LPC microcontrollers to meet the “eye diagram” signal testing requirements, but improvements in noise-related problems have been reported when using the capacitors.

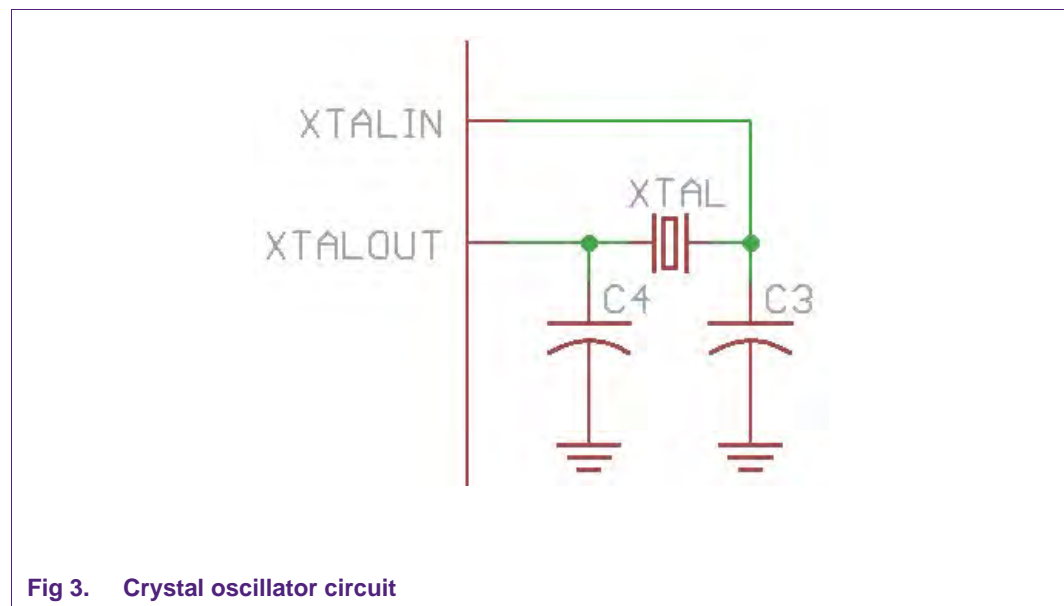
ESD protection diodes with a maximum capacitance of 50 pF are recommended on the USB\_DP and USB\_DM signal lines; this capacitance should be taken into consideration if the edge rate capacitors C1 and C2 are included in the schematics.

## 2.7 Clock circuit

When using a full-speed USB peripheral, it is important to use an external crystal, or a tight frequency tolerance ceramic resonator, for the timing element. The internal 12 MHz  $\pm 1\%$  RC oscillator, while very accurate, does not have the accuracy required for USB.

The USB peripheral operates at a clock frequency of 48 MHz, so the crystal must be chosen such that a multiple of its frequency is equal to 48 MHz. A parallel resonant 12 MHz crystal with a data signaling tolerance of 0.25 %, or  $\pm 2500$  ppm is required.

[Fig 3](#) shows the crystal oscillator circuit for the LPC microcontrollers.



**Fig 3. Crystal oscillator circuit**

The value of the crystal load capacitors (C3 and C4 in [Fig 3](#)) affects the accuracy of the oscillator. The following formula may be used to calculate a parallel resonant crystal's external load capacitors:

$$CL = ((C3 \times C4) / (C3 + C4)) + C_{\text{stray}}$$

where:

CL = the crystal load capacitance

$C_{\text{stray}}$  = the stray capacitance in the oscillator circuit, which will normally be in the 2pF to 5pF range.

Assuming that  $C3=C4$  then the equation becomes:

$$CL = ((C3 \times C4) / (2 \times C3)) + C_{\text{stray}}$$

$$CL = (C3 / 2) + C_{\text{stray}}$$

Rearranging the equation, we can find the external load capacitor value:

$$C3 = 2(CL - C_{\text{stray}})$$

For example, if the crystal load capacitance is 15 pF, and assuming  $C_{\text{stray}} = 5$  pF, then:

$$C3 = C4 = 2(15 \text{ pF} - 5 \text{ pF}) = 20 \text{ pF}$$

It is difficult to know exactly what the stray capacitance is on a particular PCB, but if you find the oscillation frequency is too high, the load capacitor values can be increased. If the frequency is too low, the load capacitors can be decreased. The best place to measure a clock frequency is using the CLKOUT pin (if available). Do not measure the oscillator frequency by attaching an oscilloscope probe to the XTAL pins, as the capacitance of the oscilloscope probe can affect the oscillator frequency.

## 2.8 Supply voltage range

Most LPC microcontrollers operate over a wide operating voltage range. A typical voltage range is 1.8 V to 3.6 V. However, when using the USB peripheral, the supply voltage range should be maintained between 3.0 V and 3.6 V for proper USB functionality. Operating outside this supply voltage range will cause unreliable USB operation.

## 3. PCB layout

### 3.1 General considerations

It is important that the USB\_DP and USB\_DM signal traces maintain parallelism on the PCB. Trace lengths for the signals should be matched as closely as possible.

Reducing the number of right-angle corners and the number of vias for the USB signals traces will minimize signal reflections and impedance changes.

### 3.2 Impedance

Although it is recommended to implement 45  $\Omega$  signal traces, for full-speed USB, it is not critical for obtaining good results. Keep your signal traces as short as possible for good performance.

## 4. References

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- [1] USB 2.0 Specification: <http://www.usb.org/developers/docs/>
- [2] Intel High Speed USB Platform Design Guidelines:  
<http://www.usb.org/developers/docs/>



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