



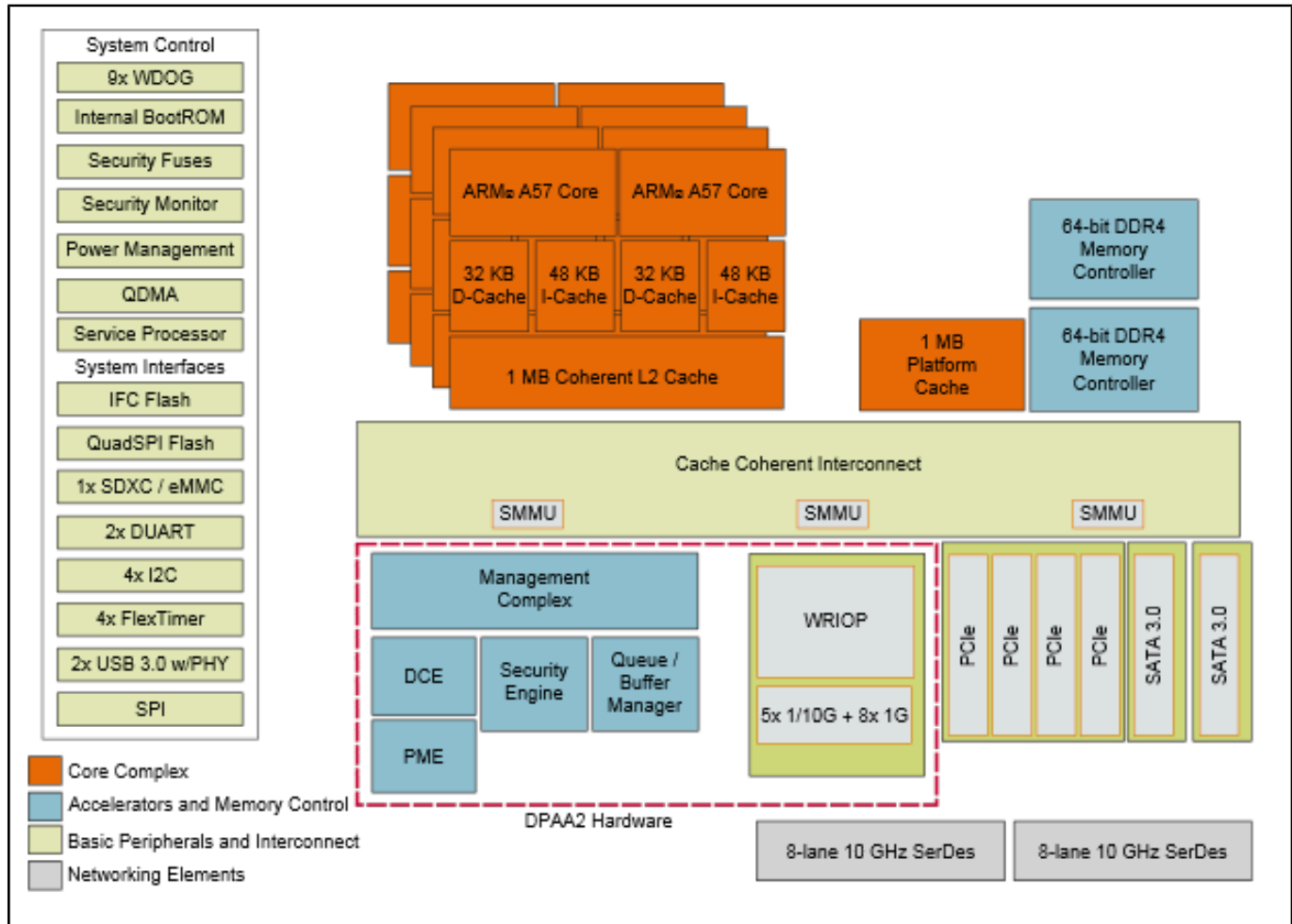
# Second Generation Data Path Acceleration Architecture (DPAA2)

## DPAA2

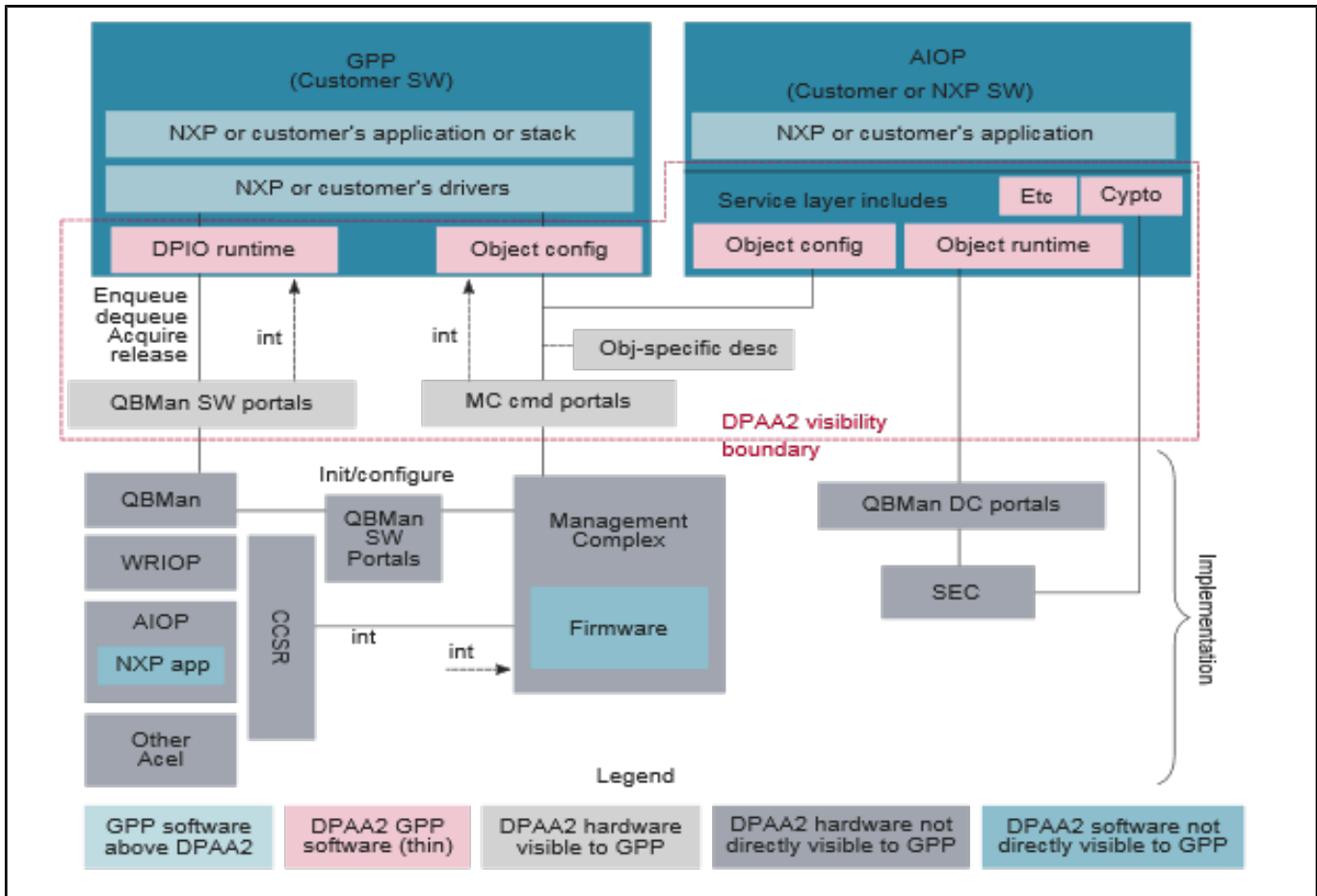
Last Updated: Apr 9, 2022

NXP has integrated data path and packet processing for more than twenty years. Working in concert with the general-purpose processors, DPAA2 enables very high networking performance while executing dynamic network functions: parse and classify, load-steering, network acceleration and multi-level prioritized queuing. The DPAA2 architecture is an evolution and extension of DPAA, taking a more holistic view of the full system architecture; it brings independent and more efficient operation to each level of packet processing.

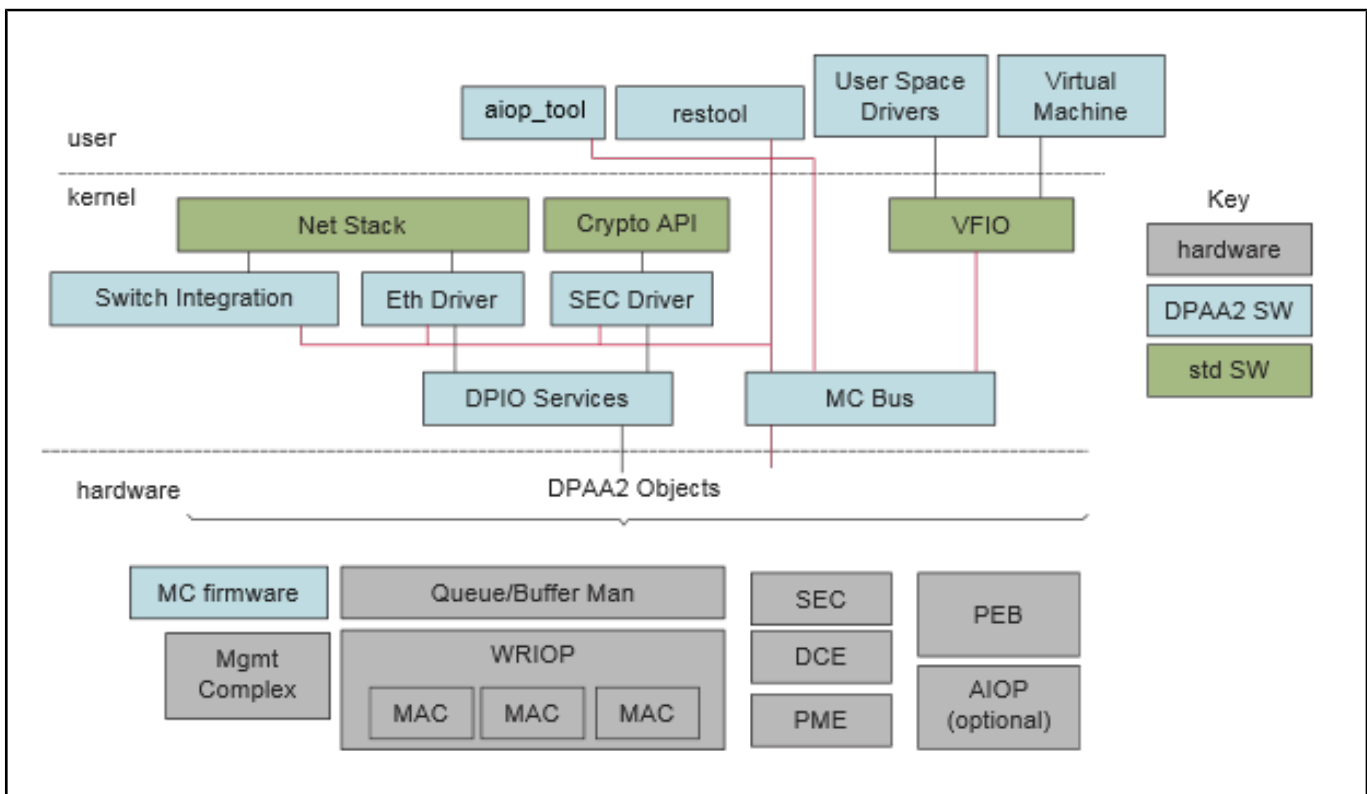
# Layerscape DPAA2 Block Diagram



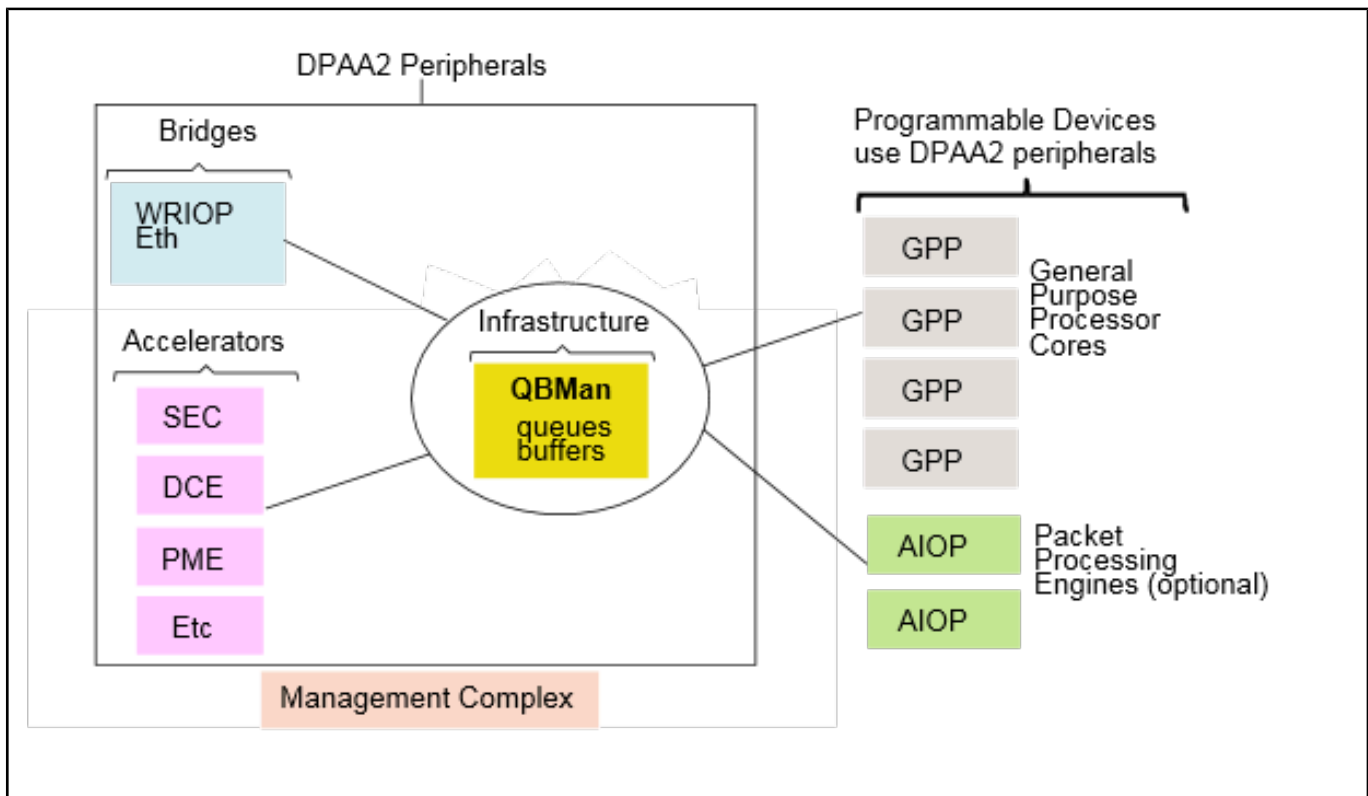
# DPAA2 Visibility Boundary Block Diagram



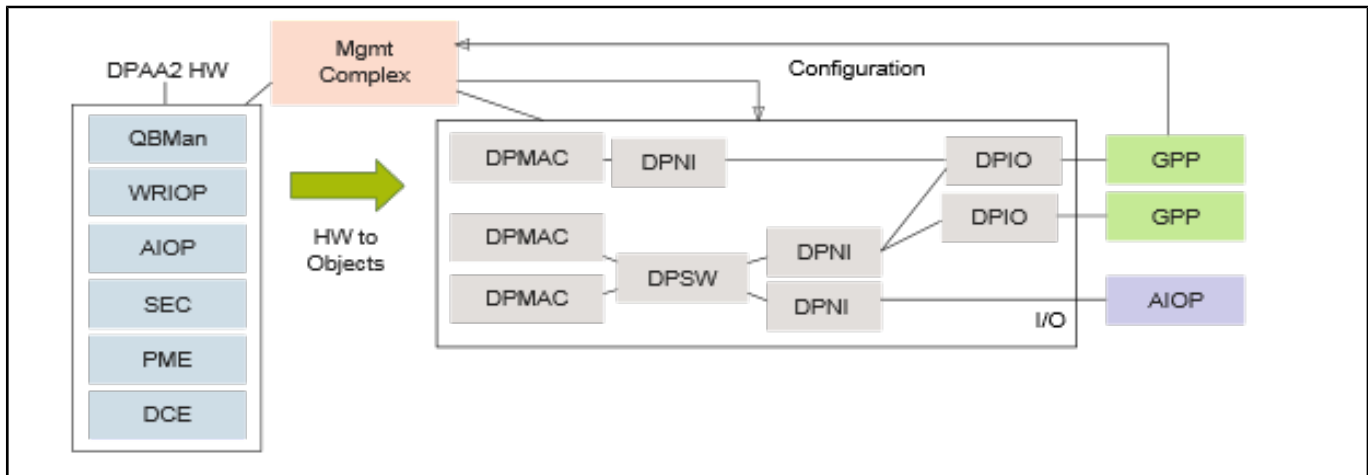
### Linux DPAA2 Software Block Diagram



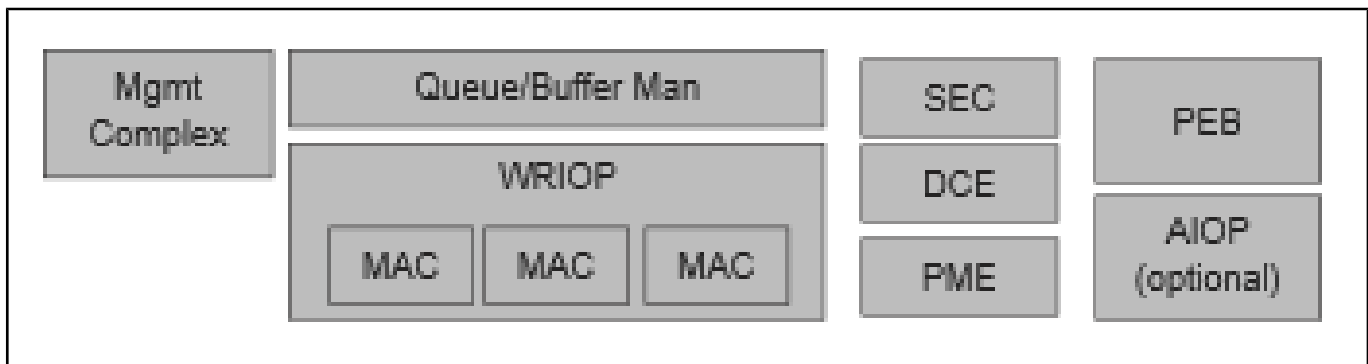
## DPAA2 Hardware Block Diagram



## DPAA Block Diagram Block Diagram



## DPAA2 Hardware Component Block Diagram



View additional information for [Second Generation Data Path Acceleration Architecture \(DPAA2\)](#).

**Note:** The information on this document is subject to change without notice.

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