Dependence of Thermal Resistance on Ambient and Actual Temperature

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ABSTRACT. We investigate the temperature dependence of the thermal resistance. We extract the thermal resistance as function of ambient temperature. The increase of thermal resistance due to self-heating leads to a non-linear relation between temperature and power dissipation. We show how to implement this in a compact model and what its effect is on simulations at high power dissipation.

I Introduction

For several modern processes self-heating becomes increasingly important. For III-V HBT's (e.g., GaAs based) and SOI processes this has always been so, because of the low thermal conductivity of GaAs and silicon-oxide. For modern high-performance SiGe processes the oxide in the deep trenches also increases the self-heating: the heat-flow is in practice confined to the restricted silicon region. For designs in these processes it is therefore paramount to take self-heating into account. Modern compact models are capable of doing this. It is rather surprising, however, that the temperature dependence of the thermal resistance has not yet being taken into account.

It is well-known that the thermal conductivity changes with temperature [1]. For many of the materials used in semiconductor devices the thermal conductivity $\kappa(T)$ as function of temperature T is approximately given as

$$\kappa(T) = \kappa_{\mathrm{ref}} \left(\frac{T}{T_{\mathrm{ref}}} \right)^{-\alpha}, \qquad (1)$$

in the relevant temperature range (e.g., between $-50°C$ and $200°C$). Here κ_{ref} is the thermal conductivity at the reference temperature T_{ref}. The values of κ_{ref} and α for different materials can for instance be found in Ref. [2]. For Si one often sees $\alpha = 4/3$ being used. This means that the thermal conductivity at $125°C$ is about a factor 1.5 lower than at $25°C$. This is quite significant. For GaAs the value is $\alpha = 1.25$. So although the thermal conductivity of Si is much higher than that of GaAs, its temperature dependence is very similar. If, therefore, for a specific device it has been found that self-heating is relevant, then it is also relevant to take the temperature dependence of κ into account.

The thermal resistance is inversely proportional to the thermal conductivity. This means that the temperature behaviour of the thermal resistance can be given as

$$R_{\mathrm{TH}}(T) = R_{\mathrm{TH,ref}} \left(\frac{T}{T_{\mathrm{ref}}} \right)^{\alpha}. \qquad (2)$$

Marsh [3] already showed an increase in thermal impedance with temperature, based on device simulations. Other authors [4, 5, 6] show the increase of the thermal resistance as function of power dissipation at constant ambient, but increasing device temperature. In section II we will present extracted thermal resistances as function of temperature, at such low dissipation that the junction temperature is (almost) equal to the ambient. This enables us to verify Eq. (2) directly.

We then discuss the effect that the temperature increase due to self-heating also increases the thermal resistance. The relation between temperature and power dissipation is then no longer linear, but it becomes non-linear. Expressions to describe this effect have been given in Refs. [7, 8, 9], but no verification versus measurements was performed. This non-linear relation is independent of the precise geometry between the heat source and the heat sink. It is important to realise that this non-linear relation is device independent and therefore valid not only for bipolar transistors, but also for other devices like LDMOS transistors. In Section III we show how to implement this relation in a compact model. We then verify the model against measurements, and show the difference between taking this non-linear dependence into account or not.

II Extraction of thermal resistance

For the extraction of the thermal resistance various methods have been published. Not all of these methods can be used for our work. The method of Ref. [10] is limited to transistors that have such a large thermal resistance that self-heating is already present before high-current effects play a role. It is especially sensitive to emitter resistance if the voltage drop over the emitter resistance becomes comparable to the thermal voltage. The method of Refs [11, 12] combines measurements over a large temperature range to extract a thermal resistance averaged over temperature. This method is therefore not suited for extracting the thermal resistance as function of temperature.

For our work we use the method of Ref. [13]. This method also has the advantage that no fitting to a model is needed, but that the thermal resistance can be determined directly from measurements. We measured the base and collector current as function of collector voltage at a fixed base-emitter voltage for three closely spaced temperatures, $T_{\mathrm{amb}} - \Delta T$, T_{amb}, and $T_{\mathrm{amb}} + \Delta T$. During these three measurements we kept the probes on the pads while changing the temperature, to keep the contact resistance as constant as possible. The thermal resistance for a reference point at collector voltage V_{CE} and ambient temperature T_{amb} is then calculated using [13]

$$R_{\mathrm{TH}} = \frac{\Delta T}{I_C \Delta V_{CE}} \frac{I_B(V_{CE} + \Delta V_{CE}, T_{\mathrm{amb}}) - I_B(V_{CE} - \Delta V_{CE}, T_{\mathrm{amb}})}{I_B(V_{CE}, T_{\mathrm{amb}} + \Delta T) - I_B(V_{CE}, T_{\mathrm{amb}} - \Delta T)}. \qquad (3)$$

The assumption here is that the early voltage V_A is large enough such that $(1 + V_{CE}/V_A) \simeq 1$. Note that in the derivation of Eq. (3) it has been taken into account that the temperature of the transistor is larger than that of the ambient temperature due to self-heating. To reduce the effect of non-linearities in the temperature and collector-voltage dependence of the base and collector currents, we used measurements symmetrically around the reference point $(V_{CE}, T_{\mathrm{amb}})$ in Eq. (3). For the temperature difference we used $\Delta T = 10°C$, which is small enough to prevent large non-linearities and large enough to reduce the effects of the inaccuracies of the thermo-chuck. Furthermore, we used $V_{CE} = 2\,\mathrm{V}$ and
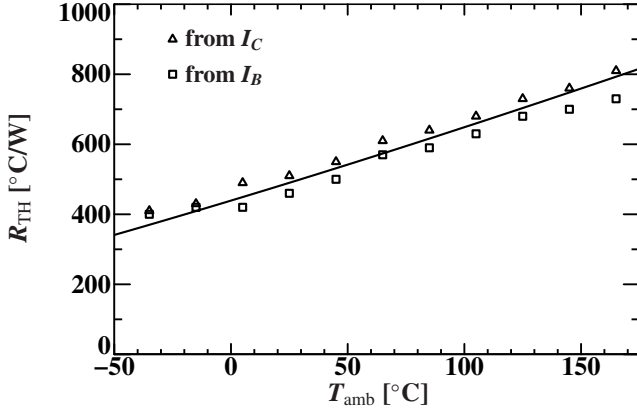
Figure 1: *Extracted thermal resistance R_{TH} for a GaAs transistor as function of ambient temperature. Both the values extracted from collector current measurements and base current measurements are shown. The line is according to Eq. (2) with $R_{\mathrm{TH}} = 490°C/W$ for $T_{\mathrm{amb}} = 25°C$ and with $\alpha = 1.25$.*

$\Delta V_{CE} = 0.2$ V. We found that the results are not sensitive to either V_{CE} or ΔV_{CE} (outside the hard-saturation and avalanche regions). A similar expression as Eq. (3) can be used to calculate the thermal resistance from the collector current only, although the influence of the Early voltage is larger.

We repeated the procedure for different ambient temperatures. To keep the current level approximately constant for the different ambient temperatures we decreased V_{BE} by 25 mV for every 20°C temperature increase. The collector current is then around 2 mA. Given the extracted thermal resistance, the increase in temperature due to self-heating is only a few degrees, which means that the extracted thermal resistance equals that at the temperature T_{amb}.

In Fig. 1 we show the extracted thermal resistance. We used a GaAs-based HBT, with an emitter area of 4 times $2 \times 20\,\mu\mathrm{m}^2$. We both show the result extracted from the base current, as well as that extracted from the collector current. The reason for the slight difference between the two methods is unclear. The line is the result based on Eq. (2) with the GaAs value $\alpha = 1.25$. As one can see, the thermal resistance increase is predicted quite nicely.

We have repeated the same kind of measurements for a SiGe device. The results are more noisy. Nevertheless, the increase in thermal resistance can also be clearly seen. The relative increase in thermal resistance in SiGe is of the same order as that of GaAs.

III Self-heating of thermal resistance

We showed that the increase in thermal resistance due to the increase in ambient temperature T_{amb} is quite large. Due to self-heating, the transistor itself has an even higher temperature T than the ambient temperature. This increases the thermal resistance even more. We now discuss this effect in detail.

III.1 Theory

We define the thermal resistance as the ratio between temperature increase and dissipation, writing

$$\Delta T = P_{\mathrm{diss}} R_{\mathrm{TH}}. \tag{4}$$

As mentioned above, the thermal resistance R_{TH} is larger than the thermal resistance at ambient temperature $R_{\mathrm{TH,amb}}$, defined as the low-dissipation limit of $\Delta T/P_{\mathrm{diss}}$. (For the temperature depen-

dence of $R_{\mathrm{TH,amb}}$ one can use Eq. (2).) To find the resulting temperature increase it is incorrect to solve the self-consistent relation

$$\Delta T = P_{\mathrm{diss}} R_{\mathrm{TH,amb}} \left(\frac{T_{\mathrm{amb}} + \Delta T}{T_{\mathrm{amb}}} \right)^{\alpha}, \tag{5}$$

found from Eqs (2) and (4). Whereas the behaviour of the transistor is determined by the temperature T at the junction, the thermal resistance is determined by the distribution of the thermal conductance in the whole heat-flow region between junction and the heat-sink (which is at ambient temperature). Since the average temperature in the heat-flow region is somewhere in-between T_{amb} and T the thermal conductance is position dependent (via the position dependence of the temperature) and the increase in thermal resistance is less than what can be found from Eq. (5).

In practice it is impossible to calculate the heat flow in the device and therefore the precise temperature distribution is also not known. Fortunately, it *is* possible to calculate the increase in temperature at the junction at high dissipation if the increase at low dissipation is known, as was shown in Refs. [7, 8]. Whereas the differential equations that describe the heat flow are non-linear in terms of T, they become linear in terms of a pseudo-temperature τ, defined as

$$\tau = T_{\mathrm{amb}} + \frac{1}{\kappa(T_{\mathrm{amb}})} \int_{T_{\mathrm{amb}}}^{T} \kappa(T')dT'. \tag{6}$$

Due to the linearity of the equations, the increase in pseudo-temperature $\Delta\tau$ is proportional to the dissipated power. It can therefore be given in terms of the low-dissipation thermal resistance as: $\Delta\tau = P_{\mathrm{diss}} R_{\mathrm{TH,amb}}$. The real temperature increase ΔT can then be calculated from the increase in pseudo-temperature $\Delta\tau$. The result is

$$\Delta T = T_{\mathrm{amb}} \left[\left(1 + \frac{(1-\alpha)P_{\mathrm{diss}} R_{\mathrm{TH,amb}}}{T_{\mathrm{amb}}} \right)^{\frac{1}{1-\alpha}} - 1 \right], \tag{7}$$

as given in Refs [8, 14]. In Ref. [9] a generalisation of Eq. (7) was given that takes the thermal resistance of the package into account. The expression (7) is valid for all geometries. Similar equations for specific geometries where already given in Ref. [15]. Below we will show how to implement Eq. (7) in a circuit simulator and compare simulation results with measurements.

The thermal resistance can be found from Eq. (7) as $R_{\mathrm{TH}} = \Delta T/P_{\mathrm{diss}}$. Note that indeed, for low dissipation, $R_{\mathrm{TH}} \to R_{\mathrm{TH,amb}}$.

An assumption of the derivation of Eq. (7) is that the temperature dependence of the thermal conductivity is uniform. This restriction is not very severe. In modern SiGe processes the thermal resistance is increased due to the use of shallow and deep trenches filled with silicon-oxide, but the heat-flow is still dominantly in silicon. It is therefore the temperature dependence of the thermal conductivity of silicon that is relevant. In contrast, for many SOI processes the transistor is completely surrounded by oxide. In that case the thermal resistance is dominated by the heat-flow through the oxide and hence the temperature dependence of the thermal conductivity of the oxide, which is smaller than that of Si [1].

III.2 Implementation into a circuit simulator

For the implementation of the increase of the thermal resistance due to self-heating, we first must make a distinction between the power P_{diss} that is dissipated by the transistor and the power P_{flow} that flows to the heat-sink driven by a temperature difference. In
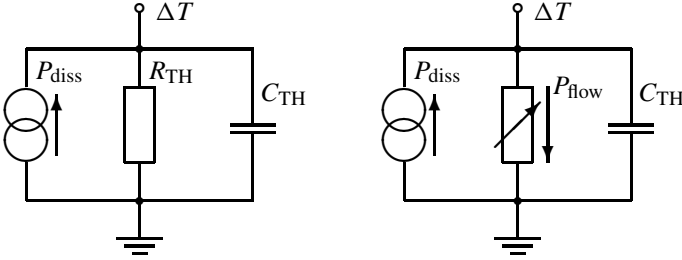
Figure 2: *Equivalent circuit used for simulating self-heating. On the left the standard circuit with constant thermal resistance R_{TH} (although the thermal resistance can depend on the ambient temperature). On the right the circuit where the thermal resistance is replaced by the power in the heat-flow P_{flow} which is implemented as a non-linear resistor. The controlling 'voltage' is ΔT, the 'current' is given by Eq. (9).*

a static situation both are equal when no external power—e.g. due to the dissipation in other transistors—is being supplied. For dynamic situations the P_{diss} can change very rapidly, whereas the P_{flow} follows the slower change in ΔT. In general situations, therefore, the expressions for ΔT given above should be in terms of P_{flow}, instead of P_{diss}.

Consider Fig. 2. On the left we show the situation for small dissipation, or rather small temperature increase. The power being removed by the heat-flow is modelled with a constant thermal resistance:

$$P_{\text{flow}} = \frac{\Delta T}{R_{\text{TH}}}. \tag{8}$$

For larger temperature increase we must take the increase in thermal resistance into account. The expression for P_{flow} can then be found as the inverse of Eq. (7):

$$P_{\text{flow}} = \frac{T_{\text{amb}}}{R_{\text{TH,amb}}(1 - \alpha)} \left[\left(\frac{T_{\text{amb}} + \Delta T}{T_{\text{amb}}} \right)^{1-\alpha} - 1 \right]. \tag{9}$$

Since now the power P_{flow} is a non-linear function of the temperature increase, we implement it as a non-linear resistance, as shown in the right of Fig. 2. Note that we regain Eq. (8) in the limit $\Delta T \to 0$.

In existing compact models the left circuit in Fig. 2 is hardcoded, and can not be changed by the user. Nevertheless, it is possible to simulate the effects by using a self-defined external thermal circuit, as shown in in Fig. 3. The power P_{flow} is then implemented in a sub-circuit and connected to the thermal node of the hard coded model (here the node ΔT).
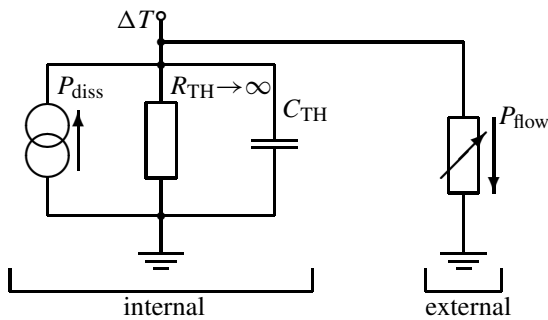

Figure 3: *Equivalent circuit used for simulating the right circuit in Fig. 2 when using a hard-coded existing compact model (internal part). P_{flow} (external part) is added in a sub-circuit.*
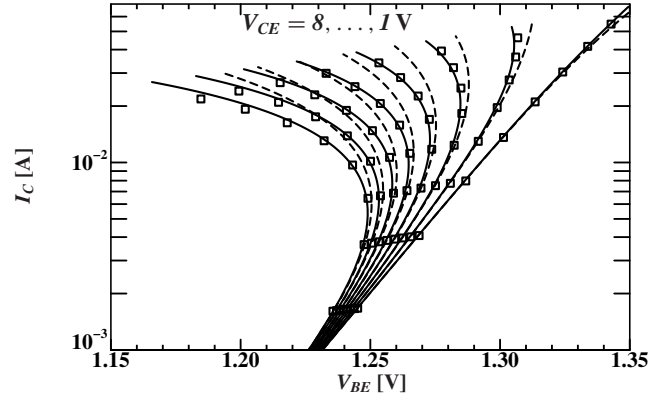

Figure 4: *Gummel plot for a GaAs transistor at 8 different collector-emitter voltages from 1 to 8 V (right to left) at $T_{\text{amb}} = 21°C$. Markers are measurements. Dashed lines are without increased thermal resistance ($\alpha = 0$). Solid lines are with increased thermal resistance according to Eq. (7) with $\alpha = 1.25$.*

III.3   Experimental results

In Fig. 4 we show the I_C-V_{BE} characteristic of the GaAs transistor used also in Section II. In these measurements the base current was swept at different values of V_{CE}. We also show simulations. The dashed lines show the simulation result found for constant thermal resistance, as in the left circuit of Fig. 2. The solid lines use the non-linear relation between dissipation and temperature increase. We simulated this as in Fig. 3 with P_{flow} from Eq. (9). The thermal resistance at low dissipation was the same for both simulations. Note that the extraction of the thermal resistance as presented in Section II was done at collector current levels around $2\,\text{mA}$ ($V_{BE} = 1.25\,\text{V}$), where there is still no significant difference between the two simulation results.

We have also measured output characteristics. In Fig. 5 we show the base-emitter voltage at constant base current. In Fig. 6 we show the corresponding collector current. It is well-known that for GaAs devices the collector current decreases with collector voltage due to self-heating. Here we show that for larger currents and voltages one needs to take into account the increase of the thermal resistance with power dissipation for a correct description of the collector current and base-emitter voltage.
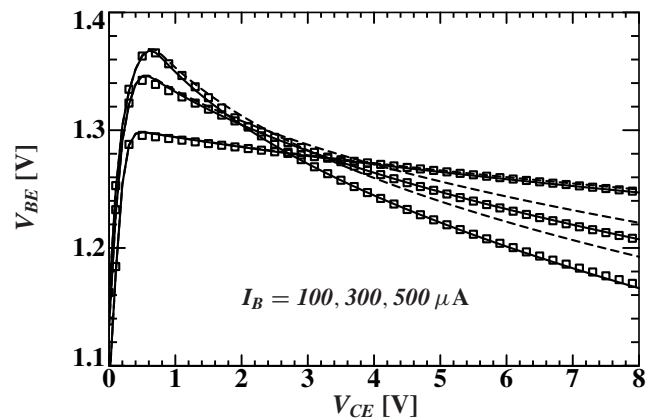

Figure 5: *V_{BE} versus V_{CE} for $I_B = 100$, 300, and $500\,\mu\text{A}$. Symbols and lines are as in Fig. 4. For the lowest I_B the solid and dashed lines are almost on top of each other for all values of V_{CE}.*
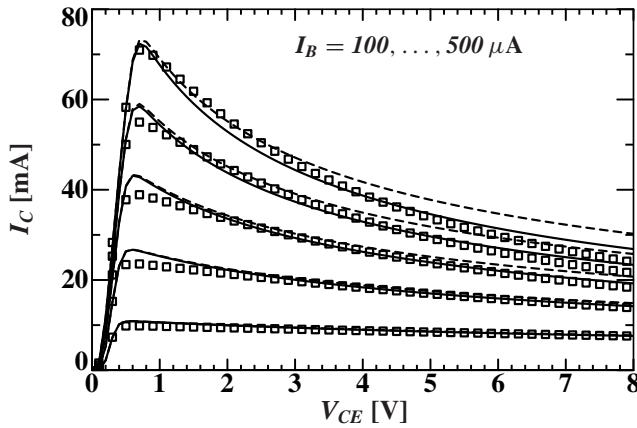
Figure 6: *I_C versus V_{CE} for $I_B = 100, 200, 300, 400$ and $500\,\mu$A. Symbols and lines are as in Fig. 4.*

Figure 7: *Collector current and base-emitter voltage at the snap-back point, as function of collector voltage. Markers are from measurements, see Fig. 4. Solid lines take increased self-heating into account. Dotted (for V_{BE}) and dashed (for I_C) lines do not.*

III.4 Thermal runaway

In Eq. (9) we have given the power that is being removed to the heat-sink. This power increases with temperature difference ΔT. When $\alpha > 1$, as in many semiconductor materials, the amount of power that can be removed has a maximum for $\Delta T \to \infty$:

$$P_{\text{flow,max}} = \frac{T_{\text{amb}}}{R_{\text{TH,amb}}(\alpha - 1)}. \quad (10)$$

This means that if the dissipated power is larger than this maximum removable power, the device will keep on increasing in temperature. The result is thermal runaway and burnout of the device [15, 16]. This can also be observed in the temperature increase found in Eq. (7), which becomes meaningless if the term between brackets becomes negative, i.e. when $P_{\text{diss}} > P_{\text{flow,max}}$.

In practice this kind of thermal runaway will not happen by itself. The dissipation has to be so large that even with a constant thermal conductivity the temperature would already reach

$$R_{\text{TH,amb}} P_{\text{flow,max}} = \frac{T_{\text{amb}}}{(\alpha - 1)}. \quad (11)$$

For Si $\alpha = 4/3$, which means that at an ambient temperature of $T_{\text{amb}} = 300\,$K this temperature increase would be 900 K. For GaAs, where $\alpha = 1.25$, it would even reach $T_{\text{junc}} = 1200\,$K. These large increases in temperature normally do not occur.

Although the effect described here is in practice not large enough to cause thermal runaway by itself, it does increase the thermal runaway one has due to other effects, like the increase of current with temperature [16]. This can, for instance, be observed in Fig. 4, where the snap-back point moves to lower values of V_{BE} and I_C. In Fig. 7 we give both the collector current and base-emitter voltage at those snapback points. The collector current shown is often taken as the maximal allowable current. We show that it decreases due to the increase in thermal resistance with self-heating. The difference is especially large at low V_{CE}.

IV Conclusions

We have reported for the first time the extraction of the thermal resistance as function of the ambient temperature. The change of thermal resistance with temperature is quite large, changing by more than a factor of 2 over the temperature range $-50°$C to $200°$C, as is expected from the change in thermal conductivity with temperature. For circuits containing devices with considerable self-heating this can have a large effect on circuit simulations
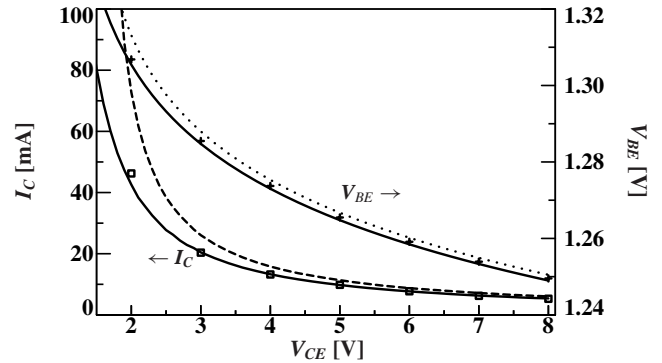
that are regularly done at elevated or decreased temperatures. This important effect has not yet been implemented in compact models.

The increase of thermal resistance is not only due to the increase of the ambient temperature, but also due to self-heating. This leads to a non-linear relation between temperature increase and dissipation, in terms of the low-dissipation thermal resistance at the ambient temperature. This non-linear relation is independent of the device or technology and can therefore also be used for LD-MOS transistors, etc. We have shown how to simulate this effect using existing compact model implementations. We then showed that for a correct description of the measurements at high dissipation one needs to take the effect into account in the simulations.

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