

# X-S32K148EVBQ144/Q176

## CUSTOMER EVB

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Revisions				
Rev	Description	Designer	Date	Approved
X4	Schematic	J.Sanchez		TBD
A	Prototype			
AX1	First Release			

### CAUTION:

This schematic is provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP S32K family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

TPV?

TPH5

TP?


### Notes:

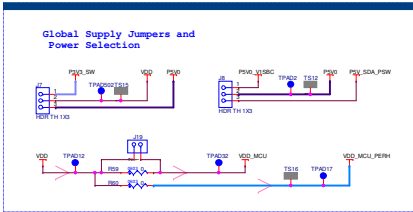
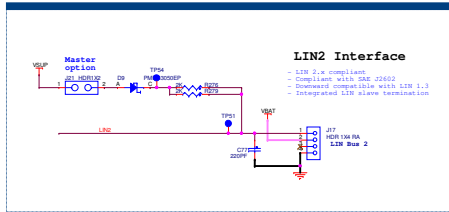
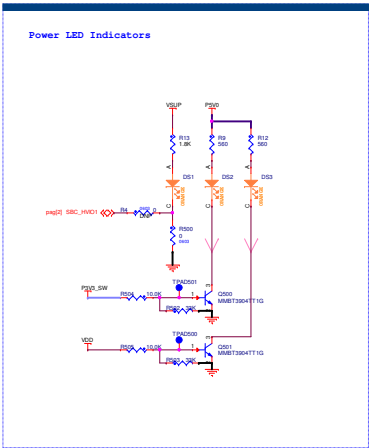
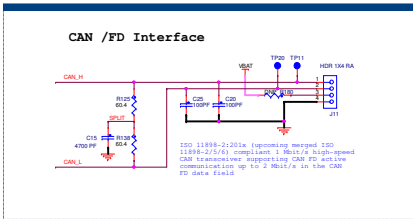
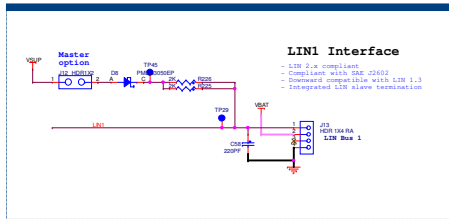
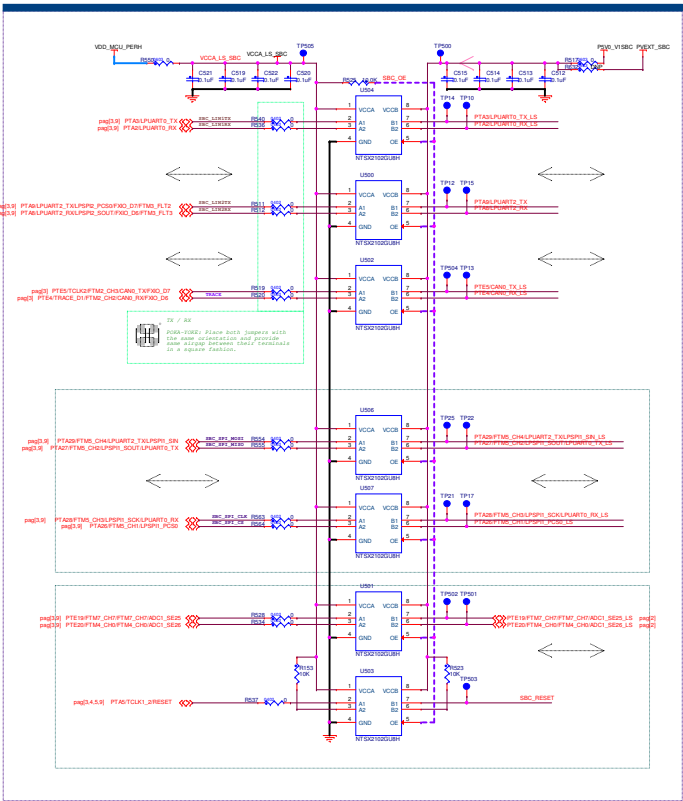
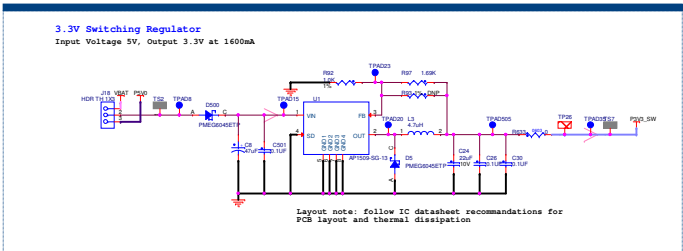
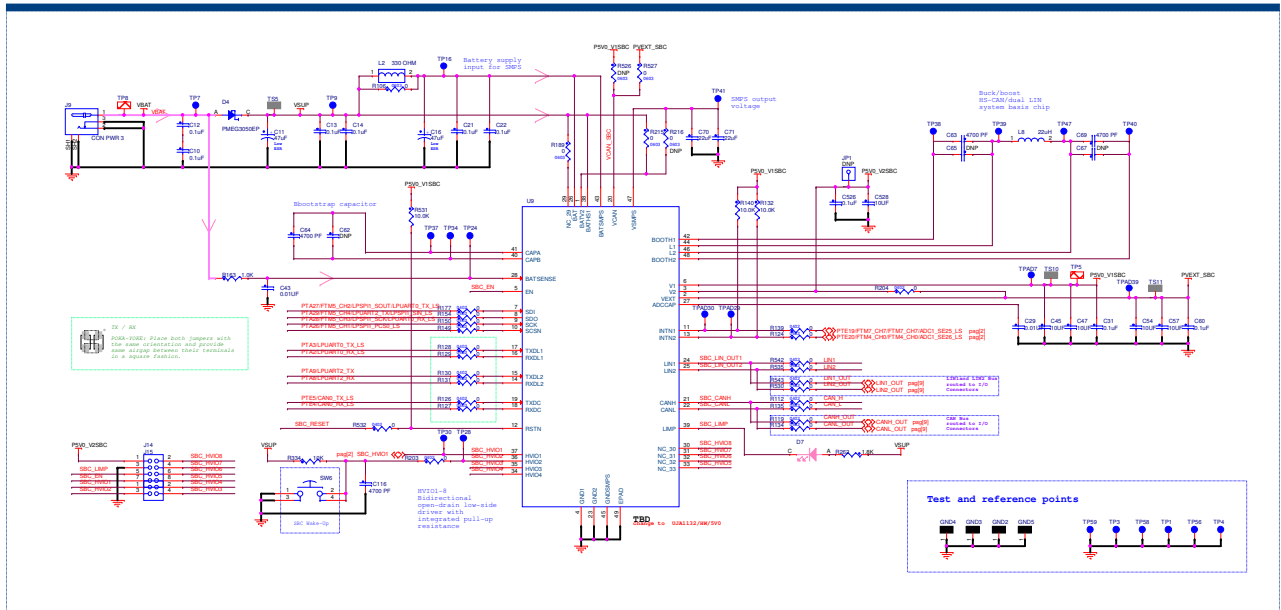
- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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Drawn by: Jesus Sanchez		Page Title: <b>TITLE</b>	
Approved: Juan Romero		Size B	Document Number SCH-29642 PDF: SPF-29642
Date: Wednesday, July 12, 2017		Sheet 1	Rev A
of 11			

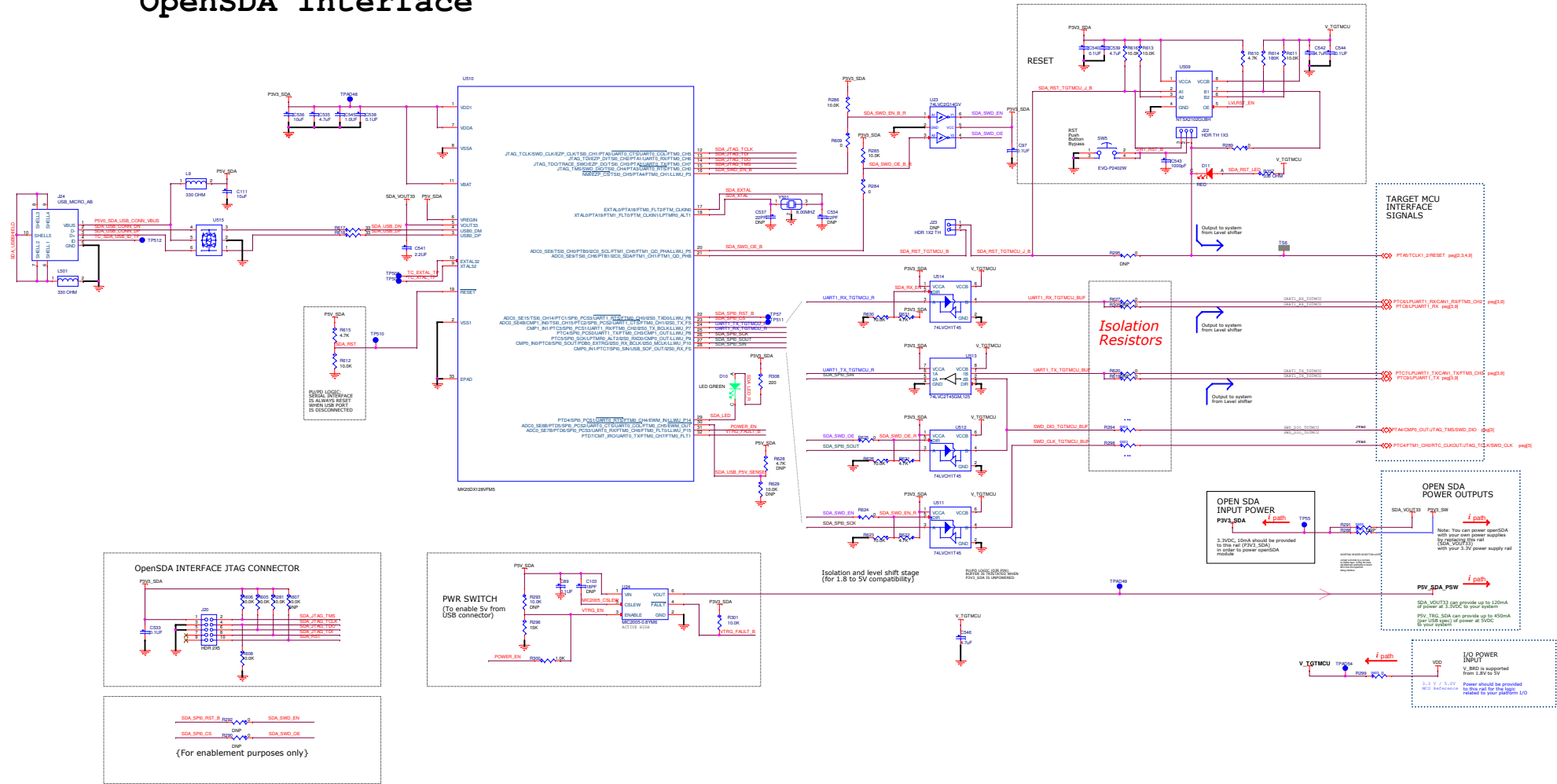


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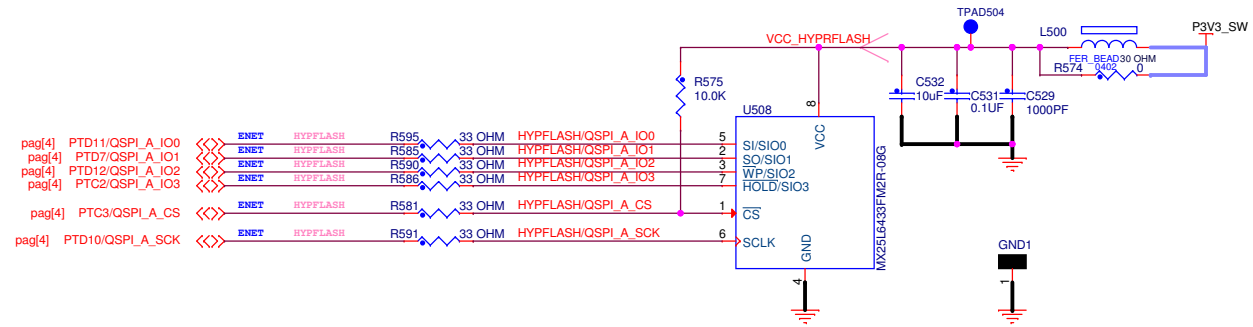
# OpenSDA Interface



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# CMOS FLASH Memory 64M-BIT



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Approved: <Approver>		Size B	Document Number SCH-29642 PDF: SPF-29642
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**SAI Audio**

Microcontroller Pin	Signal	Connector Pin
pag[3,9] PTA14/FTM0_FLT0/FTM3_FLT1/SAI0_D3	SAI0_DATA3	1
pag[3,9] PTE0/LPSPI0_SCK/TCLK1/LP2C1_SDA/SAI0_D2	SAI0_DATA2	3
pag[3,9] PTE1/LPSPI0_SIN/LP2C0_HREQ/LP2C1_SCL/SAI0_D1	SAI0_DATA1	5
pag[3,9] PTA13/FTM1_CH7/FTM2_QD_PHA/SAI0_D0	SAI0_DATA0	7
pag[3,9] PTA12/FTM1_CH6/CAN1_RX/LP2C1_SDAS/SAI0_BCLK	SAI0_BCLK	9
pag[3,9] PTA11/FTM1_CH5/FXIO_D1/CMP0_RRT/SAI0_SYNC	SAI0_SYNC	11
pag[3,9] PTD1/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/SAI0_MCLK	SAI0_MCLK	13
pag[3,9] PTD14/FTM2_CH5/LPUART1_TX/ENET_TMR0/CLKOUT	ENET0_TMR0	15
pag[3,9] PTD18/FTM5_CH7/FXIO_D2/LP2C1_SCL/ADC1_SE16	ENET0_TMR0	17
pag[3,9] PTC30/FTM5_CH4/FXIO_D0/LP2C1_SDAS/FXIO_D0/ADC0_SE30	ENET0_TMR0	19
pag[3,6,9] PTB9/FTM3_CH1/LP2C0_SCL	ENET0_TMR0	21
pag[3,9] PTB8/FTM3_CH0/SAI1_BCLK	ENET0_TMR0	23
pag[3,9] PTD13/FTM2_CH4/LPUART1_RX/ENET_TMR1/RTC_CLKOUT	ENET0_TMR0	25
pag[3,9] PTE2/LPSPI0_SOUT/FTM3_CH6/SAI1_SYNC/ADC1_SE10	ENET0_TMR0	27
pag[3,6,9] PTB10/FTM3_CH2/LP2C0_SDAS	ENET0_TMR0	29
pag[3,9] PTD19/FTM6_CH0/FXIO_D3/LP2C1_SCL/ADC1_SE17	ENET0_TMR0	31
pag[3,9] PTC31/FTM5_CH6/FXIO_D1/LP2C1_SDA/FXIO_D1/ADC0_SE31	ENET0_TMR0	33
pag[3,9] PTE15/LPSPI2_SCK/FTM2_CH6/FTM4_FLT1/FXIO_D2	ENET0_TMR0	35
pag[3,9] PTE16/LPSPI2_SIN/FTM2_CH7/FTM4_FLT0/FXIO_D3	ENET0_TMR0	37
pag[3,6,9] PTE10/CLKOUT/LPSPI2_PCS1/FTM2_CH4/FXIO_D4	ENET0_TMR0	39
pag[3,9] PTD15/FTM0_CH0/TRACE_D3/LPSPI0_SCK/ENET_TMR2	ENET0_TMR0	41
pag[3,9] PTE9/FTM0_CH7/LPUART2_CTS/ENET_TMR3	ENET0_TMR0	43

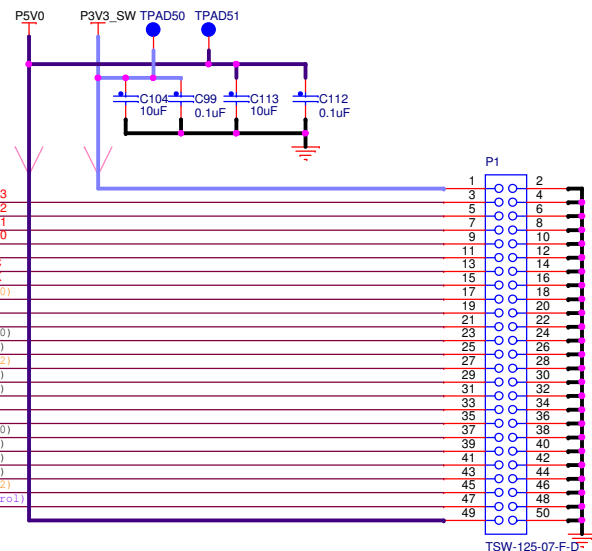
**Physical Schematic:**


The diagram shows a multi-pin connector P1 with 50 pins. The internal wiring is as follows:

- Pin 1: SAI0\_DATA3
- Pin 3: SAI0\_DATA2
- Pin 5: SAI0\_DATA1
- Pin 7: SAI0\_DATA0
- Pin 9: SAI0\_BCLK
- Pin 11: SAI0\_SYNC
- Pin 13: SAI0\_MCLK
- Pin 15: ENET0\_TMR0
- Pin 17: ENET0\_TMR0
- Pin 19: ENET0\_TMR0
- Pin 21: ENET0\_TMR0
- Pin 23: ENET0\_TMR0
- Pin 25: ENET0\_TMR0
- Pin 27: ENET0\_TMR0
- Pin 29: ENET0\_TMR0
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- Pin 39: ENET0\_TMR0
- Pin 41: ENET0\_TMR0
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- Pin 45: ENET0\_TMR0
- Pin 47: ENET0\_TMR0
- Pin 49: ENET0\_TMR0

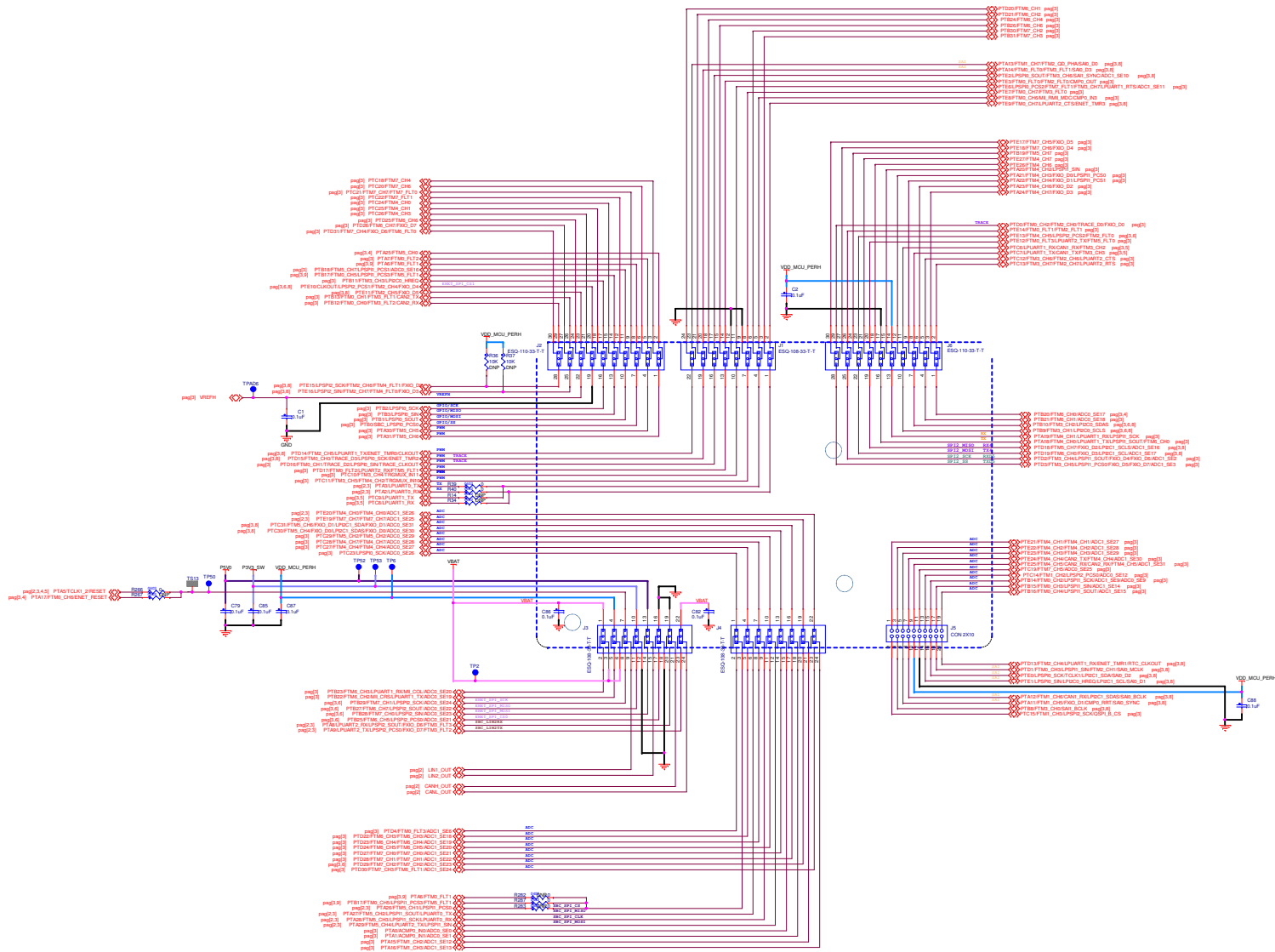
Capacitors: C104 (10uF), C99 (0.1uF), C113 (10uF), C112 (0.1uF).


TSW-125-07-F-D

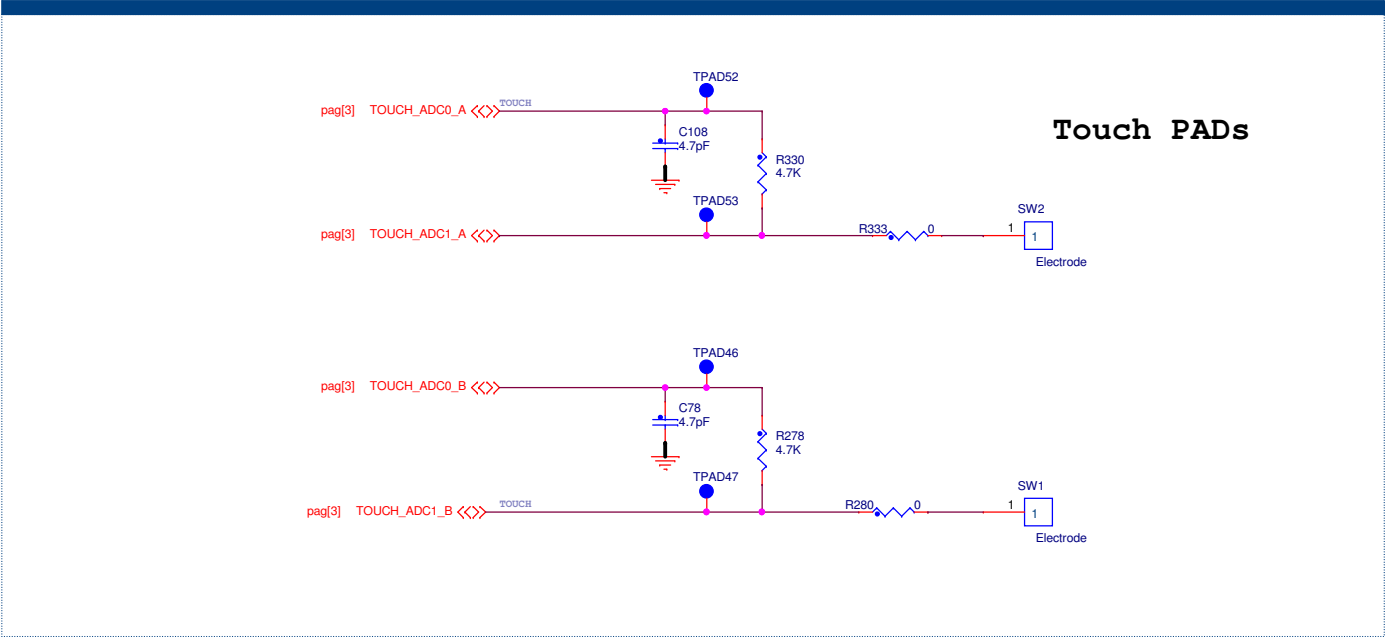


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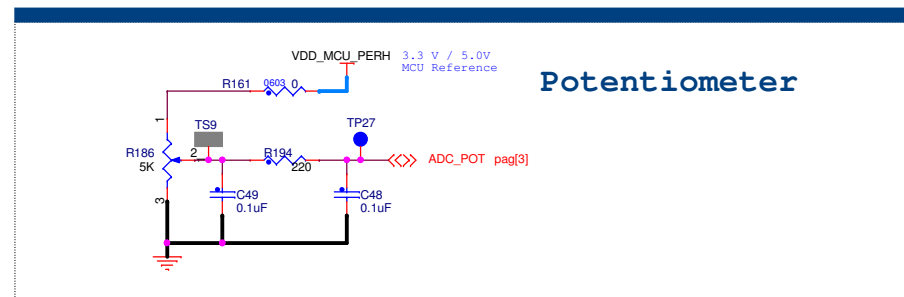
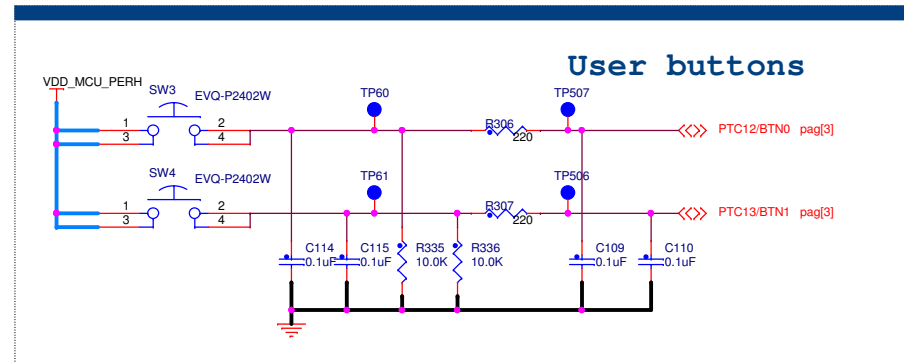
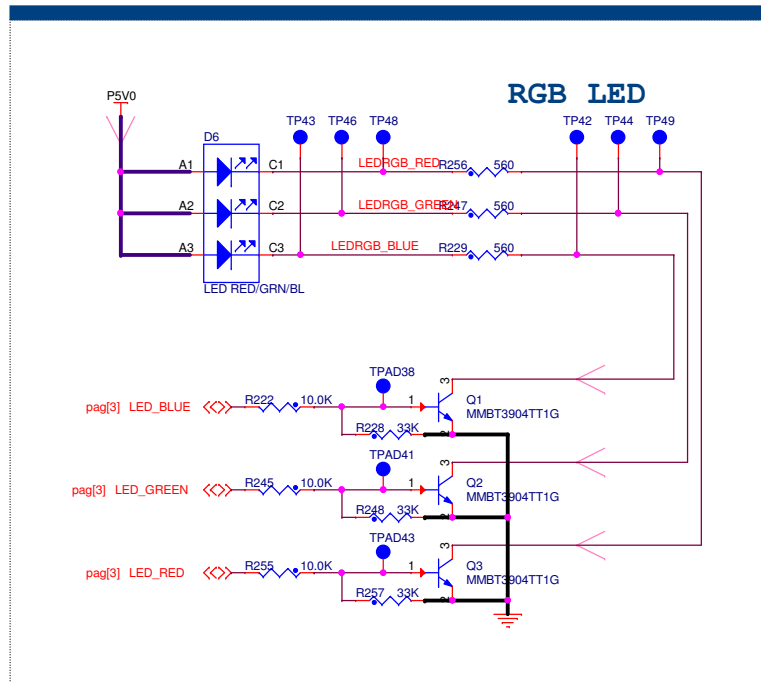





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Approved: Juan Romero		Size B	Document Number SCH-29642 PDF: SPF-29642
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