AN11080

Using SPIFI on LPC1850 Rev '-'

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Document information

Info	Content
Keywords	LPC1857FET256, LPC1837FET256, LPC1827FET100, LPC1825FET100, LPC1823FET100, LPC1822FET100, LPC1817FET100, LPC1815FET100, LPC1813FET100, LPC1811FET100, LPC1800, SPIFI, SPI Flash Interface
Abstract	This application note describes how to develop a SPI Flash secondary bootloader for the LPC1800 family, rev ‘-‘ version.

Revision history

Rev	Date	Description
1	20110701	Initial version.

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1. Introduction

This application note describes how to write a SPI Flash secondary bootloader for the LPC1800 series, rev '-' parts using the SPI Flash Interface (SPIFI) peripheral. The LPC1800, rev '-', contains a basic SPIFI implementation that does not support execution-in-place. However, it is still possible to use the SPI Flash Interface (SPIFI) to load a boot program into the LPC1800 which can read additional code from SPIFI and start a main program or implement overlays. Using the SPIFI peripheral in combination with SPI Flash or QSPI Flash is a viable replacement for external NAND and NOR flash memory and can save board space. With the SPIFI controller's integrated cache memory, code execution-in-place could run as fast as 65 % to 70 % the speed of internal flash memory and could beat performance of 16-bit external nor flash. Ease-of-use is improved over NAND memory as serial flash maps directly into the processor's memory space and does not require use of a flash filesystem or wear leveling.

1.1 System setup

The software included with this application note was built with the Keil uVision IDE and runs on the LPC1850 board from Hitex which includes a Winbond quad SPI flash. The part on the board is the Winbond W25Q80BVS1G1004 which is an 8 Mb quad-SPI flash memory. Other single and quad-SPI flash memories from other vendors can be used but have not been tested on the Rev. '-' LPC1800 silicon. On the LPC1800 and LPC4300 rev. 'A' silicon, the tested-and-supported devices list is expected to include 95 devices from 11 manufacturers. A preliminary version of this list is printed below:

Table 1. Supported SPI flash parts for Rev. 'A' silicon (preliminary)

Manufacturer	Part Numbers
AMIC	A25L512, A25L010, A25L020, A25L040, A25L080, A25L016, A25L032, A25LQ032
Atmel	AT25F512B, AT25DF021, AT25DF041A, AT25DF081A, AT25DF161, AT25DQ161, AT25DF321A, AT25DF641
Chingis	Pm25LD256, Pm25LD512, Pm25LD010, Pm25LD020, Pm25LD040, Pm25LQ032
Elite (ESMT)	F25L08P, F25L16P, F25L32P, F25L32Q
Eon	EN25F10, EN25F20, EN25F40, EN25Q40, EN25F80, EN25Q80, EN25QH16, EN25Q32, EN25Q64, EN25Q128
Gigadevice	GD25Q512, GD25Q10, GD25Q20, GD25Q40, GD25Q80, GD25Q16, GD25Q32, GD25Q64
Macronix	MX25L8006, MX25L8035, MX25L8036, MX25U8035, MX25L1606, MX25L1633, MX25L1635, MX25L1636, MX25U1635, MX25L3206, MX25L3235, MX25L3236, MX25U3235, MX25L6436, MX25L6445, MX25L6465, MX25L12836, MX25L12845, MX25L12865, MX25L25635, MX25L25735
Numonyx	M25P10, M25P20, M25P40, M25P80, M25PX80, M25P16, M25PX16, M25P32, M25PX32, M25P64, M25PX64, N25Q032, N25Q064, N25Q128
Spansion	S25FL004K, S25FL008K, S25FL016K, S25FL032K, S25FL032P, S25FL064K, S25FL064P, S25FL129P
SST	SST26VF016, SST26VF032, SST25VF064
Winbond	W25Q40, W25Q80, W25Q16, W25Q32, W25Q64

Below is a photo of the Hitex board with the LPC1800 Cortex-M3 microcontroller and Winbond quad SPI flash.

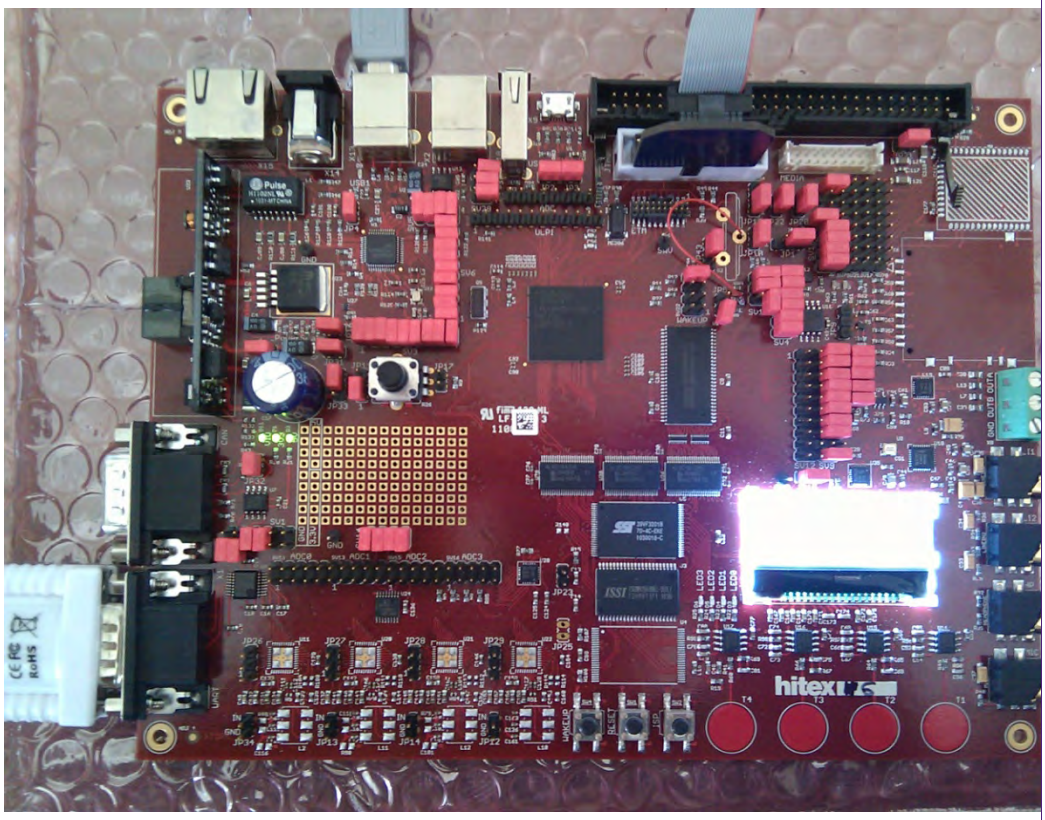

Fig 1. LPC1850 board from Hitex

To connect the demo, a USB cable or DC adapter are required to power the board. A USB-to-serial converter is required to see the output from the demo. A serial program should be connected to the serial port at 115,200 baud with no handshaking, 8 data bits, and 1 stop bit. Finally, a Keil uLink-2 or uLink-Pro should be connected to the connector labeled “X4 JTAG” and plugged into the PC loaded with Keil uVision4 software.

1.2 Board rework

The SPIFI programming portion of this application note can be completed with no changes to the Hitex board. However, to boot from SPIFI, a wire must be added between the right side of R87 and ground. If the EMC must be used in this design, then the wire should be changed to a 1K resistor- this will be enough to set the boot mode without disabling the EMC.

2. Secondary bootloader firmware

The firmware presented in this app note gives a demo of how to implement a secondary bootloader-like loader in the LPC1800 Rev ‘-‘ parts.

2.1 Firmware overview

There is one project included with this app note, which can be compiled either in programmer mode (#define SPIFI_PROGRAMMER 1) or bootloader mode (#define SPIFI_BOOTLOADER 1). Since the programmer project must contain the data from the compilation of the bootloader project, the build must take place in a specific sequence.

Table 2. SPIFI bootloader build steps

Step number	Description
1	Build project with SPIFI_BOOTLOADER defined as 1.
2	Convert build output RAM\spifi_test.bin to spifi_bootloader_image.c file using bin2hex.pl or other conversion tool
3	Edit spifi_bootloader_image.c and add the ROM bootloader header. See spifi_test.c for an example.
4	Build project with SPIFI_PROGRAMMER defined as 1. The programmer project includes the bootloader code by including spifi_bootloader_image.c.

2.2 Firmware block diagram

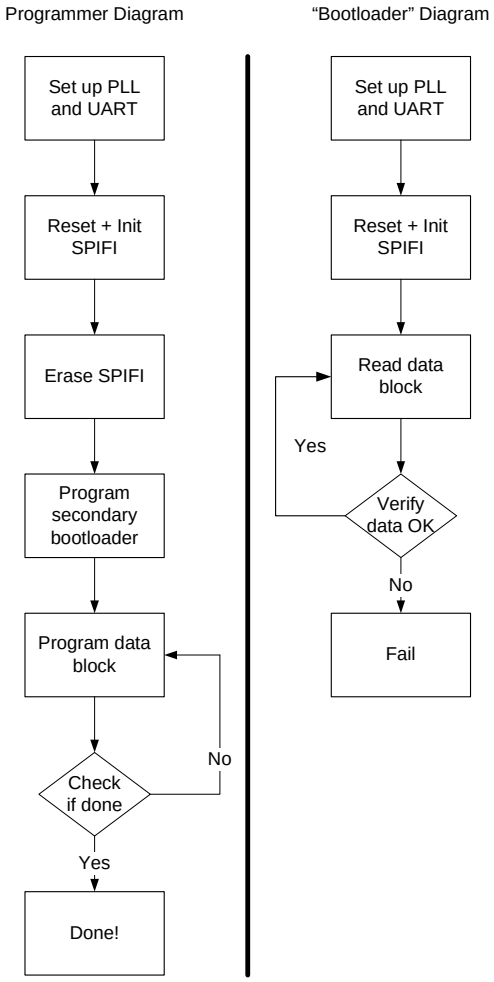

Fig 2. Secondary bootloader block diagram

2.3 Expected output

From the Keil uVision4 IDE, select "Debug Project" on the SPIFI programmer after completing the build steps. The terminal program should show erasing and programming status. After programming is complete, if the board is reset, the terminal program should indicate that the contents of SPIFI are being read and checked. Each time a new block of

4 kB of data is read from SPIFI, it will be checked for correctness and the block number will be printed out in the terminal program using the UART.

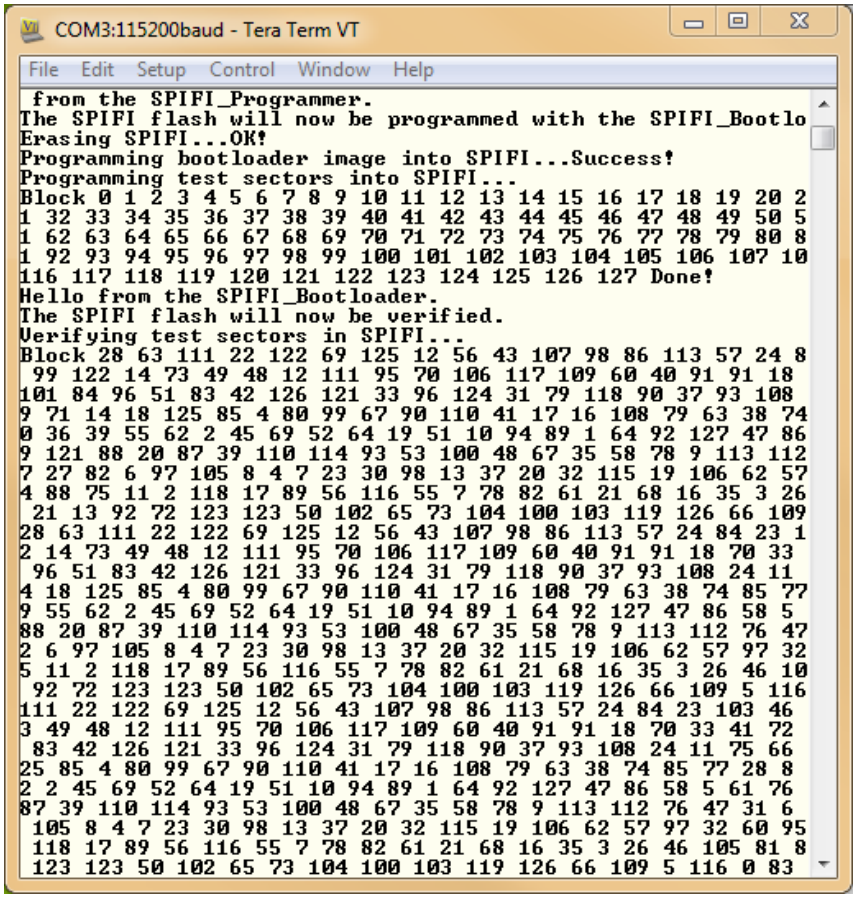

Fig 3. SPIFI programmer and bootloader output

2.4 Conclusion

Despite known errata in the LPC1800 Rev '-' version, the SPIFI peripheral can be used for booting and loading additional data. Recommendations are to ensure that all reads and writes to the SPIFI peripheral consists of large blocks such as 4 kB. Random access should be done with the same size blocks. No byte or half-word operations should be done, only 32-bit words. Execute-in-place is not supported yet and performance does not match what is expected from the Rev. 'A' silicon.

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