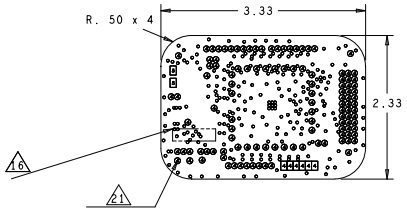
NOTES (UNLESS OTHERWISE SPECIFIED)

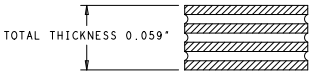
1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
5. CHARACTERISTIC IMPEDANCE - NONE
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .010"/.005"
7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).
8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   BLUE COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
    TYPE: LDI - OR EQUIVALENT.
    A. LOCATION = +/-.001" OF PLATED PADS.
    B. DIAMETER OR SIZE = +/-.001 OF ORIGINAL DATA
11. ELECTRICAL TEST - 100% IPCD356.
12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.
13. DFM CHECK MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
15. TWO SOLDER SAMPLES TO BE PROVIDED.
    - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)
18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.
20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
21. BASIC GRID INCREMENT AT 1.1 IS .0001.
22. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	12-20-17	PAUL.GAN



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
∘	10.0	+0.0/-10.0	PLATED	242
⊗	40.0	+3.0/-3.0	PLATED	116
⊡	41.0	+3.0/-3.0	PLATED	6
⊟	51.0	+3.0/-3.0	PLATED	2

8



FINISHED Cu WEIGHT

LAYER 1	COMPONENT SIDE	1 oz.
LAYER 2	GROUND PLANE	1/2 oz.
LAYER 3	POWER PLANE	1/2 oz.
LAYER 4	SOLDER SIDE	1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

___ COMPANY PUBLIC
X COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN, PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±5-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-29953

APPROVALS	DATE
DRAWN STACY CUI	12-20-17
CHECKED XI .YANG	12-20-17
DESIGN ENGINEER PAUL GAN	12-20-17

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
FRDMCD1020EVM

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-29953	FAB-29953	A

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1