

1 介绍

1.1 概述

LPC553x/LPC55S3x是一个基于Arm Cortex-M33的微控制器，用于嵌入式应用。本文介绍了如何对外部NOR FLASH芯片烧写映像并从它来启动。

LPC553x/LPC55S3x既支持芯片内置FLASH映像启动，也支持外部NOR FLASH映像启动。为了擦除/烧写/读取芯片内置或外部FLASH，可使用ROM，通过ISP接口将启动映像下载到芯片内置和外部FLASH中。ROM也负责启动流程，它决定从片内FLASH、外部FLASH启动，或进入ISP模式。

CMPA/CFPA包含启动相关的参数。要更新设置，请在ISP模式下使用ROM，或在应用程序中使用ROM API。

1.2 存储区布局

图1显示了LPC553x的存储区布局。详情请见LPC553x用户手册（UM）中的附件。

目录

1	介绍	1
1.1	概述	1
1.2	存储区布局	1
1.3	启动选择	2
1.4	启动映像偏移	4
1.5	启动映像头	4
2	通过blhost烧写NOR FLASH（非安全模式）	5
2.1	连接到NOR FLASH	5
2.2	配置FlexSPI NOR FLASH	6
2.3	通过blhost烧写NOR FLASH	6
3	从外部NOR FLASH启动（非安全模式）	9
3.1	FlexSPI NOR FLASH启动映像布局（单个映像）	10
3.2	FlexSPI启动动手示例	10
4	修订历史	13
	法律信息	14



Pos. (KB)		Physical Address	Region / Bus
4096	<unused>	0xFFFF FFFF size = 511.0 MB	Vendor-specific
3585		0xE010 0000	
3585	Private peripheral bus (external) (includes NVIC and SYSTICK timer)	0xE00F FFFF size = 768.0 KB	
3584.25		0xE004 0000	Private peripheral bus
3584.25	Private peripheral bus (internal)	0xE003 FFFF size = 256.0 KB	
3584		0xE000 0000	
3584	<unused>	0xDFFF FFFF size = 2.0 G	External device (S-AHB bus)
1536		0x6000 0000	
1536	<unused>	0x5FFF FFFF size = 511.19 MB	
1024.81		0x400D 0000	
1024.81	AHB peripherals	0x400C FFFF size = 320.0 KB	
1024.5	<unused>	0x4007 FFFF size = 256.0 KB	
1024.25		0x4004 0000	
1024.25	APB slave group 1 (synchronous) (up to 32 slaves of 4 KB each)	0x4003 FFFF size = 128.0 KB	System bus
1024.13		0x4002 0000	
1024.12	APB slave group 0 (synchronous) (up to 32 slaves of 4 KB each)	0x4001 FFFF size = 128.0 KB	
1024		0x4000 0000	
1024	<unused>	0x3FFF FFFF size = 256.0 MB	
768		0x3000 0000	
768	External Quad/Octal Flash (FlexSPI)	0x2FFF FFFF size = 128.0 MB	
640	mirrored from Code space (see 0x0800 0000)	0x2800 0000	
640	<unused>	0x27FF FFFF	
512.11		0x2001 C000	
512.11	Main SRAM SRAMs A thru E) 112 KB (size configurable)	0x2001 BFFF size = 112.0 KB	
512		0x2000 0000	
512	<unused>	0x1FFF FFFF size = 256.0 MB	
256		0x1000 0000	
256	External Quad/Octal Flash (FlexSPI)	0x0FFF FFFF size = 128.0 MB	
128		0x0800 0000	
128	<unused>	0x07FF FFFF size = 63.98 MB	
64.02		0x0400 4000	
64.02	Code SRAM (SRAM X, 16 kB)	0x0400 3FFF size = 16.0 KB	
64		0x0400 0000	
64	<unused>	0x03FF FFFF size = 15.81 MB	Code bus
48.19		0x0303 0000	
48.19	Boot ROM 192 KB	0x0302 FFFF size = 192.0 KB	
48		0x0300 0000	
48	<unused>	0x02FF FFFF size = 47.75 MB	
0.25		0x0004 0000	
0.25	Flash Memory (size configurable)	0x0003 FFFF size = 256.0 KB	
0	Active Interrupt Vectors	0x0000 0000	

图1. LPC553x系列的FLASH存储区布局

1.3 启动选择

ROM有4种启动模式。ROM使用ISP引脚或CMPA配置来选择启动模式，即片内FLASH启动、FlexSPI启动、ISP启动或自动启动模式。更多详情，请参见启动模式和基于ISP引脚的ISP下载模式。

默认的启动源是使用ISP引脚。参见表1中的CMPA -> BOOT_CFG -> DEFAULT_BOOT_SOURCE介绍。

表1. CMPA配置中的默认启动源

CMPA->BOOT_CFG->DEFAULT_BOOT_SOURCE	描述
0	ISP引脚源 (默认)
1	FlexSPI闪存
2	串行ISP启动
3	内部FLASH
4	自动启动, 类似于ISP的自动启动选项

当CMPA->BOOT_CFG->DEFAULT_BOOT_SOURCE=0 (默认) 时, ISP引脚决定启动选项, 如表2中所示。

表2. 基于ISP引脚的启动模式和ISP下载模式

启动模式	ISP1 (PIO0_7)	ISP0 (PIO0_5)	说明
内部FLASH启动	低	低	从内部FLASH启动
ISP启动	低	高	从UART/SPI/I2C/USB等下载映像
FLEXSPI启动	高	低	从外部NOR FLASH启动。
自动启动	高	高	按如下优先级启动: 内部启动 -> 外部NOR FLASH启动 -> 恢复启动 -> ISP模式。

CMPA中的3'位决定ISP下载模式接口。默认情况下, ISP_MODE0-2为3'b0, 即自动ISP模式。在大多数情况下, 不需要修改CMPA中的ISP_MODE位。

表3. 基于DEFAULT_ISP_MODE位的ISP下载模式 (6:4, CMPA中的字0)

ISP启动模式	ISP_MODE_2	ISP_MODE_1	ISP_MODE_0	说明
Auto ISP	0	0	0	LPC553x/LPC55S3x从UART0、I2C1、HS_SPI、USB0-FS 或 CAN 探测活跃的外设。从被探测的外设上下载映像。
USB HID ISP	0	0	1	下载USB0端口的映像。
UART ISP	0	1	0	下载映像。
SPI slave ISP (HS-SPI)	0	1	1	下载映像。
I2C slave ISP	1	0	0	下载映像。
CAN slave ISP1	1	0	1	下载映像。
Disable ISP	1	1	1	禁用ISP模式。

对于每个ISP接口使用的引脚说明，请参见LPC553x的用户手册（UM）。

1.4 启动映像偏移

引导加载程序从启动媒介上指定的偏移查找启动映像。具体请参见表4。

表4. 启动映像偏移

启动媒介	应用程序映像偏移
内部FLASH启动	0x0
FlexSPI NOR FLASH启动	0x1000
SPI 1位NOR恢复启动	0x0

注意

CPU时钟须设置为CMPA字段中指定的启动速度。映像直接从内部FLASH或外部NOR FLASH启动。如果映像从FlexSPI NOR FLASH启动，应用程序不要改变FlexSPI时钟。否则，FlexSPI停止工作，应用程序挂起。

1.5 启动映像头

一旦确定了启动模式（选择为FlexSPI启动），并且在NOR FLASH上有可用的启动映像，ROM引导加载程序就会尝试从NOR FLASH上启动映像。映像的开头应与Arm Cortex标准向量表格式兼容，但它使用了预留的用于特殊ROM定义的位置（0值）。

对于内部FLASH，空间地址基值是0x0000_0000。对于FlexSPI，空间地址基值是0x0800_0000。

表5. 映像头的布局

偏移	字节数	标记	说明
0x00	4	(初始SP)	栈指针。
0x04	4	(初始PC)	第1条执行指令。
0x08	24	(向量表)	Cortex-M33向量表入口。
0x20	4	(映像长度)	映像长度。
0x24	4	(映像类型)	映像类型： <ul style="list-style-type: none"> 0x0000 — 明文映像 0x0002 — 带CRC的明文映像 0x0004 — 带签名的XIP明文映像 0x0005 — 带CRC的XIP明文映像 0x0006 — SB3 文件
0x28	4	offsetToExtendedHeader	验证区块偏移或CRC32校验和。
0x2C	8	(向量表)	
0x34	4	imageExecutionAddress	映像加载地址

续表下一页...

表5. 映像头布局 (续)

偏移	字节大小	标记	说明
0x38	4	(向量表)	

本应用笔记着重介绍最简单的一种：明文映像。在这种模式下，映像类型为0x0000，映像长度为0。

2 通过blhost烧写NOR FLASH (非安全模式)

ROM支持通过FlexSPI接口访问来自不同供应商的各种四线/NOR SPI FLASH芯片。根据位于FLASH芯片上偏移0x400处的FLASH配置块 (FCB)，ROM可采用1位、2位 (双线)、4位 (四线) 或8位 (八线或HyperBus) 模式。

为了正确地使用外部存储器件，请用相应的配置文件启动该器件。如果外部存储器件没有被启动，那么就不能用ROM ISP命令访问它。采用ROM中使用预先分配的存储器标识符 (FCB)，可以启动特定的、已支持的外部存储器件。

FCB位于FLASH芯片的偏移0x400处。它是一个由ROM预先分配的512字节的存储器标识符，描述了外部NOR FLASH的每个细节。Boot ROM利用FCB来获取NOR FLASH的所有信息，并通过FlexSPI配置NOR FLASH。有关FCB的详细信息，请参见LPC553x和LPC55S3x的参考手册中的第13.3.1.1.2章，FlexSPI NOR FLASH启动。

2.1 连接到NOR FLASH

本节介绍了如何使用blhost工具将映像烧写到外部NOR FLASH中，以用于启动。blhost工具使用UART、SPI、I2C和USB HID，通过ROM ISP模式与ROM代码通信。

表6. 用于NOR FLASH连接的FlexSPI引脚分配

FlexSPI引脚	GPIO
FLEXSPI_SSEL0	PIO0_21
FLEXSPI_SSEL1	PIO0_22
FLEXSPI_CLK	PIO0_19
FLEXSPI_D0	PIO0_6
FLEXSPI_D1	PIO0_4
FLEXSPI_D2	PIO0_3
FLEXSPI_D3	PIO0_2
FLEXSPI_D4	PIO1_16
FLEXSPI_D5	PIO1_15
FLEXSPI_D6	PIO1_27
FLEXSPI_D7	PIO1_29
FLEXSPI_DQS	PIO0_25

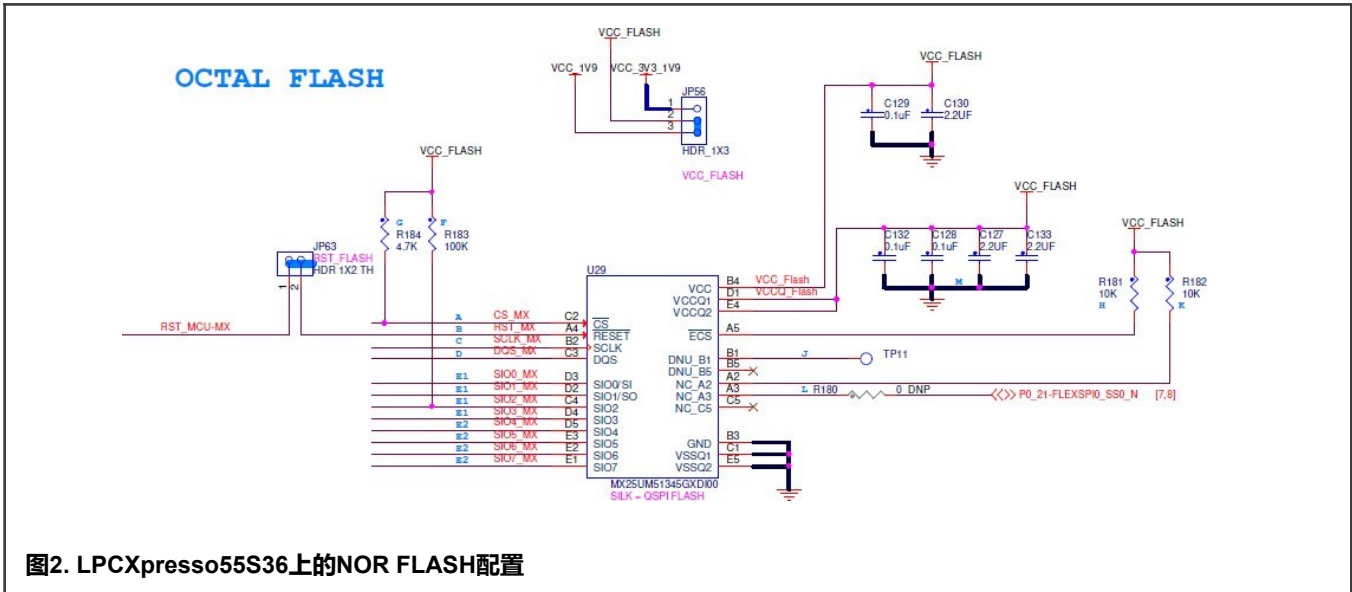


图2. LPCXpresso55S36上的NOR FLASH配置

2.2 配置FlexSPI NOR FLASH

FLEXSPI NOR FLASH配置参数的结构很复杂，但有一个简单的使用方法。为了对FCB进行编码，恩智浦定义了两个uint32_t变量，option0和option1。在大多数情况下，只需配置option0，而将option1留为0x0000_0000。

更多信息，请参阅LPC553x用户手册（UM）中的第11.3.1.2.9.2章，FLEXSPI NOR FLASH配置参数。

表7列出了一些最常用的选项。

表7. 选项代码

Option0代码	说明
0xc0000001	QuadSPI NOR - Quad SDR Read
0xc0233002	HyperFLASH 1V8 (50 MHz)
0xc0333002	HyperFLASH 3V0 (50 MHz)
0xc0433005	MXIC OPI DDR (OPI DDR enabled by default) (50 MHz)
0xc0600002	Micron NOR DDR (50 MHz)
0xc0603002	Micron OPI DDR (50 MHz)
0xc0633002	Micron OPI DDR (DDR read enabled by default) (50 MHz)
0xc0803002	Adesto OPI DDR (50 MHz)

2.3 通过blhost烧写NOR FLASH

LPCXpresso55S36使用MX25UM513连接到FlexSPI接口。

1. 将配置参数存储在RAM中。这些参数用于在下一步配置FLEXSPI。如图4所示，FLEXSPI的配置参数为0xc0403001。
2. 根据FLASH类型选择配置参数。

2.3.1 进入ISP模式

1. 要将启动模式设置为ISP启动，请将ISP0设为高（HIGH），ISP1设为低（LOW）。
2. 将FLEXSPI信号系统与电路板上的引脚正确相连。
3. 关闭电路板的电源。
4. 打开电路板的电源。使用USB电缆（连接到J3），将ISP的USB接口连接到PC。

2.3.2 测试ISP连接

测试MCU是否进入ISP模式，硬件连接是否正常。要用ROM进行ping，请使用get-property1命令。

```
$ ./blhost.exe -u 0x1Fc9,0x0025 get-property 1
Inject command 'get-property'
Response status = 0 (0x0) Success.
Response word 1 = 1258488064 (0x4b030100)
Current Version = K3.1.0
```

图3. Ping ISP连接

2.3.3 生成FLASH配置块

用option0代码生成FLASH配置块，并将配置块存储在RAM中。

```
$ ./blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xC0000001
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.
```

```
$ ./blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.
```

图4. 生成FLASH配置块（FCB）并配置FLASH

2.3.4 用blhost擦除/烧写NOR FLASH

现在，外部NOR FLASH已经配置成功，你可以对其擦除/烧写。

```
$ ./blhost.exe -u 0x1Fc9,0x0025 flash-erase-region 0x08000000 0x20000
Inject command 'flash-erase-region'
Successful generic response to command 'flash-erase-region'
Response status = 0 (0x0) Success.
```

图5. 擦除NOR FLASH

```

$ ./blhost.exe -u 0x1Fc9,0x0025 read-memory 0x08000400 0x100
Inject command 'read-memory'
Successful response to command 'read-memory'
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
(1/1)100% Completed!
Successful generic response to command 'read-memory'
Response status = 0 (0x0) Success.
Response word 1 = 256 (0x100)
Read 256 of 256 bytes.

```

图6. 读取NOR FLASH

```

$ ./blhost.exe -u 0x1Fc9,0x0025 write-memory 0x08001000 boot_image.bin
Inject command 'write-memory'
Preparing to send 75464 (0x126c8) bytes to the target.
Successful generic response to command 'write-memory'
(1/1)100% Completed!
usbhid: received data phase abort
Response status = 10203 (0x27db) kStatusMemoryCumulativeWrite
Wrote 75464 of 75464 bytes.

```

图7. 烧写NOR FLASH

2.3.5 将FCB参数存储在NOR FLASH上

生成FLEXSPI NOR FCB并写入FLASH中，用于FLEXSPI启动。它需要一个位于偏移地址0x08000400处的FCB。当通过FLEXSPI接口从外部NOR FLASH启动映像时，该FCB用于配置FLEXSPI接口。每次当ROM试图从FLEXSPI FLASH启动映像时，都需要FCB。FCB是由之前的FLEXSPI配置参数(0xc0000002)生成的。将生成FCB和烧写参数都存储在RAM中。这些参数用于下一步生成FCB并烧写到FLASH中的0x08000400处。

注意

Boot ROM支持用一个特定的选项0xF000000F，将生成的FCB烧写到NOR FLASH存储器的起始位置(0x08000400)。

```

$ ./blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xF000000F
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.

```

图8. 将FCB配置参数存储在RAM中


```
$ ./blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.
```

图9. FCB生成并烧写到FLASH中，偏移地址为0x08000400

要检查FCB是否被写入，可读回0x08000400处的数据。

```
$ ./blhost.exe -u 0x1Fc9,0x0025 read-memory 0x08000400 0x200
Inject command 'read-memory'
Successful response to command 'read-memory'
46 43 46 42 00 04 01 56 00 00 00 00 03 03 03 00
00 00 01 00 00 00 00 00 00 00 00 00 01 00 02 00
01 07 00 00 01 0a 00 00 00 00 00 00 00 00 00 00
02 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00
10 00 00 00 01 08 01 00 00 00 00 00 00 00 00 00
00 00 00 04 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
ec 07 13 07 20 0b 04 33 04 27 00 00 00 00 00 00
05 04 04 24 00 00 00 00 00 00 00 00 00 00 00 00
05 07 f3 07 20 0b 04 33 04 27 00 00 00 00 00 00
```

图10. 通过blhost工具读回FCB的信息

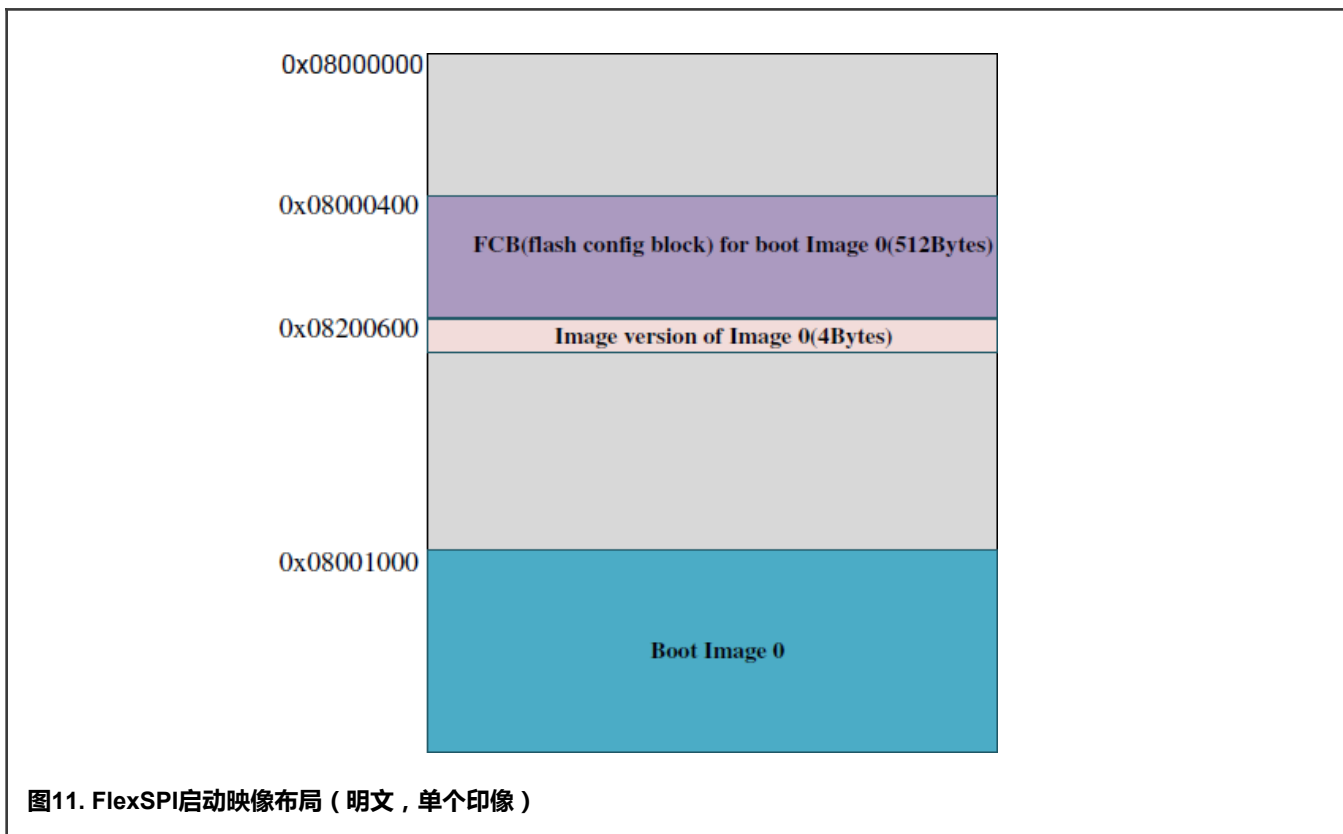
如图10所示，46 43 46 42是FCFB的ASCII字符串。它标示了FCB块的开始。

3 从外部NOR FLASH启动（非安全模式）

本节演示如何从外部NOR FLASH启动映像。详情请参见LPC553X用户手册（UM）中的非安全启动ROM。

Boot ROM支持几种映像类型，包括明文映像、带CRC的明文映像、带签名的XIP明文映像和带CRC的XIP明文映像。本节只讨论最简单的一种：明文映像。

3.1 FlexSPI NOR FLASH启动映像布局（单个映像）



FlexSPI启动映像地址必须是在0x0800_1000处（XIP、加载和执行地址相同）。须在0x0800_0400处写一个有效的FCB块。Boot ROM通过1位SPI模式获取FCB，用FCB信息配置NOR FLASH，并尝试启动NOR FLASH映像。

3.2 FlexSPI启动动手示例

3.2.1 准备FlexSPI启动映像

以SDK中的led_blinky 演示程序为例，项目位置是：

```
\SDK_2_10_0_LPCXpresso55S36\boards\lpcxpresso55s36\demo_apps\led_blinky
```

1. 改变链接文件中的映像起始地址，开始地址必须是0x0800_1000。

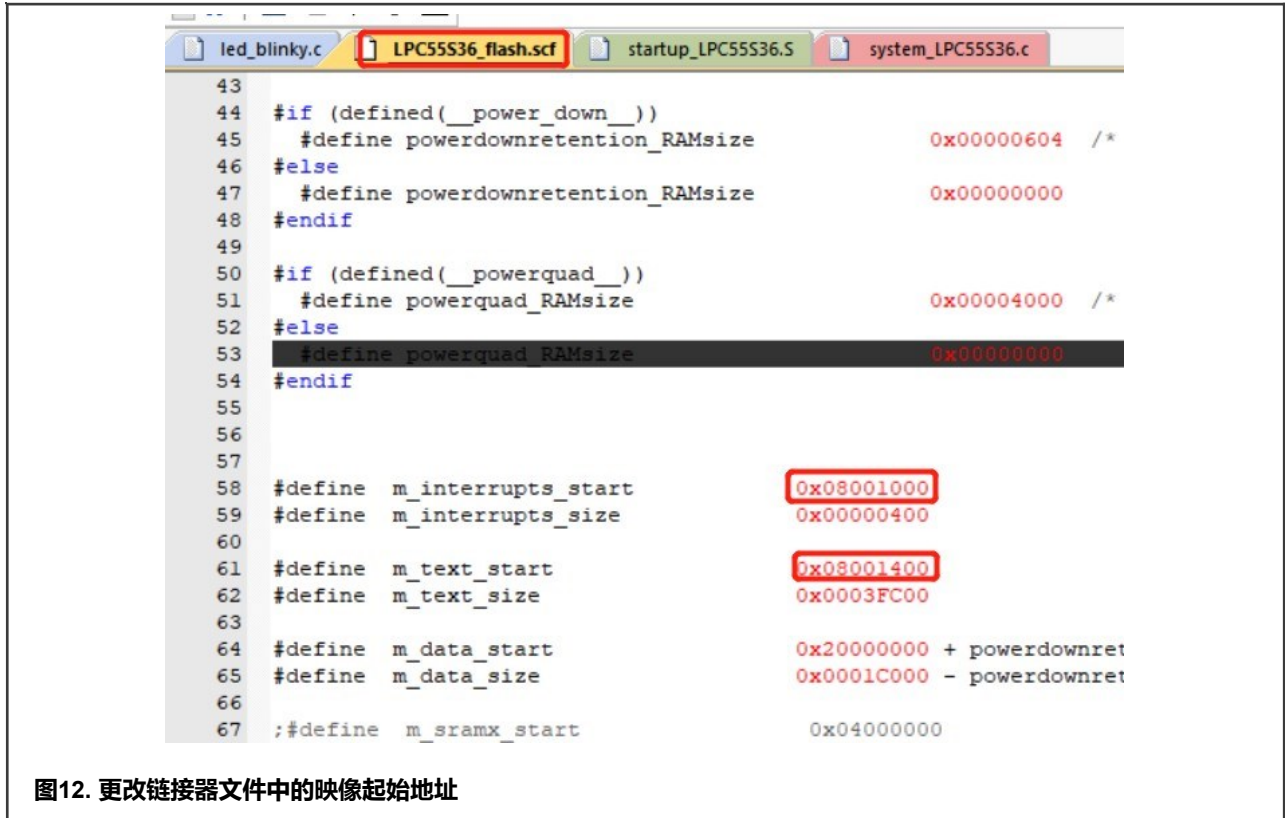


图12. 更改链接器文件中的映像起始地址

2. 将BOARD_BootClockFROHF96M这一行注释掉，因为ROM使用PLL作为FlexSPI时钟源。当从外部存储器运行时，不可能改变PLL设置或时钟设置。当改变FlexSPI时钟设置时，设备必须从内部存储区（Flash或SRAM）运行。

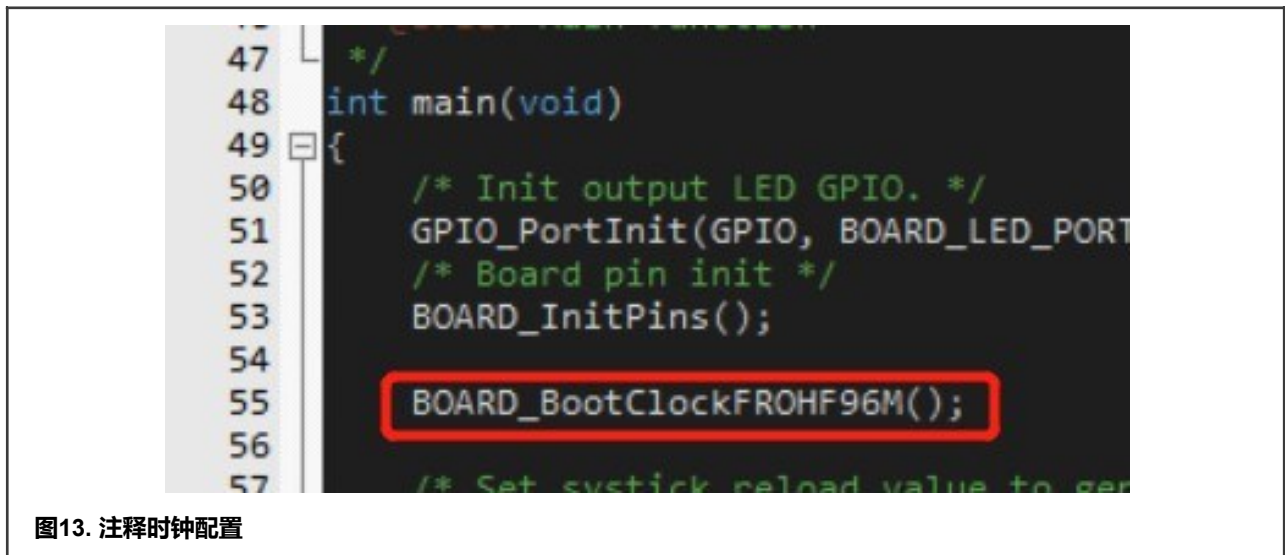


图13. 注释时钟配置

3. 为了编译和生成bin文件，要在用户选项中添加post build命令来生成二进制文件。编译该项目，led_blinky.bin就在/mdk/debug 文件夹中生成了。

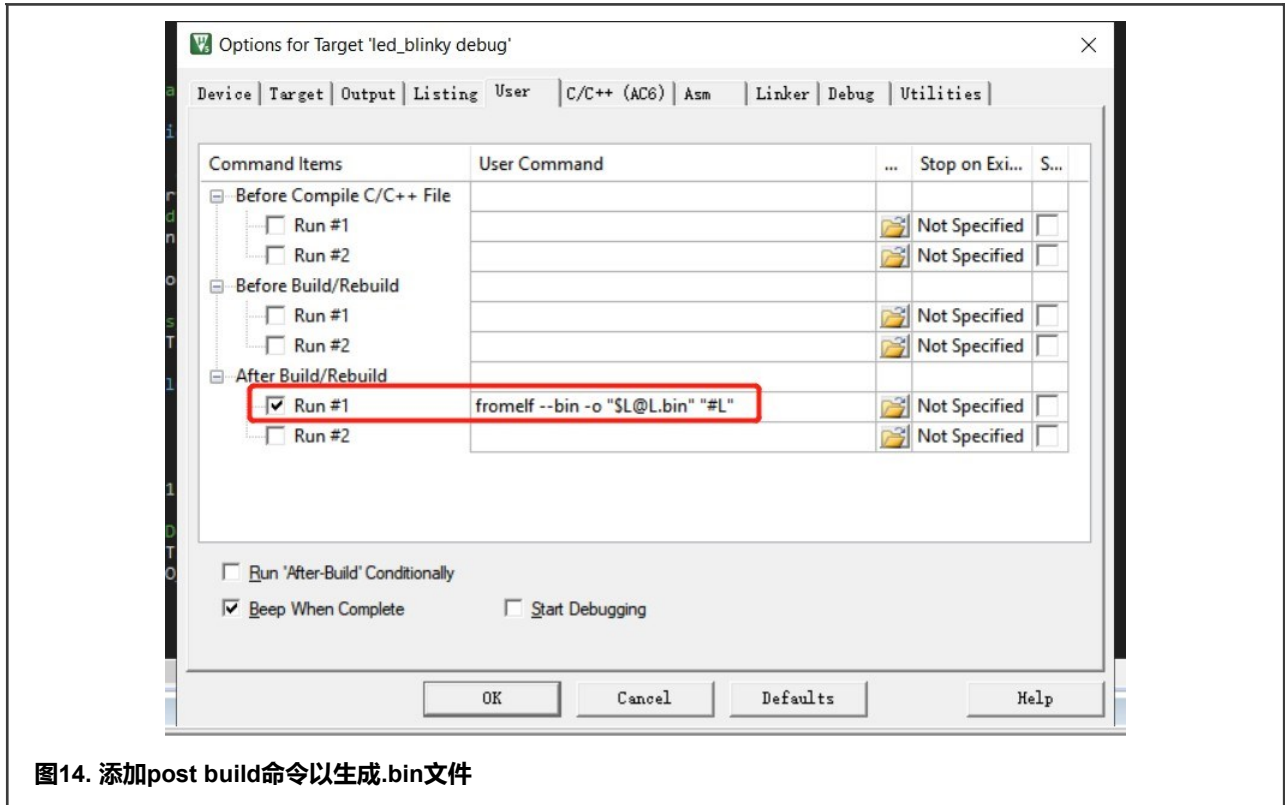


图14. 添加post build命令以生成.bin文件

3.2.2 将FlexSPI映像下载到NOR FLASH中

要把FCB写入0x0800_0400处，请按照[“通过blhost烧写NOR FLASH”](#)。要在0x0800_1000处下载led_blinky.bin，请使用write-memory命令。

图15显示了所有需要的blhost命令。

```

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xC0000001
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 flash-erase-region 0x08000000 0x20000
Inject command 'flash-erase-region'
Successful generic response to command 'flash-erase-region'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xF000000F
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 write-memory 0x08001000 led_blinky.bin
Inject command 'write-memory'
Preparing to send 6284 (0x188c) bytes to the target.
Successful generic response to command 'write-memory'
(1/1)100% Completed!
Successful generic response to command 'write-memory'
Response status = 0 (0x0) Success.
wrote 6284 of 6284 bytes.

```

图15. 烧写FCB并下载映像

3.2.3 执行NOR FLASH映像

将ISP启动引脚设置为外部NOR FLASH启动，按下电路板上的Reset（复位）引脚。板上的LED灯闪烁，意味着映像执行成功。

4 修订历史

版本号	日期	说明
0	2022年2月10日	初版发布
1	2022年5月25日	将LPC553x替换为LPC553x/LPC55S3x

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile — are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved.

Airfast — is a trademark of NXP B.V.

Bluetooth — the Bluetooth wordmark and logos are registered trademarks owned by Bluetooth SIG, Inc. and any use of such marks by NXP Semiconductors is under license.

Cadence — the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All rights reserved worldwide.

CodeWarrior — is a trademark of NXP B.V.

ColdFire — is a trademark of NXP B.V.

ColdFire+ — is a trademark of NXP B.V.

EdgeLock — is a trademark of NXP B.V.

EdgeScale — is a trademark of NXP B.V.

EdgeVerse — is a trademark of NXP B.V.

eIQ — is a trademark of NXP B.V.

FeliCa — is a trademark of Sony Corporation.

Freescale — is a trademark of NXP B.V.

HITAG — is a trademark of NXP B.V.

ICODE and I-CODE — are trademarks of NXP B.V.

Immersiv3D — is a trademark of NXP B.V.

I2C-bus — logo is a trademark of NXP B.V.

Kinetis — is a trademark of NXP B.V.

Layerscape — is a trademark of NXP B.V.

Mantis — is a trademark of NXP B.V.

MIFARE — is a trademark of NXP B.V.

MOBILEGT — is a trademark of NXP B.V.

NTAG — is a trademark of NXP B.V.

Processor Expert — is a trademark of NXP B.V.

QorIQ — is a trademark of NXP B.V.

SafeAssure — is a trademark of NXP B.V.

SafeAssure — logo is a trademark of NXP B.V.

StarCore — is a trademark of NXP B.V.

Synopsys — Portions Copyright © 2021 Synopsys, Inc. Used with permission. All rights reserved.

Tower — is a trademark of NXP B.V.

UCODE — is a trademark of NXP B.V.

VortiQa — is a trademark of NXP B.V.

arm

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2022.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 May 2022

Document identifier: AN13543