Freescale Semiconductor
Solution Guide

NIC3G8360EWP
Rev. 0, 03/2005

Using the PowerQUICC™ II Pro MPC8360E to Build a Network Interface Card for 3G Wireless Equipment

Third Generation (3G) is the general name for technologies that support high-quality voice, high-speed data, and video in wireless cellular networks. The IMT-2000 specification defined by the International Telecommunication Union (ITU) defines two 3G variants and established transmission rate standards for 3G systems—wideband CDMA (W-CDMA) and cdma2000—based on Code Division Multiple Access (CDMA) technology. In Europe, W-CDMA/3G service is known as Universal Mobile Telephony System (UMTS). Figure 1 shows a UMTS network.

Contents

freescale™ semiconductor

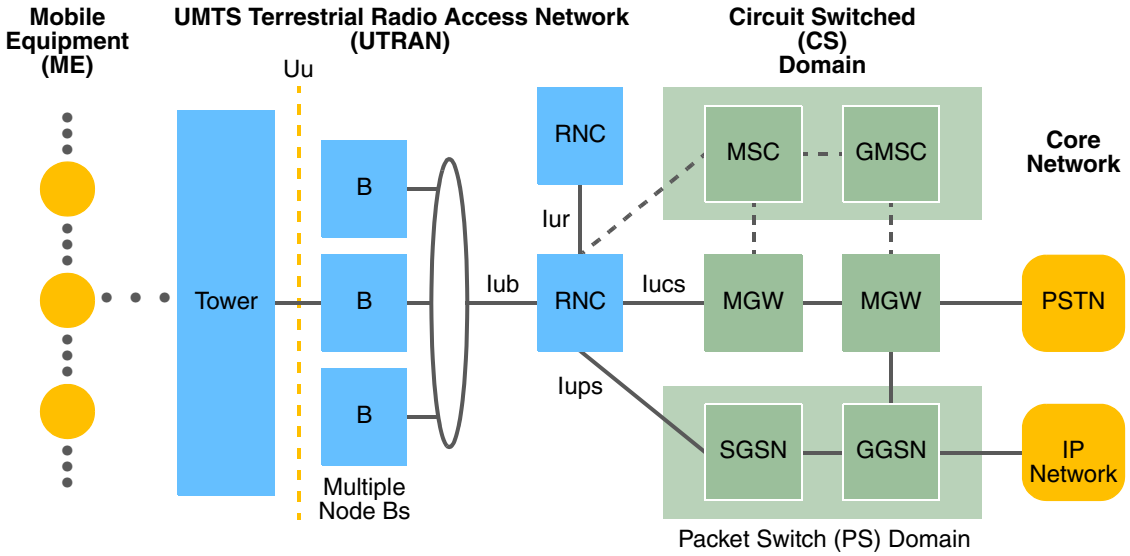

Figure 1. Overview of 3G UMTS Network

The UMTS Terrestrial Radio Access Network (UTRAN) includes the Radio Network Controller (RNC), the 3G Base stations (Node Bs), and the air interface (Tower) to the mobile equipment (ME). Table 1 describes UMTS network elements and interfaces.

Table 1. Network Functions

Function	Definition
MSC	Mobile Switching Centre (MSC) including the Visitor location register (VLR) is a switch that serves the Mobile Equipment (ME) in its current location for Circuit Switched (CS) services.
GMSC	Gateway MSC (GMSC) is the switch at the point where the UMTS network is connected to the external CS network.
MGW	The MSC and GMSC handle control functionality, but user data goes through the Media Gateway (MGW), which performs the actual switching for user data and network interworking processing
SGSN	Serving GPRS Support Node (SGSN), which covers functions similar to the MSC for packet data, including VLR type functionality
GGSN	Gateway GPRS Support Node (GGSN) connects the Packet-Switched (PS) core network to other networks such as the Internet.
Node B	A 3G Base station (Node B) handles radio channels, including the multiplexing/demultiplexing of user voice and data information.
RNC	The Radio Network Controller (RNC) is responsible for controlling and managing the multiple base stations (Node Bs) including the utilization of radio network services.
3G Network Interfaces	
Uu	Interface between the UMTS Terrestrial Radio Access Network (UTRAN) and the ME includes for example phones, laptops and PDAs.
Iub	Interface between the NodeBs and the RNCs. Typically multiple T1/E1 links from each NodeB aggregated to one or several ATM STM-1 (OC-3) links or one STM-4 link.

Table 1. Network Functions (continued)

Function	Definition
Iur	Interface between the RNCs for soft handover. Usually implemented on one or several ATM STM-1 (OC-3) links or one STM-4 (OC-12) link.
Iucs	Core network interface between the RNCs and circuit-switched voice network. Usually implemented on a STM-4 (OC-12) link or an Ethernet link.
Iups	Core network interface between the RNCs and packet-switched data network. Usually implemented on a STM-4 (OC-12) link or an Ethernet link.

1 Design Challenges

With the potential to offer multiple revenue streams from a single IP packet network, the triple play of voice, video, and data is the goal of every telecom operator. To meet the needs of end-users in today's 3G markets, equipment manufacturers must provide an extensive range of cost-effective integrated voice and high-speed data services. In addition to cost effectiveness, flexibility and future proofing are crucial considerations because, although the network will eventually rely completely on IP (Internet Protocol) communication links, ATM will be the dominant transmission standard for the foreseeable future. Therefore, today's equipment must inter-operate between circuit and packet-switched networks and between many standards and protocols.

The network interface card (NIC) in 3G Wireless Base Stations (also referred to as NodeBs) carry voice and data from the end user equipment over T1/E1 links to the Radio Network Controller (RNC) bundled through the Inverse Multiplexing over ATM (IMA) protocol, which transports higher bandwidth traffic over multiple lower bandwidth links. Using ATM as the transport technology, these links will migrate to higher data rates, such as OC-3/STM-1 (to aggregate the traffic of multiple Node Bs), with ATM Adaptation Layers to carry voice (AAL2), data (AAL5), and signaling (AAL1) traffic to a GSM Base Station.

Due to the increasing popularity of IP technology and IP networks, Release 5 of the 3GPP specification adds a secondary option to the Transport Network Layer (TNL) using IP. The TNL links network equipment in the UTRAN. User data can now be conveyed over UDP/IP in the Iur and Iub interfaces, in addition to the AAL2/ATM option. With the use of IPv6 mandatory and IPv4 optional, different header compression techniques are important. For example, each IPv6 header is 128 bits long so compression of these headers is required to improve bandwidth usage on narrowband links such as E1/T1.

For a Node B that is compliant with 3GPP Release 5, MLPPP and Ethernet are generally used for low bandwidth interfaces. For high bandwidth interfaces, where the traffic for multiple Node Bs is aggregated, 1 or 2 STM-1 interfaces or Gigabit Ethernet are more appropriate.

ATM remains the switching layer predominantly used on the UTOPIA back plane, but alternative back plane concepts, such as Ethernet, are under consideration for future IP-ready solutions. When adding IP networking capability to an existing ATM based Node B, interworking capability should be added between the IP based network and the legacy ATM back plane. With an ATM network and an Ethernet back plane compliant with the Open Base Station Architecture Initiative (OBSAI), interworking is also required. OBSAI is an open forum started by Hyundai Syscomm, LG Electronics, Nokia, Samsung Electronics and ZTE Corporation in 2002 with the goal of creating an open market or common architecture for a base station transceiver system (BTS) with four components—transport, base band, RF, and control modules. This interworking occurs on the UDP level because OBSAI specifies the base band module to be UDP/IP/Ethernet-based.

In the migration to a complete IP packet-based Iub interface and Node B architecture, telecom operators must move quickly to a cost-effective Ethernet-based network. To do this without redesigning existing Node Bs and RNC

equipment, equipment vendors may complement their systems with emerging technologies and protocols, such as PWE3 (Pseudo Wire Emulation Edge-to-Edge as defined by the IETF) which allows the transport of ATM and/or TDM data over a packet network.

As you can see, a variety of physical implementations for the Iub and Iur interfaces and the backplane are required. This makes a flexible and programmable solution for the network interface highly desirable.

Specific design challenges for Network Interface Cards include:

- Support for the increasing number of different network interfaces and speeds required, ranging from channelized T1/E1 lines through OC-12 SONET and Gigabit Ethernet interfaces
- Scalability from Pico to Macro solutions, including aggregation
- Support for the convergence of ATM and IP packet networks by adapting to different protocols used including: ATM (AAL2, AAL5) VLAN, RTP, PPP, ML/MC-PPP, PPP Mux, IP header compression, Routing, Diffserv, IPSec and QoS
- Management of quality of service (QoS) to ensure prioritization of latency sensitive traffic, such as voice
- Flexibility to add new features and functions through in-field software upgrades as market demands dictate

In this environment, wireless equipment manufacturers face the complex challenge of adding more flexibility and processing power to line cards without inflating system cost or exceeding the power budget.

2 Freescale Semiconductor Solutions

The competitive 3G wireless market necessitates highly integrated, cost-effective and scalable system solutions. With these system requirements in mind, Freescale is pleased to introduce the latest addition to its popular PowerQUICC family of microprocessors—the PowerQUICC II Pro MPC8360E.

The MPC8360E incorporates the e300, 603e core which includes 32 KBytes of L1 instruction and data caches, 32-bit PCI bridge, four DMA channels, USB support, dual 32-bit DDR memory controller, a double precision floating point unit and on-board memory management units. A block diagram of the MPC8360E is shown in Figure 2.

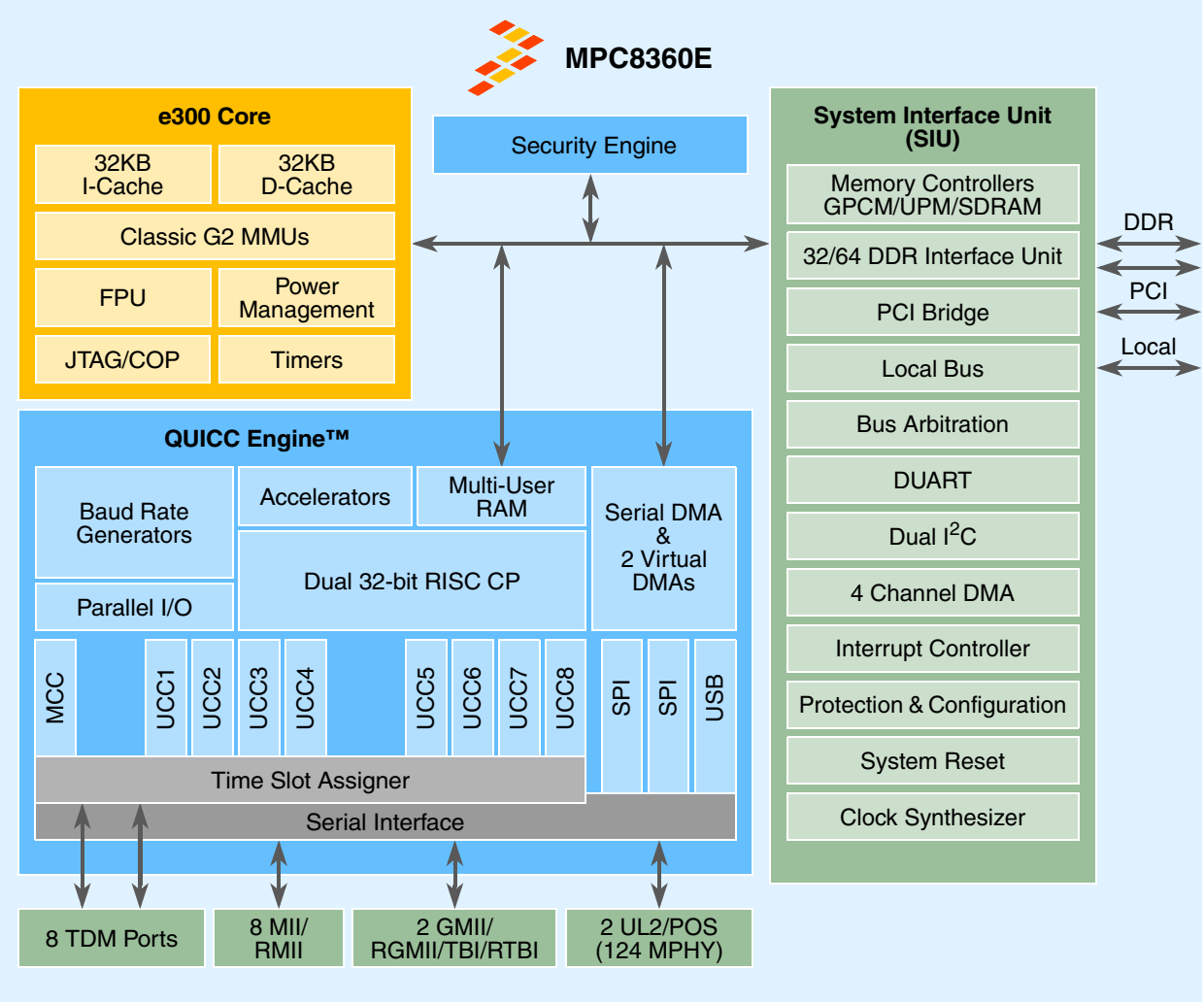

Figure 2. MPC8360E Block Diagram

A new communications complex—the QUICC Engine™—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port,

VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced inter-working features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides vendors with a highly integrated, fully programmable communications processor that allows reuse of existing legacy PowerQUICC II and III software drivers and microcode packages. This helps ensure that a low cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32K bytes of Level 1 Instruction and 32K bytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS

  - QoS types of traffic, such as voice, video, and data
- Security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC™ processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) Interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC, however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

2.2.2 Application Development System (ADS)

Freescale provides an ADS board as a reference platform and programming development environment for the MPC8360E with a complete Linux Board Support Package. The ADS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

Also available is a complete development system based around the AdvancedTCA (ATCA) form factor chassis with a choice of AMC cards that can be operate stand alone, or as modular inserts into the main processor baseboard. This allows maximum flexibility for prototyping wireless network interface, control and base band applications using Freescale silicon solutions.

2.2.3 Modular Software Building Blocks

The QUICC Engine will be supported by a complete set of configurable device API drivers and initialization software. Figure 3 shows the wealth of software protocols that the QUICC Engine with the e300 PowerPC™ core is able to provide.

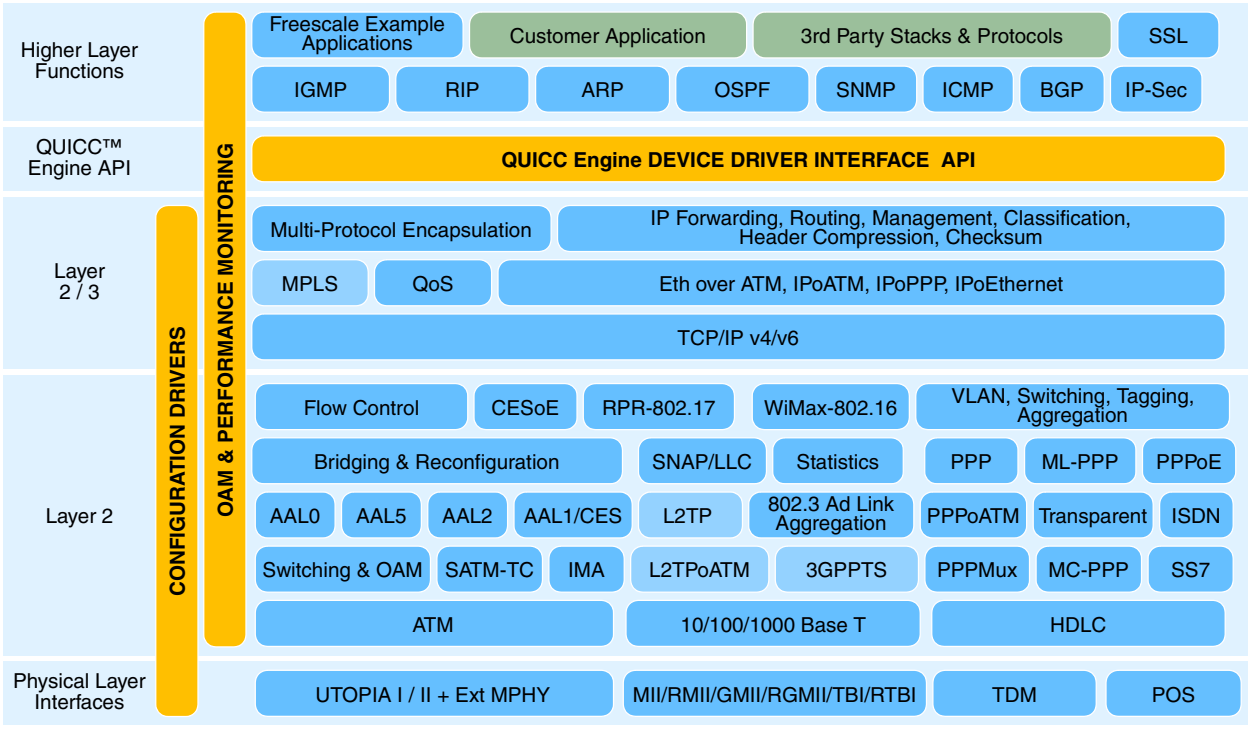

Figure 3. Software Protocol Support for the QUICC Engine

3 Application Example—Node B Network Interface Card

The MPC8360E's internal features and protocol support allow a wide range of network solutions to be developed. Figure 4 illustrates how easily a typical Node B Network Interface Card application created with the MPC8360E.

In this application the MPC8360E provides all of the processing, protocol and interworking functions required to implement the Node B Network Interface card. The QUICC Engine is used to carry voice, data and video using ATM or IP over eight T1 /E1 TDM links bundled with IMA or MLPPP terminated protocols between the Node Bs and the RNC. In addition, one of the UCCs in the QUICC Engine could be used to support either a Gigabit Ethernet (GMII) or ATM (Utopia 8/16bit) interface to a back plane in the Node B. Another UCC could be used to implement an STM-1 / OC-3 (AAL5 and AAL2) link to the network (RNC). The unused UCCs can be configured as serial (UART) or Ethernet (MII) for debug and control.

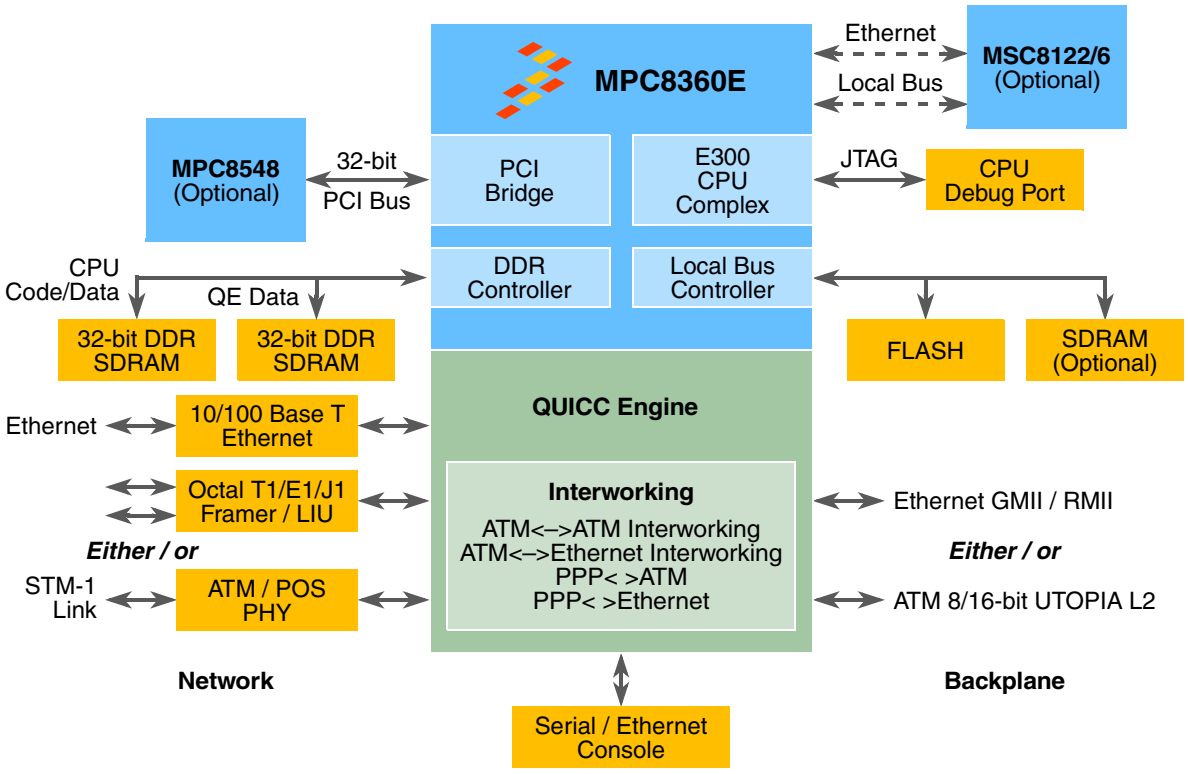

Figure 4. NodeB Network Interface Card Using the MPC8360E

In this application, the MPC8360E's QUICC Engine uses interworking to offload the e300 CPU and accelerate data plane functions, including mapping of ATM ports based on the VPI/VCI/CID to IP/UDP ports based on the MAC addresses.

The main system memory is provided by a dual 32-bit DDR SDRAM controller, which allows extremely efficient partitioning of system parameters and data. One 32-bit DDR memory can be used for control plane processing (code/data) and the other can be used for data plane processing (data). The 32-bit DDR SDRAM controllers can also be combined into a single 64-bit DDR SDRAM controller. The local bus can be used for optional SDRAM or on-board FLASH EPROM.

In this example, the MPC8360E can support an Ethernet connection or local bus connection to a DSP farm on the base band module. Options include the MSC81xx DSPs based on StarCore technology, which supports an Ethernet interface. The MSC8122 takes advantage of the scalable Starcore® architecture to provide a "DSP-farm-on-a-chip"

level of performance integration. Using the latest process technologies for low core voltage and low power dissipation, the quad-core MSC8122 can deliver up to 8000 DSP MMACS performance at up to 500MHz, yielding a performance equal to 2.0GHz.

The PCI bus on the MPC8360E can be used to interface to an MPC8548 PowerQUICC III if additional CPU processing power is required. The MPC8548 supports an e500 PowerPC core up to 1.33GHz with 32Kbytes of L1 instruction cache, 32Kbytes of L1 data cache, and 512Kbytes of L2 cache/SRAM. The CPU in the MPC8360E provides more than 1200 MIPS of processing performance. When combined with the parallel communication capability of the QUICC Engine, this will be sufficient in many cases.

4 Summary

The PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration, and cost-effectiveness for a wide variety of applications. For a flexible, high performance, wireless network interface cards, the MPC8360E offers a comprehensive feature set that enables cost effective solutions with an unrivalled level of versatility to evolve as standards and the system requirements change.

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

email:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

NIC3G8360EWP
Rev. 0
03/2005

freescale™
semiconductor