ENGINEERING SPECIFICATIONS

MPC860SAR-PHY ADAPTER BOARD

ATM155, ATM25.6 and E1/T1 Physical Adapter to the 860SAR

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Haim Amir
MOTOROLA SEMICONDUCTOR ISRAEL LTD.

CHAPTER 1 - GENERAL INFORMATION

1•1 INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the MPC860SAR-PHY board.

1•2 FEATURES

The main features of the MPC860SAR-PHY board are as follows:

- The board connect to the MPC860ADS/MPC8xxFADS via a 96PIN connector (P13).
- ATM 155.52Mhz, 51.84Mhz using the PMC PM5346 device. or IDT77155.
- ATM 25.6Mbps using the IDT IDT77105 device.
- The PM5346 and IDT77105 are connected to the MPC860SAR via the Utopia bus, operating @25Mhz maximum.
- The physical interface connection to the PM5346 is via an optical adapter (HP HFBR-5205).
- The physical interface connection to the IDT77105 is via RJ45 with 4 twisted pair wires.
- The selection of working with IDT77105 or PM5346 is by changing five jumpers.
- T1 1.54Mbps using the DALLAS DS2180 device.
- E1 2.048Mbps using the DALLAS DS2181 device.
- The T1/E1 (DS2180, DS2181) uses the same socket.
- The T1/E1 Interface Line is done by DS2186 (Transmitter) and DS2187 (Receiver)

1•3 SPECIFICATIONS

The MPC860SAR-PHY specifications are given in Table 1-1.

Table 1-1 MPC860SAR-PHY Specifications

CHARACTERISTICS	SPECIFICATIONS
Power requirements (no other boards attached)	+5Vdc @ 2 A (typical), 2.5 A (maximum)
Operating temperature	0 degrees to 30 degrees C ambient air temperature
Storage temperature	-25 degrees to 85 degrees C
Relative humidity	5% to 90% (non-condensing)
Dimensions Height Depth Thickness	 3.93inches (100 mm) 7.086 inches (180 mm) 0.063 inches (1.6 mm)

1•4 GENERAL DESCRIPTION

The MPC860SAR-PHY is a development tool for the MPC860SAR device. This board is used for hardware and software development of applications using the MPC860SAR device mounted on the MPC860ADS/ MPC8xxFADS.

The MPC860SAR-PHY is a board that connected to MPC860ADS/MPC8xxFADS and provides ATM155.52M/51.84M, interface to the line via SC optical line driver and to the 860SAR via a UTOPIA bus. The used device is PM5346. ATM25.6M interface to the line via RJ45 connector and to the 860SAR via a UTOPIA bus. The used device is IDT77105. And E1/T1 interface to the line via RJ45 connector, to the 860SAR via a E1/T1 860SAR dedicated pins, the E1/T1 are two devices that only one of them is mounted on the board. The used devices are DS2180 for T1 and DS2181 for E1. The board can perform at the same time E1/T1 and ATM155.52M/51.84 or 25.6M. The control of all the PM5346 and IDT77105 is done by the 860SAR ports, and the control of the DS2180/DS2181 is done by the 860SAR SPI port. The MPC860SAR-PHY has logic analyzer connectors. The logic analyzer connectors enable to monitor the used activity pins of the MPC860SAR.

NOTE: Before operating the board the user should define the modes of operation and then make sure all the Dip Switches and jumpers are set accordingly.

1•5 RELATED DOCUMENTATION

The following publications are applicable to the MPC860SAR-PHY and may provide additional helpful information.

- MPC860SAR Spec.
- ATM spec
- E1/T1 Spec.
- PMC PM5346 Device User manual.
- IDT77155 Device User Manual.
- IDT77105 Device User Manual.
- DALLAS: DS2180AQ, DS2181AQ, DS2186, DS2187 Devices User Manual.

1•6 ABBREVIATIONS USED IN THE DOCUMENT

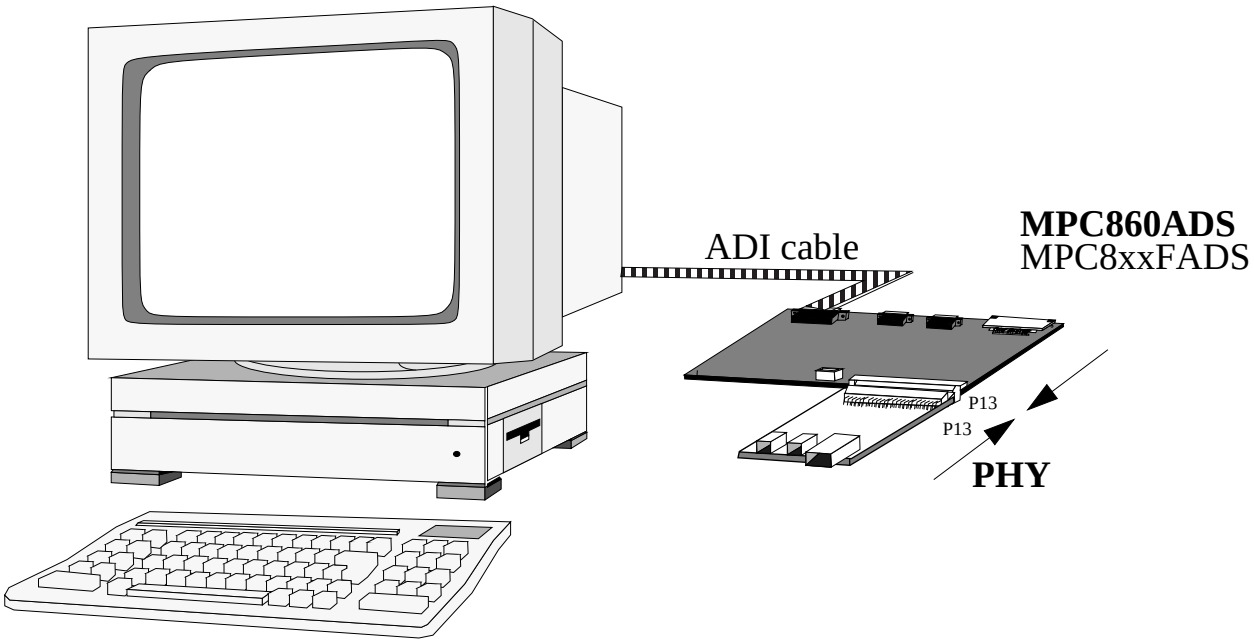
- ATM - Asynchronous Transfer Mode.
- SAR - Segmentation And Reassembly.
- TC - Transmission Convergence.
- PMD - Physical Medium Dependent.
- UTOPIA - Universal Test & Operations PHY Interface for ATM.
- AAL - ATM Adaptation Layer.
- spec - Engineering specification document.

1•7 REQUIRED EQUIPMENT

The MPC860SAR-PHY can operate in two working environments:

- MPC860ADS or MPC8xxFADS board.
- Fiber optic cables multimode SC type from one side.
- Cable to connect to the RJ45 connector for the E1/T1 or ATM25.6M.

FIGURE 1-1 MPC860SAR-PHY Connection Way



CHAPTER 2 - HARDWARE PREPARATION AND INSTALLATION

2•1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MPC860SAR-PHY.

2•2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

2•3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the MPC860SAR-PHY board, changes of the Dip-Switchs and jumpers settings may be required before connecting the board to the MPC860ADS/ MPC8xxFADS. The location of the LEDs, Dip-Switches, and connectors is illustrated in the figures bellow. The board has been factory tested and is shipped with Dip-Switch settings as described in the following paragraphs. The default state of the Dip switches are shown in the tables below:

FIGURE 1-2 Dip-Switch DS1

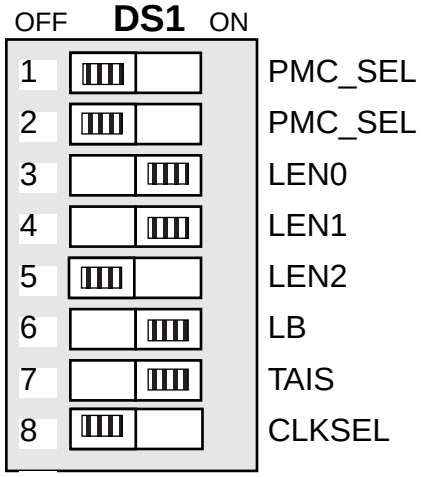


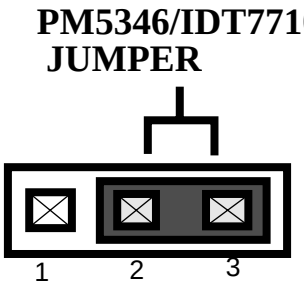
Table 2-1 DS1 Board setting.

Number	ON/OFF	Default
DS1(1)	ATM155.52/ATM51.84	OFF
DS1(2)	ATM155.52/ATM51.84	OFF
DS1(3)	LEN0	ON
DS1(4)	LEN1	ON
DS1(5)	LEN2	OFF
DS1(6)	Loop Back	ON
DS1(7)	Transmit Alarm Indication Signal	ON
DS1(8)	CLKSEL	OFF

2•3•1 PM5346 - IDT77105 J1 - J5

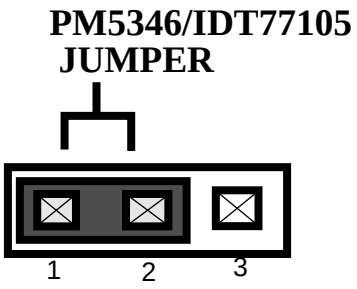
IDT77105 - Enabled

When the jumpers: J1 - J5 are installed on pins 2 - 3, IDT77107 is choice.



PM5346 - Enabled

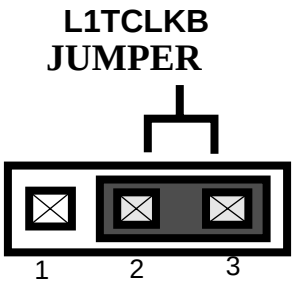
When the jumpers: J1 - J5 are installed on pins 1 - 2, PM5346 is choice.



2•3•2 L1TCLKB J6

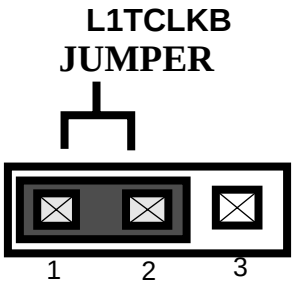
L1TCLKB

When the jumper J6 is installed on pins 2 - 3, U12 implements the TCLK to the E1/T1.
NOTE: In this case J8, J9 and U12 must be install.
The default is that pins 1 - 2 is connected.



L1TCLKB

When the jumper J6 is installed on pins 1 - 2, TCLK is connected to the RCLK.
The user should config the SIMOD register bit CRTB to 1. In this case U12 should be off the board.
The default is that pins 1 - 2 is connected.

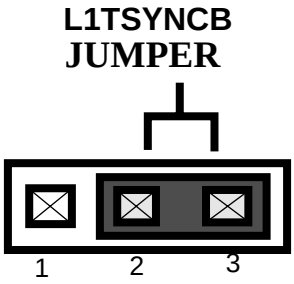


2•3•3 L1TSYNCB J7

L1TSYNCB

When the jumper J7 is installed on pins 2 - 3,
the 860SAR implements the TSYNC to the E1/T.
by using U12 for TIN2 and producing TOUT2 for TSYNC

NOTE: In this case J8, J9 and U12 must be install.
The default is that pins 1 - 2 is connected.



L1TSYNCB

When the jumper J7 is installed on pins 1 - 2,
TCLK is connected to the RCLK.
The user should config the SIMOD register
bit CRTB to 1. In this case U12, J8 and J9 should be
off the board.
The default is that pins 1 - 2 is connected.

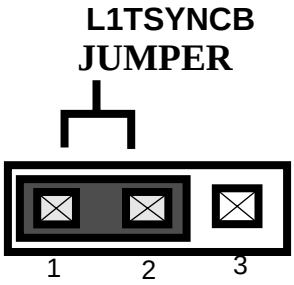
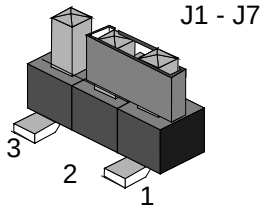
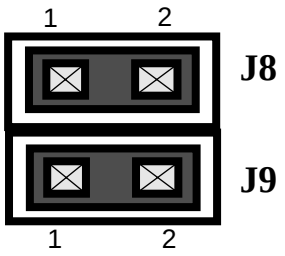


FIGURE 2-1 JUMPERS J1 - J7



2•3•4 TOUT2, TIN2 J8, J9

When the jumper J8, J9 are installed,
the 860SAR gets its L1TCLKB from the on board crystal (U12)
and perform the L1TSYNCB from TOUT2.
NOTE: In this case J6, J7 must be connected
between pins 2, 3.



When the jumper J8, J9 are not installed, the 860SAR gets
its L1TCLKB from the on board RCLK. (by setting SIMOD
register bit CRTB to 1)
NOTE: In this case J6, J7 must be connected
between pins 1, 2.

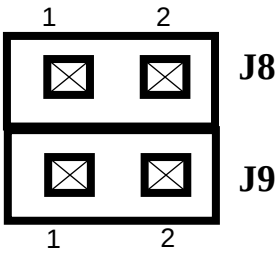
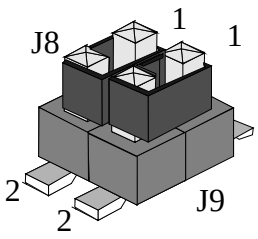


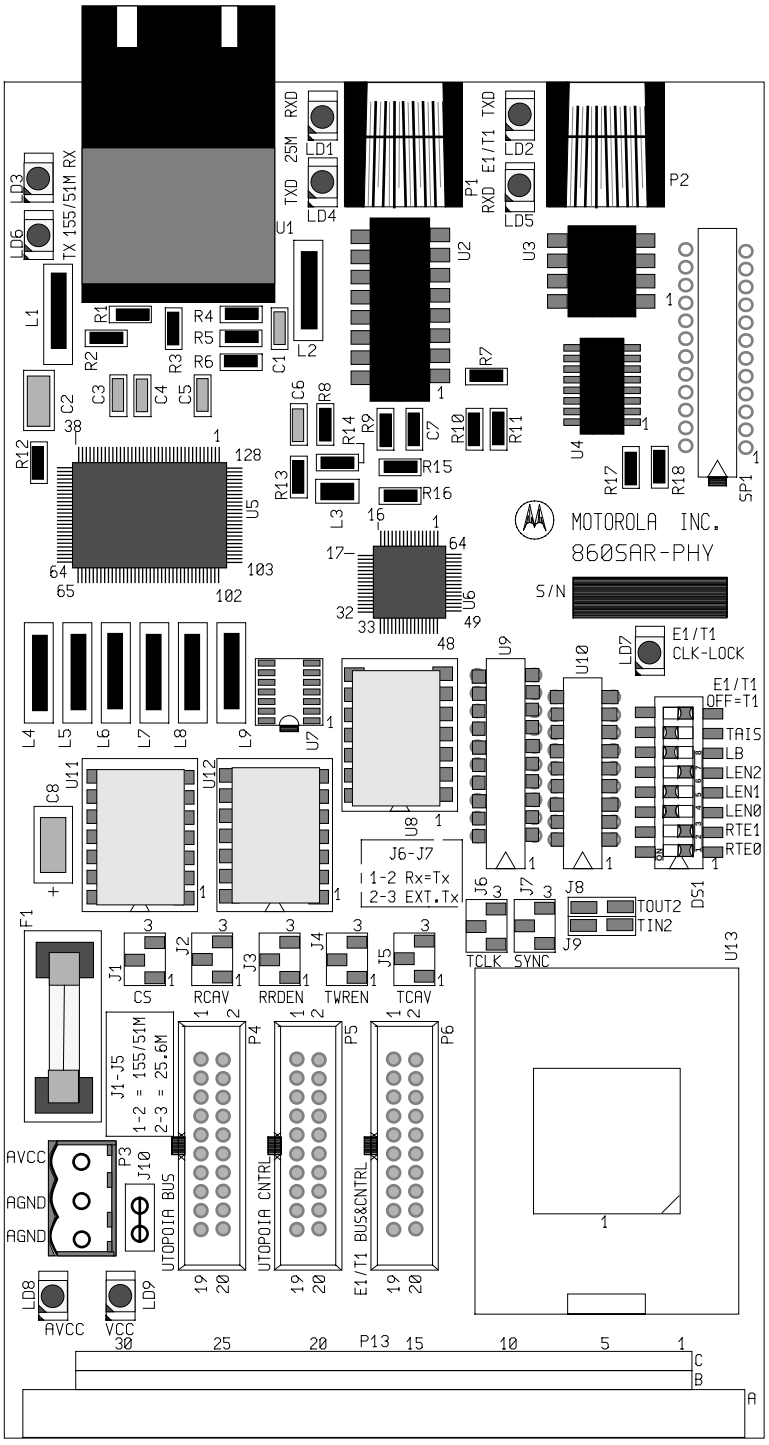
FIGURE 2-2 J8, J9 TOUT2, TIN2



Parameters can be changed for the following conditions:

- ATM155.52Mb/s or 51.84Mb/s (DS1, 1, 2).
- E1/T1 wave shaping including cable length. (DS1, 3-5).
- E1/T1 Transmit Loop Back enable (DS1, 6).
- E1/T1 Transmit Alarm Indication enable. (DS1, 7).
- E1/T1 selection. (DS1, 8).
- ATM25.6Mb/s (IDT77105), J1-J5 pins 2,3 or ATM155.52/51.84Mb/s (PM5346) J1-J5 pins 1,2.
    - The selection of the Chip Select signal for IDT77105 or PM5346 (J1).
    - The selection of the RCAV signal for IDT77105 or PM5346 (J2).
    - The selection of the RRDEN signal for IDT77105 or PM5346 (J3).
    - The selection of the TWREN signal for IDT77105 or PM5346 (J4).
    - The selection of the TCAV signal for IDT77105 or PM5346 (J5).
- E1/T1 TCLK source (J6).
- E1/T1 TSYNC source (J7).
- Use TOUT2 and TIN2 as a general purpose I/O. (J8, J9).

FIGURE 2-3 MPC860SAR-PHY Board



2•3•5 DS1 Board Configuration.

Table 2-2 DS1 Board configuration

Number	ON/OFF	Default	
DS1(1)	ATM155.52/ATM51.84	OFF	155.52Mb/s Selected
DS1(2)	ATM155.52/ATM51.84	OFF	
DS1(3)	LEN0	ON	0 db buildout, 0 - 133feet
DS1(4)	LEN1	ON	
DS1(5)	LEN2	OFF	
DS1(6)	Loop Back	ON	No LoopBack
DS1(7)	Transmit Alarm Indication Signal	ON	No TAIS
DS1(8)	CLKSEL	OFF	T1 Selected

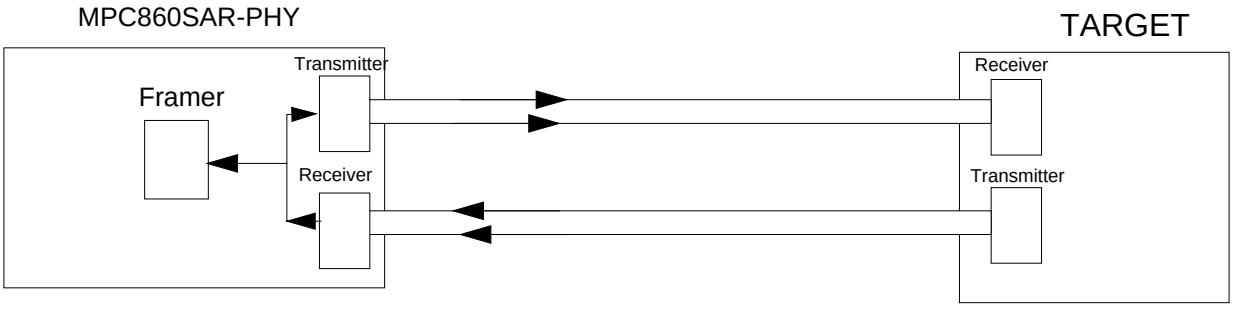
DS1(1-2) configure the ATM frequency. If the PM5346 was chosen, (J1 - J5 connected pins 1 and 2) by setting DS1(1,2) to OFF, the frequency selected is 155.52Mb/s, or if DS1(1) is ON and DS1(2) remain OFF the ATM frequency is 51.84Mb/s.
DS1(3-5) The device DS2186 Transmit Line Interface, supports T1 short loop (DSX-1; 0 to 655 feet), T1 long loop (CSU; 0 dB, -7.5 dB and -15 dB) and E1 (CCITT G.703) pulse templet requirements. The shape of T1 wave form is controlled by LEN0:LEN2 when DS1(8) is OFF these control inputs allow the user to select the appropriate output pulse shape to meet DSX-1 CSU templates over a wide variety of cable types and lengths. those cable types include ABAM, PIC and PULP. The E1 mode is enabled when DS1(8) is ON only one output pulse shape is available for E1 mode; LEN0:LEN2 can be in any state except all'0'.

Table 2-3 T1 LENGTH SELECTION

LEN2	LEN1	LEN0	OPTION SELECTION	APPLICATION
0	0	0	Test Mode	Do not use
0	0	1	-7.5dB buildout	T1 CSU
0	1	0	-15dB buildout	T1 CSU
0	1	1	0dB buildout, 0 - 133 feet	T1 CSU, DSX-1cross connect.
1	0	0	133 - 266 feet	DSX-1cross connect.
1	0	1	266 -399 feet	DSX-1cross connect.
1	1	0	399 - 533 feet	DSX-1cross connect.
1	1	1	533 - 655 feet	DSX-1cross connect.

DS1(6) Loop Back. The board gives the ability to the user to loop back its target through the board and still to be able to read the input data from the target according to draw bellow. To enable external loop back DS1(6) should be OFF.

FIGURE 2-4 ENABLING EXTERNAL LOOP BACK

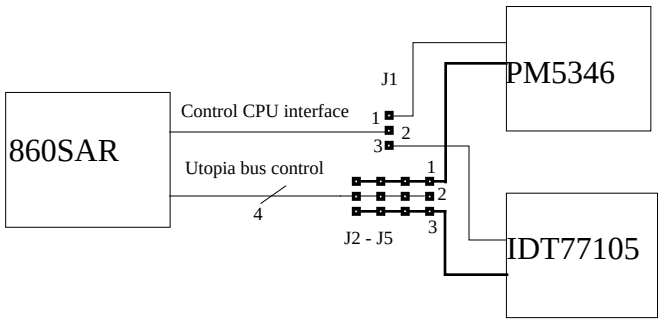


DS1(7) The user can send an alarm indication signal to the target by moving DS1(7) to OFF.
DS1(8) Select the type of operation T1 or E1. The default for DS1(8) is OFF (T1).

2•3•6 PM5346 / IDT77105 Enabling, J1 - J5.

J1 - J5 Enables the PM5346 or IDT77105 by five jumpers as shone in the draw bellow. The jumpers J1-J5, When pins 1 and 2 are connected the PM5346, ATM155.52/51.84Mb/s will be active, if pins 2 and 3 are connected the IDT77105, 25.6Mb/s will be active. The jumpers J1 to J5 controls the following signals:
J1 controls the Chip Select signal which control the CPU interface.
J2 controls the Receive Cell AVailable signal.
J3 controls the Receive ENable signal.
J4 controls the Transmit ENable signal.
J5 controls the Transmit Cell AVailable signal.

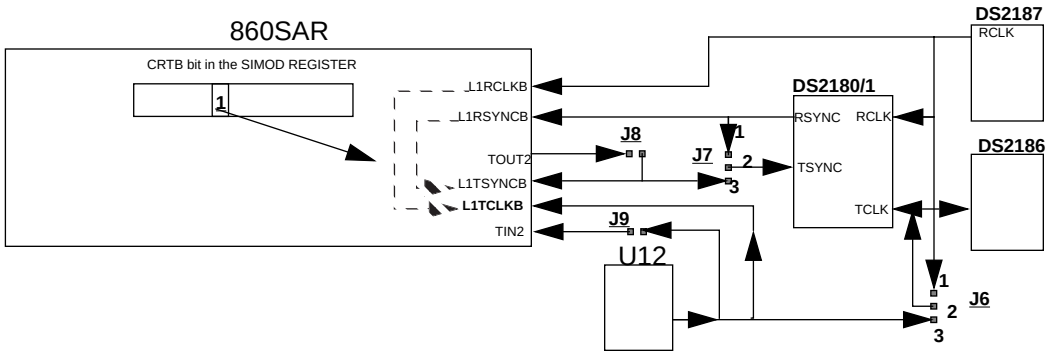
FIGURE 2-5 ENABLE PM5346 or IDT77105.



2•3•7 L1TCLK and L1TSYNC J6 - J9

There are two ways to produce the L1TCLK and L1TSYNC signals (These signals are input to the 860SAR) The first way is to use the L1RCLK from the DS2187 and L1RSYNC from DS2180/DS2181 by connecting J6 and J7 pins 1,2 and setting CRTB bit in the SIMOD REGISTER in the 860SAR to'1'.
In this option L1TCLK and L1TSYNC are used internally and the output pins can be used as a general I/O.
NOTE: that in this option U12, J8 and J9 must be off the board.
The second way is to populate U12, for E1 2.048Mhz or for T1 1.544Mhz in this way the user should populate J8 and J9. J9 transfer the L1TCLK to TIN2 the 860SAR produce TOUT2 from TIN2. J8 transfer the TOUT2 to L1TSYNC. In this option J6, J7 must be connected on pins 2, 3.
The figure bellow illustrate the optional connection.

FIGURE 2-6 L1TCLK and L1TSYNC Configuration



2•4 INSTALLATION INSTRUCTIONS

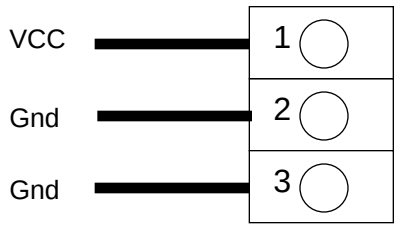
When the MPC860SAR-PHY has been configured as desired by the user, it can be installed according to the required working environment as follows:
Connect the MPC860SAR-PHY to P13 of the M860ADS or P8 in the M8xxFADS.

NOTE: The 5V DIGITAL POWER IS SUPPLIES BY P13.

2•4•1 +5V Analog Power Supply Connection

The MPC860SAR-PHY requires an external +5 Vdc analog, power supply for operating the board analog part.
Connect the +5V analog power supply to connector P3 as shown below:

FIGURE 2-7 P3: +5V Power Connector



P3 is a 3 terminal block power connector with power plug. The plug designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires. To insure solid ground, two Gnd terminals are supplied. It is recommended to connect both Gnd wires to the common of the power supply, while VCC is connected with a single wire.

CHAPTER 3 - OPERATING INSTRUCTIONS

3•1 INTRODUCTION

This chapter provides necessary information to use the MPC860SAR-PHY connected to M860ADS or M8xxFADS. This includes controls and indicators details, of the board.

3•2 CONTROLS AND INDICATORS

The MPC860SAR-PHY has the following switches and indicators.

3•2•1 Dip Switch DS1

DS1 control the following functions.

- MP5346 ATM frequency. pins 1, 2
- T1 line configuration pins 3, 4 and 5.
- External loop back ability pin 6.
- TAIS pin 7.
- E1 or T1 clock select pin 8.

3•2•2 J1 - J5

J1 - J5 enable the PM5346 (155.52Mb/s or 51.84Mb/s) or IDT77105 (25.6Mb/s).

3•2•3 J6 - J9

Select the source of the L1TCLK and L1TSYNC of the E1/T1 circuit.

3•2•4 ATM25.6Mb/s Receive led. LD1

LD1 is light whenever the IDT77105 receive data.

3•2•5 ATM25.6Mb/s Transmit led. LD4

LD4 is light whenever the IDT77105 transmit data.

3•2•6 ATM155.52/51.8Mb/s Receive led. LD3

LD3 is light whenever the PM5346 receive data.

3•2•7 ATM155.52/51.8Mb/s Transmit led. LD6

LD6 is light whenever the PM5346 transmit data.

3•2•8 E1/T1 Transmit led. LD2

LD2 is light whenever the E1/T1 transmit data.

3•2•9 E1/T1 receive led. LD2

LD5 is light whenever the E1/T1 receive data.

3•2•10 Clock IN Lock LD7

LD7 is the E1/T1 clock in lock indication.

3•2•11 Analog VCC Power LD8

LD8 is light whenever the analog VCC is supplies.

3•2•12 Digital VCC Power LD9

LD9 is light whenever the MPC860SAR-PHY connected to the M860ADS or to M8xxFADS and the ADS has a power supply.

CHAPTER 4 - FUNCTIONAL DESCRIPTION

4•1 INTRODUCTION

This chapter details the hardware design of the MPC860SAR-PHY, and describes each module.

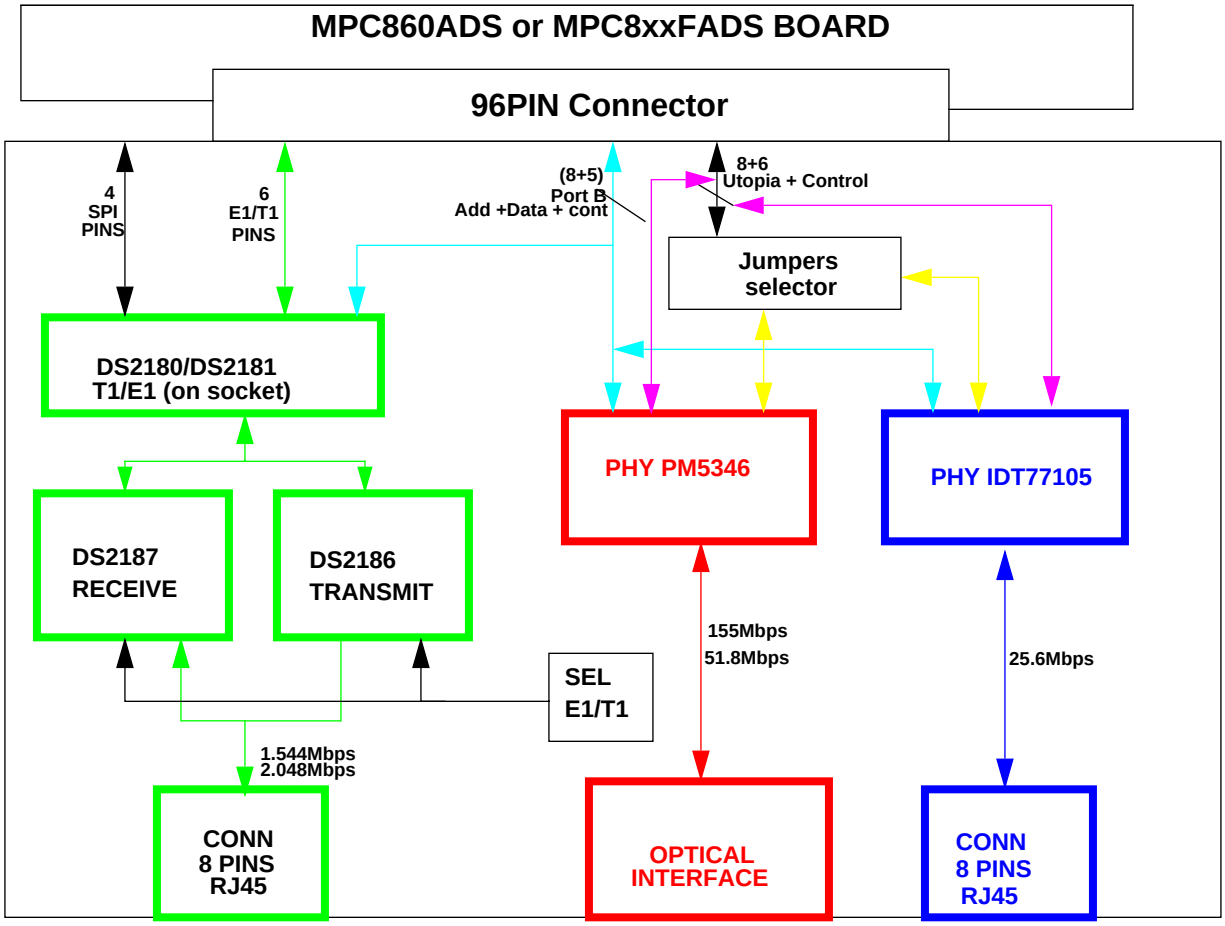
4•2 GENERAL DESCRIPTION

The MPC860SAR-PHY compose of four parts.

- 1. M860ADS or M8xxFADS include the MPC860SAR on board.
- 2. ATM155.52/51.84Mbps used the PMC Sierra PM5346 or the IDT77155 device.
- 3. ATM25.6Mbps used the IDT77105 device.
- 4. E1 - 2.048Mbps / T1 - 1.544Mbps use the DALLAS framer DS2180/DS2181 and DS2186 and DS2187.

The following paragraphs will describe each one of the board parts.

FIGURE 4-1 860SAR_PHY BLOCK DIAGRAM



The first part is the 860SAR

4•3 The 860SAR

The 860SAR has the same pinout as the MPC860 chip.

The MPC860SAR-PHY is a member of the MPC860 PowerQUICC family in addition to all MPC860 capabilities, the 860SAR includes the Universal Test & Operation PHY Interface for ATM (UTOPIA), AAL5 and AAL0 Segmentation and Reassembly (SAR) functionality, ATM Pace Controller (APC) and PHY interface for E1 and T1 that implemented by the serial channels.

The MPC860SAR operates in two ATM modes, the first, parallel via the Universal Test & Operations PHY Interface for ATM (UTOPIA), Implementing the AAL5 and AAL0, Segmentation And Reassembly (SAR) connected to the ATM UTOPIA PHY Device. The second is serial via one of the SCC ports implementing the AAL5, AAL0, SAR and Transmission Convergence TC sublayer to interface to E1/T1 framer.
The Utopia bus and the control bus are common to the PM5346 and to the IDT77105. A set of jumpers divisional between the two parts so that from the 860SAR point of view only one device is connected to its UTOPIA bus and to the control bus.

4•3•1 860SAR GENERAL DESCRIPTION

The ATM controller perform several ATM sublayers. There are two modes that are supported by the ATM controller. The first is ATM controller with UTOPIA parallel interface (parallel mode) and the second mode is ATM controller with serial interface (serial mode). In both modes the ATM controller performs ATM Adaptation Layer (AAL5 and AAL0), Segmentation and Reassembly (SAR) and the ATM layer protocol function. In the Parallel mode, the ATM layer interfaces the PHY directly through UTOPIA interface. In the serial mode, the ATM controller also implements the Transmission Convergence (TC) sublayer and interfaces the PHY, serially, through its SCCs.

As mentioned above, the PHY interface to the ATM controller is UTOPIA or a bit stream from the TC layer. On the other side of the ATM function the ATM controller performs the AAL SAR on the user data which resides in the system memory on a single or multiple data buffers.

This chapter describes the transmit and receive mechanisms for the two modes and the functionality of the ATM Pace Controller (APC) which is common to the two modes. Detailed information for the two modes can be found in the M860SAR user manual.

4•3•1•1 ATM controller Parallel Mode.

In the parallel mode, the SAR handles receive and transmit on a cell by cell basis. The UTOPIA interface implements cell level handshake and therefore the supported bit rate is higher than the bit rate accomplished in the serial mode.

4•3•1•2 Transmitter Overview

The transmit process begins at the ATM Pace controller (APC). The APC controls the ATM traffic of the transmitter; it consists of a timer which is set by the user that defines the maximum outgoing bit rate. The APC holds the traffic parameter of each channel and shares the total bit rate among the requesting channels. It can provide Constant Bit Rate (CBR) and support for Available Bit Rate (ABR) traffic services. Its task is to define the next channel (or channels) to be transmitted.

If the APC schedules a channel to be transmitted and the PHY asserts the Transmit Cell Available (TxCav) signal, the transmitter will start the transmit process. At first the transmitter will take the first ch# from the Transmit Queue. according to the ch# it will open the channel's entry in the Transmit Connection Table (TCT) and check the status of the specific connection. If there is no open data buffer, it will open a new transmit buffer using the channel's Buffer descriptor (BD) list. Then it will copy 48 octets from the external buffer, internally. It will perform CRC32 for AAL5, copy the cell header from the cell header entry of the TCT and then transmit the whole cell through the UTOPIA interface.

At the last cell of an AAL5 frame, the transmitter will append to the user frame the trailer of the Common Part Conversion Sublayer - Protocol Data Unit (CPCS-PDU). It will add pad as required, it will append the length (which were calculated during the frame transmit) and copy the CPCS-UU and CPI from the BD.

Also the transmitter will set the CPI bit at the header of the last cell of the message. An interrupt will be optionally generated to declare the end of Tx frame.

In case of no additional valid buffer for the requesting channel in the BD list, the transmit process will end and the PHY will optionally generate an Idle cell. The PHY will keep transmitting Idle cells every time this channel will generate a transmit request until a new valid buffer will be ready, or Deactivate Channel command will be issued.

In case of AAL0, the ATM controller will simply copy the whole cell (except the HEC) which was prepared by the user, from the Channel's buffer and transmit it through the UTOPIA I/F. The ATM controller will optionally (Option check - TBD) generate CRC10 on the cell payload and place the result at the end of the payload (CRC10 field). This feature is best for supporting OAM CRC10 (see ITU I.610).

4•3•1•3 Receiver Overview

The receive process begins when the PHY assert the receive Cell Available signal (RxCav). This indicates that the PHY has a complete cell in its receive FIFO.

The receive process will begin by receiving the cell header through the UTOPIA I/F. The receiver will translate the header address (VC/VP/PTI) to a channel number by performing a binary search on the Address Look-up Table. A cell header that have no match in the look-up table will be treated as a raw cell (AAL0). Then the channel status will be read from the Receive Connection Table (RCT) and the complete cell will be copied from the UTOPIA I/F, internally. If there is no open buffer a new buffer will be opened, CRC will be calculated, payload (48 octets) will be copied to the buffer and the RCT parameters will be updated. In case of no additional empty buffers for the received channel in the BD list, an Interrupt will be generated and the cell will be discarded.

The end of AAL5 frame will be recognized by the CPI bit. In that case the receiver will separate the trailer of the Common Part Conversion Sublayer - Protocol Data Unit (CPCS-PDU) from the user data. It will cut the pads as required; it will check the length field against the length which was calculated during the frame receive, copy the CPCS-UU and CPI to the BD and close the buffer. An interrupt will be optionally generated to declare the end of Rx frame. CRC or length error will be marked in the BD and an interrupt will be generated for this case.

In case of AAL0, the ATM controller will simply copy the whole cell (except the HEC) from the UTOPIA to the channel's buffer list. It will calculate and check CRC10 on the cell payload. This option is best for OAM cell check (see ITU I.610).

4•3•1•4 ATM controller Serial Mode.

The serial mode is independent of the physical interface standard used. The physical interface should be able to provide synchronization signals to the 860sar such that it will deliver and accept byte aligned data to/from the 860sar serial interface. Generally, one of the 860sar TDM ports will be used in the serial mode to allow easy connection to an E1 or T1 line interface device. Other serial interfaces are not precluded and may be selected when programming the 860sar serial interface. This User's Manual describes the TDM interface using the Time Slot Assigner (TSA)

In the serial mode, the transmit and receive flows are similar to the parallel mode. In addition to the functionality of the parallel mode, the serial mode perform the TC layer which adds Cell Delineation, Scrambling, Idle cell generation/screening and interface using the TDM, an E1 or T1 line interface device.

4•3•1•5 Transmitter Overview

Similarly to the parallel mode, the transmit process begins at the ATM Pace Controller (APC). The APC controls the ATM traffic of the transmitter. The APC holds the traffic parameter of each channel and can provide Constant Bit Rate (CBR) and Available Bit Rate (ABR) traffic services. Its task is to define the next channel (or channels) to be transmitted. The APC writes the channel number (Internal I.D) to the Transmit Queue.

In the serial mode, transmit request is generated by the serial. The transmitter will read the next channel from the Transmit Queue, It will read the channel data from the Transmit Connection Table (TCT) and

update the TCT. It will copy the cell internally, calculating CRC32, performing scrambling (optionally), adding the cell header and calculating HEC. After cell assembly process, it will transmit the cell to the serial.

At the last cell of an AAL5 frame, the transmitter will append to the user frame the trailer of the Common Part Conversion Sublayer - Protocol Data Unit (CPCS-PDU). It will add pad as required, it will append the length (which were calculated during the frame transmit) and copy the CPCS-UU and CPI from the BD. Also the transmitter will set the CPI bit at the header of the last cell of the message. An interrupt will be optionally generated to declare the end of Tx frame.

This time, In case of empty Transmit Queue or no additional valid buffer (valid BD) for the requesting channel in the BD list, the transmitter will generate an Idle or Unassigned cell (to be defined by the user). The transmitter will keep sending Idle/unassigned cells until there is a valid ch# in the Transmit Queue or a new valid buffer (BD) will be ready, or Deactivate Channel command will be issued.

Similarly to the parallel mode, In case of AAL0, the ATM controller will simply copy the whole cell (except the HEC) which was prepared by the user, from the channel's Cell buffer, internally. It will optionally (Option check - TBD) generate CRC10 on the cell payload and place the result at the end of the payload (CRC10 field). This feature is best for supporting OAM CRC10 (see ITU I.610).

4•3•1•6 Receiver Overview

The receive process can start only after the receiver acquire synchronization on the incoming cells and can perform cell delineation.

The receive request is generated by the serial. At first, the receiver will copy the first word from the Serial to the DPR. The receiver will translate the header address (VC/CP/PTI) to a channel number using a look-up table. If a header does not match any entry in the look-up table, it will be treated as an AAL0 cell. Then the channel status will be read from the Receive Connection Table (RCT). The Cell will be copied from the serial internally. Then CRC32 will be calculated, scrambling (optionally) will be done and HEC will be checked. Cells with HEC errors will be treated regularly and the error will be reported in the BD. At the end of the cell assembly process, the cell payload will be copied to the external memory by the DMA bursts. RCT will be updated. In case of no additional empty buffer for the received channel in the BD list, an Interrupt will be generated and the cell will be discarded.

The end of an AAL5 frame will be recognized by the CPI bit. In that case the transmitter will concatenate the trailer of the Common Part Conversion Sublayer - Protocol Data Unit (CPCS-PDU) from the user data. It will cut the pads as required, it will check the length field against the length which were calculated during the frame receive, copy the CPCS-UU and CPI to the BD and close the buffer. An interrupt will be optionally generated to declare the end of Rx frame. CRC or length error will be marked in the BD and an interrupt will be generated for this case

The receiver will screen out Idle cells and optionally screen out Unassigned cells.

Similarly to the parallel mode, In case of AAL0, the ATM controller will simply copy the whole cell from the serial to the channel's buffer list. It will calculate and check CRC10 on the cell payload. This option is best for OAM cell check (see ITU I.610).

4•3•1•7 Cell Delineation

Cell Delineation is part of the receiver flow. The user must provide synchronization signals to the 860sar and octet-align incoming cells to the synchronization signals. The ATM controller provide SDH/PDH oriented cell delineation using the HEC mechanism defined in I.432 on an octet basis. The synchronization signals must be octet aligned with incoming cells. When using E1 and T1 ATM links, the cells are always octet aligned (see ITU G.804) and synchronization signals are provided by the E1 and T1 interface devices.

When reception commences, The ATM controller takes a short while to acquire correct cell delineation. Once The ATM controller has locked to the incoming cell stream, it remains locked unless there are excessive errors. An interrupt is generated whenever the cell lock status changes and a status bit will indicate the current delineation status.

4•3•1•8 Cell Payload Scrambling

Cell Payload Scrambling is, optionally, done in both transmit flow (scrambling) and receive flow (descrambling) using the $X^{43}+1$ scrambling algorithm. The first cell to be transmitted after initialization will not be correctly scrambled because there is no valid data in the 43-bit delay line. ATM controller always transmits an empty cell first therefore avoiding data corruption. On reception, the descrambling algorithm self-synchronizes before the HEC delineation process is complete and cell reception begins.

4•3•1•9 Extended mode.

In this mode the ATM controller can extend the number of supported connection from 32 channels (Rx and Tx) up to 64K transmit and receive channels. In this case, the TCT and RCT expansion will be placed in the user memory (external) and a CAM or address compression method will be used instead of the receive look-up table. In this case "internal" channels (channels with internal TCT and RCT) will be supported regularly and "external" channels (channels with TCT and RCT placed in the user memory) will be used with additional DMA access to read and update the external TCT and RCT. The bit rate supported by the Extended mode will be reduced and is depend on the number of external channels and the bit rate ratio between external and internal channels.

4•3•1•10 ATM Pace Control (APC)

The ATM Pace Control determines the next channel (or N channels) to be transmitted and writes this channel, in the Transmit Queue every cell times. The APC is an internal mechanism which is fully controlled by the CP. The CP holds a cyclic table (APC Table) in which it calculate the timings of all the active channels.

The APC predefined inputs are programmed by the user: APC Table length, N - the number of cell to be selected in N cell times and APC request timer. The APC uses APC_pace parameter in the TCT, which can be changed "on the fly" to define the required bit rate. This attribute and the ability to change the rate "on the fly" is used to control ABR traffic.

For CBR, the APC_period is fixed. it is set by the user prior to the activation command. For ABR, The APC_period is dynamic and it defines the ABR Available Cell Rate (ACR). It is the user responsibility to evaluate Resource Management (RM) cells and update the APC_period entry in the TCT.

The APC, optionally, may handle two APC tables. The first table will be serviced with high priority and the second will be serviced with a lower priority where channels from the second table will be scheduled on a bit rate availability basis. This capability is used for channels with higher Cell Delay Variation (CDV) tolerance and UBR traffic

4•3•1•11 Expanded cells

Typical ATM cells are 53 byte long: header (4 bytes), Hec (1 byte) and payload (48 bytes). The 860sar also support up to 64 byte cells (expanded cell) which use extra header fields for internal information in switch applications. In this case the expanded header will be 0 to 3 words long. In this case an expanded cell will contain expanded header (0 or 4 or 8 or 12 bytes), Cell header (4 bytes) and payload (48 bytes).

During transmit, the expanded header of each cell will be taken from the expanded field in the BD and transmitted ahead of the cell header and payload. At the receive side, the expanded header of the last cell of the current connection, will be copied to the expanded field in the Rx BD.

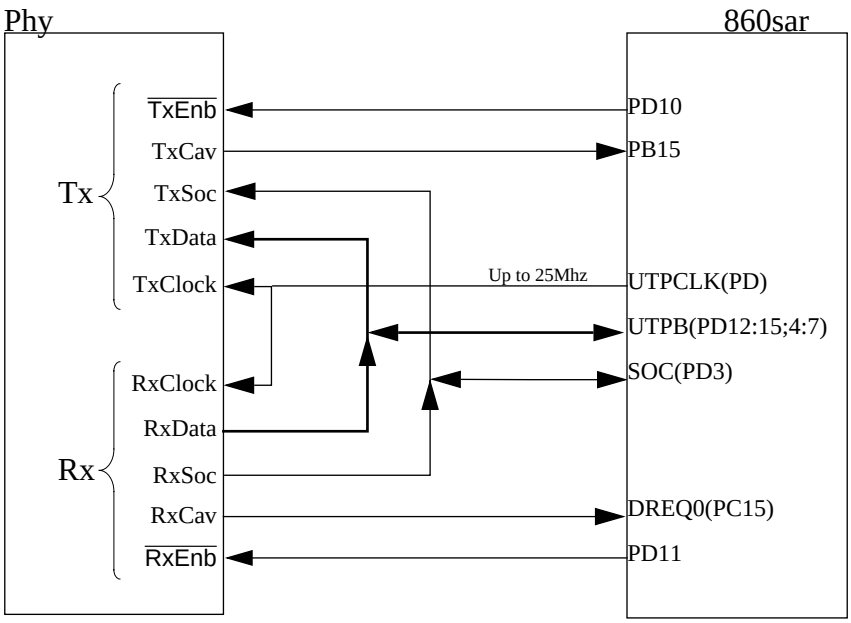
4•4 UTOPIA BUS

The 860sar implements the ATM layer UTOPIA master according to UTOPIA level 2 specification (The ATM Forums UTOPIA level 2 Version 0.95) for a single ATM single PHY configuration. The 860sar implements UTOPIA on an 8-bit wide bidirectional data bus, using a cell-level handshake, operating up to 25 MHz. The UTOPIA controller controls all interface signals. Assertion of Tx Cell Available (TxCav) or Rx

Cell Available (RxCav) will issue a request to the CP to handle a Receive or Transmit operation. During the cell transfer, the UTOPIA controller will control the enable signals ($\overline{\text{TxEnb}}$ or $\overline{\text{RxEnb}}$) and the Transmit Start Of Cell signal (TxSOC). It will sample the RxSOC during the cell transfer.

Most of the UTOPIA pins will be muxed on 860sar port D pins as shown in the figure bellow. IDMA request on Ext0 pin is replaced with RxCav and TxCav is using port B[15] pin.

FIGURE 4-1 860sar UTOPIA



The 860sar is implementing cell level interface. The cell level handshake is identical to the octet level handshake except for one difference, namely that once the TxCav or RxCav is asserted, the PHY must be capable of accepting or transferring a whole cell. The 860sar uses this property to transmit or receive a whole cell directly to/from the system memory on a receive or transmit operation.

4•4•0•1 Receive Cell transfer operation.

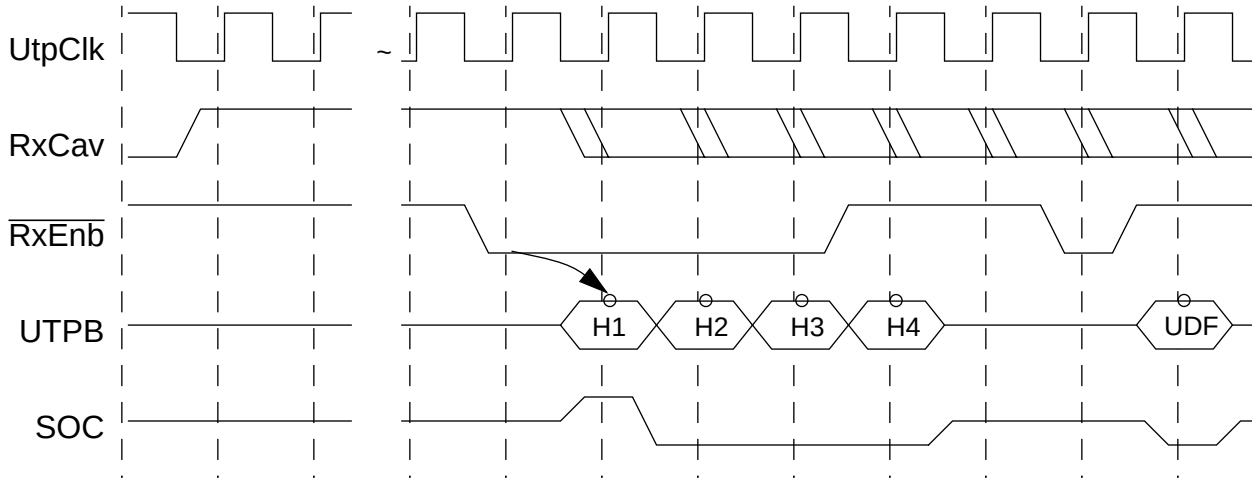
Assertion of RxCav will generate a request of receive cell transfer. The 860sar UTOPIA implements the cell level handshake, therefore as soon as the RxCav is asserted, the PHY side should be able to transfer a whole cell upon $\overline{\text{RxEnb}}$. The 860sar UTOPIA controller divide the cell transfers to small sections of 4 bytes transfers (or less). and use the $\overline{\text{RxEnb}}$ to control that. For example, sequence of a 53 byte cell transfer is divided to the following UTOPIA transfer sections:

- Header transfer (4 octets)
- UDF (HEC) transfer (1 octet)
- 12 cell body transfers (12 x 4 octets)

For each of the above sections section, the 860sar will assert the $\overline{\text{RxEnb}}$. On the next cycle it will start sampling the UTOPIA bus (UTPB) and the RxSOC signal. For the UDF section, there will be only one octet transfer. All other sections will be 4 octet long.

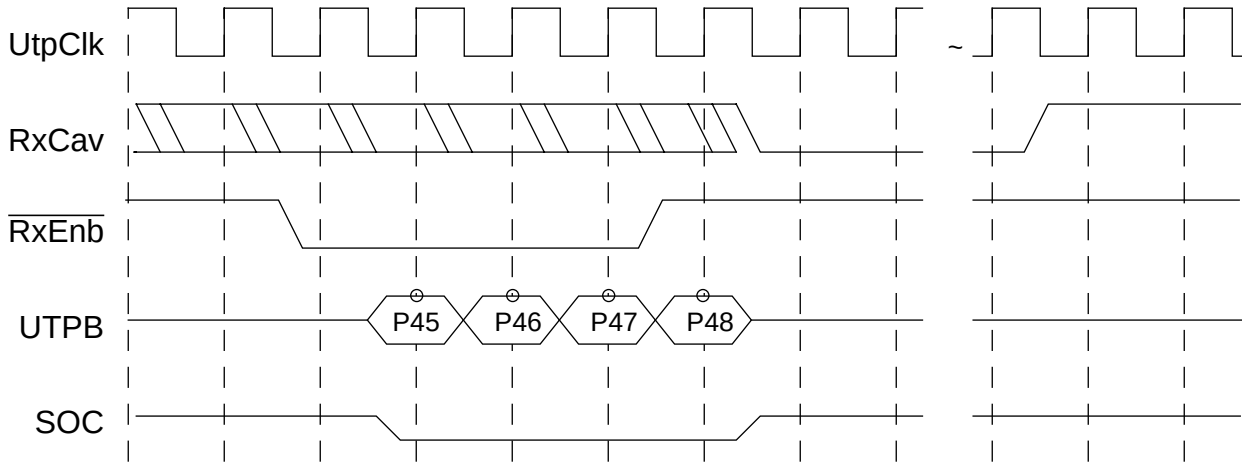
The start of cell transfer of 860sar is shown in Figure . The circles represent the sampling point of the 860sar. Note that the RxCav is not sampled during the cell transfer.

FIGURE 4-2 Receive UTOPIA start of cell



The end of cell transfer of 860sar is shown in Figure . The circles represent the sampling point of the 860sar. In this example the PHY side was not ready with additional cell, therefore it deasserted RxCav and then after few clocks it asserted RxCav again to notify of an additional cell. In case that the PHY side is ready to send an additional cell at the end of the current cell, it could assert RxCav at any time during cell transfer and hold it asserted until the first transfer of the additional cell.

FIGURE 4-3 Receive UTOPIA end of cell



4•4•0•2 Transmit Cell transfer operation.

Assertion of TxCav will generate a request of transmit cell transfer. RxCav request is have a higher priority than the TxCav, therefore, this request will be granted by the CP as soon as it completed all the cell receive requests. The 860sar UTOPIA implements the cell level handshake, therefore the PHY side should be able to receive a whole cell upon $\overline{\text{TxEnb}}$. The 860sar UTOPIA controller divide the cell transfers to small

sections of 4 bytes transfers (or less). and use the $\overline{\text{TxEnb}}$ to control that. For example, sequence of a 53 byte cell transfer is divided to the following UTOPIA transfer sections:

- Header transfer (4 octets)
- UDF (HEC) transfer (1 octet)
- cell body transfers (total of 48 octets)

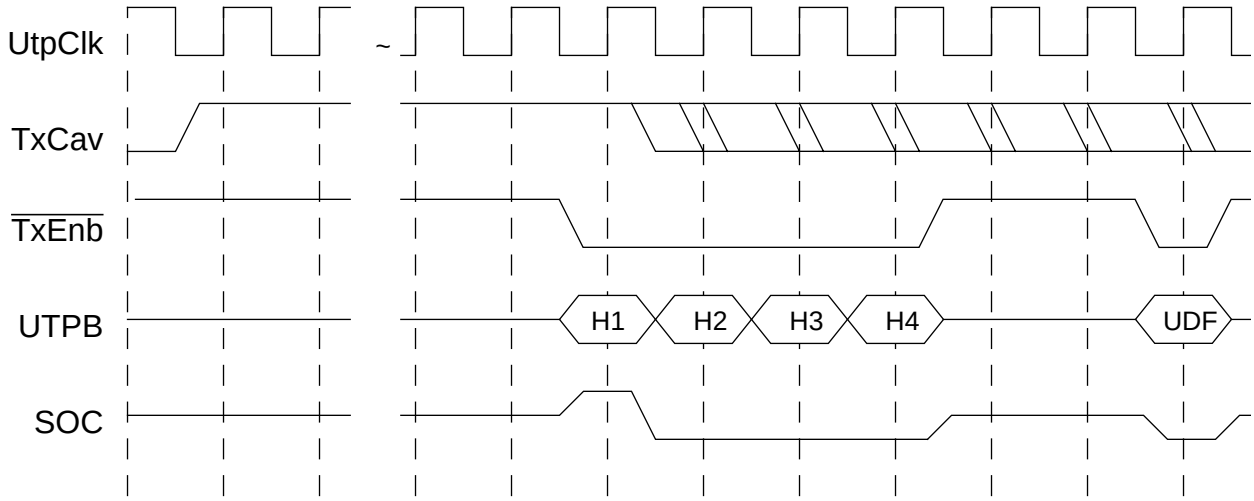
For each of the above sections section, the 860sar will assert the $\overline{\text{TxEnb}}$ and at the same time it will drive the UTOPIA bus (UTPB), TxSOC and TxPrty signals with valid data. For the UDF section, there will be only one octet transfer. All other sections will be 4 octet long.

4•4•0•3 UTOPIA Bus and SOC Drive

The UTOPIA bus (UTPB) and SOC signal will be driven by the 860sar only on Tx transfer and when $\overline{\text{TxEnb}}$ is asserted. Otherwise, the 860sar will keep UTPB and SOC tristated.

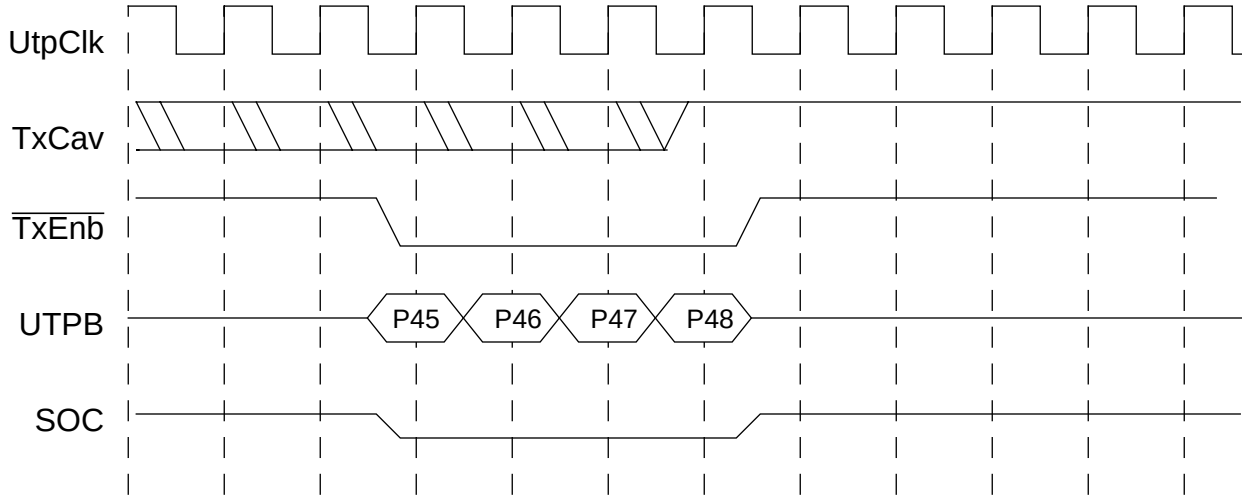
The start of cell transfer of 860sar is shown in Figure . Note that the TxCav is not sampled during the cell transfer.

FIGURE 4-4 Transmit UTOPIA start of cell



The end of cell transfer of 860sar is shown in Figure . In this example the PHY side was ready with additional cell, therefore it asserted TxCav immediately at the end of the cell transfer. The TxCav should be kept asserted until $\overline{\text{TxEnb}}$ will be asserted by the 860sar to indicate a transfer start of a new cell.

FIGURE 4-5 Transmit UTOPIA end of cell



4•5 860sar Signals

The 860sar system bus signals is identical to the MPC860 signals which described in MPC860 User Manual, chapter 2. In additional to MPC860 signals, additional 860sar signals were added to perform the UTOPIA interface, these signals are valid only under parallel mode, see 2.1.1.1 Port D Pin Assignment Register (PDPAR). This chapter summarize the 860sar additional pins.

PIN NAME	PIN NUMBER	DESCRIPTION
PB[15] BRGO3 **TXCAV**	R17	General-Purpose I/O Port B Bit 15—This is bit 15 of the general-purpose I/O port B. BRGO3—This is BRG3 output clock. **TXCAV—Tx Cell Available input signal.**
PC[15] DREQ1 $\overline{\text{RTS1}}$ L1ST1 **RXCAV**	D16	General-Purpose I/O Port C Bit 15—This is bit 15 of the general-purpose I/O port C. DREQ1—This is the IDMA channel 1 request input signal. RTS1—This is the Request to Send modem line for SCC1. L1ST1—This one of four output strobes that can be generated by the Serial Interface. **RXCAV—Rx Cell Available input signal**
PD[15] L1TSYNCA **UTPB[0]**	U17	General-Purpose I/O Port D Bit 15—This is bit 15 of the general-purpose I/O port D. L1TSYNCA—Input transmit data sync signal to the TDM channel A. **UTPB[0]—UTOPIA bus bit 0 input/output signal.**
PD[14] L1RSYNCA **UTPB[1]**	V19	General-Purpose I/O Port D Bit 14—This is bit 14 of the general-purpose I/O port D. L1RSYNCA—Input receive data sync signal to the TDM channel A. **UTPB[1]—UTOPIA bus bit 1 input/output signal.**
PD[13] L1TSYNCB **UTPB[2]**	V18	General-Purpose I/O Port D Bit 13—This is bit 13 of the general-purpose I/O port D. L1TSYNCB—Input transmit data sync signal to the TDM channel B. **UTPB[2]—UTOPIA bus bit 2 input/output signal.**

PD[12] L1RSYNCB **UTPB[3]**	R16	General-Purpose I/O Port D Bit 12—This is bit 12 of the general-purpose I/O port D. L1RSYNCB—Input receive data sync signal to the TDM channel B. **UTPB[3]—UTOPIA bus bit 3 input/output signal.**
PD[11] RXD3 **$\overline{\text{RXENB}}$**	T16	General-Purpose I/O Port D Bit 11—This is bit 11 of the general-purpose I/O port D. RXD3—Receive data for serial channel 3. **$\overline{\text{RXENB}}$ —Rx Enable output signal.**
PD[10] TXD3 **$\overline{\text{TXENB}}$**	W18	General-Purpose I/O Port D Bit 10—This is bit 10 of the general-purpose I/O port D. TXD3—Transmit data for serial channel 3. **$\overline{\text{TXENB}}$ —Tx Enable output signal.**
PD[9] RXD4 **UTPCLK**	V17	General-Purpose I/O Port D Bit 9—This is bit 9 of the general-purpose I/O port D. RXD4—Receive data for serial channel 4. **UTPCLK—UTOPIA Clock output signal.**
PD[7] RTS3 **UTPB[4]**	T15	General-Purpose I/O Port D Bit 7—This is bit 7 of the general-purpose I/O port D. RTS3—Active low request to send output indicates that SCC3 is ready to transmit data. **UTPB[4]—UTOPIA bus bit 4 input/output signal.**
PD[6] RTS4 **UTPB[5]**	V16	General-Purpose I/O Port D Bit 6—This is bit 6 of the general-purpose I/O port D. RTS4—Active low request to send output indicates that SCC4 is ready to transmit data. **UTPB[5]—UTOPIA bus bit 5 input/output signal.**
PD[5] REJECT2 **UTPB[6]**	U15	General-Purpose I/O Port D Bit 5—This is bit 5 of the general-purpose I/O port D. REJECT2—This input to SCC2 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match. **UTPB[6]—UTOPIA bus bit 6 input/output signal.**
PD[4] REJECT3 **UTPB[7]**	U16	General-Purpose I/O Port D Bit 4—This is bit 4 of the general-purpose I/O port D. REJECT3—This input to SCC3 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match. **UTPB[7]—UTOPIA bus bit 7 input/output signal. (most significant bit of UTPB)**
PD[3] REJECT4 **SOC**	W16	General-purpose I/O Port D Bit 3—This is bit 3 of the general-purpose I/O port D. REJECT4—This input to SCC4 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match. **SOC—Start Of Cell input/output signal.**

Boldface signals are the signals which were added in the 860sar. They are valid only in UTOPIA parallel mode.

4•6 PARALEL CONTROL BUS

The control bus is the bus that reads and writes the internal registers of the PM5346 and IDT77105 include the signals D0 - D7, A0 - A7, Read, Write, CS, IRQ, Reset and ALE. This board use all the control bus signals from the 860SAR I/O ports. The following table show the relation between the wanted signal to the 860SAR I/O pin. NOTE that the A0 - A7 and D0 - D7 signals are muxed and the ALE signal is used to latch the address.

The board will supplied with a set of commands which let the user to access the internal registers of the PM5346 and the IDT77105. These commands perform the read write cycle of the devices.
The user should remember not to use these pins to it's uses.

Table 4-1 86SAR I/O pins Related to Control Bus

PM5346/IDT77105 control bus signal	MPC860SAR
ADD/DATA0	PC8
ADD/DATA1	PC9
ADD/DATA2	PA1
ADD/DATA3	PA3
ADD/DATA4	PB16
ADD/DATA5	PB17
ADD/DATA6	PA8
ADD/DATA7	PA9
READ~	PB18
WRITE	PC12
ALE	PB14
RESET~	PB26
CS~	PB27
IRQ~	IRQ2

4•7 PM5346 S/UNI - 155 - LITE

The PM5346 is a Saturn User Network Interface 155.52 & 51.84 Mb/s.
The PM5346 is a monolitic integrated circuit that implements the SONET/SDH processing and ATM mapping functions of 155Mbps or 51Mbps ATM User Network Interface. it is fully compliant with both SONET and SDH requirements and ATM Forum UNI specification.

The S/UNI-LITE receives SONET/SDH frames via a bit serial interface, recovers clock and data, and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions and monitors section, line and path bit interleaved parity (B1,B2,B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1)are also accumulated. The S/UNI-LITE interprets the received payload pointers (H1,H2)and extracts the synchronous payload envelop which carrier the received ATM cell payload.

The S/UNI LITE frames to the ATM payload using cell delineation. HCS error correction is provided. idle/ unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrecteble header check sequence error. The ATM cell payload are descrambling. Generic Flow control (GFC) bits from error free cells are extracted and presented on the serial link for external processing.

Legitimate ATM cells are written to a four cell FIFO buffer. These cells are read from the FIFO using a synchronous 8 bit wide datapath interface with cell-based handshake. Counts of received ATM cell headers that are errored and uncorrecteble, those that are errored and correctable and all passed cells are accumulated independently for performance monitoring purposes.
The S/UNI-LITE transmits SONET/SDH frames via a bit serial interface and formats section, line and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and create section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and far end block error indications (Z2, G1) are also inserted.
The S/UNI-LITE generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carriers the ATM cell payload. It supports the insertion of a variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostic.

ATM cells are written to an internal programmable - length 4 -cell FIFO using a synchronous 8 bit data path interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less then one cell or the XOFF input is asserted. Generic Flow Control (GFC) bits may be inserted downstream of the FIFO via a serial link so that all FIFO latency may be bypassed.
The S/UNI-LITE generates of the header check sequence and scrambles the payload of the ATM cells. Payload scrambling can be disable.

4•8 ATM25.6 IDT77105

The IDT 77105 is like the PM5346 but it is an ATM 25.6Mbps. It has the same UTOPIA bus and the same control bus.
The IDT77105 perform the following features

PHY Transmission Converence (TC) and Physical Media Dependent (PMD) Sublayer functions for 25.6Mbps ATM Networks.
The IDT77105 implements the physical layer standard for 25.6Mbps ATM network communications. The physical layer decided into two sections PMD and TC. The PMD include the functions for transmit, receive and clock recovery that allow connection to transmission media conforming to TIA/EIA 568. The TC defines the line coding, scrambling, data framing and synchronization.

UTOPIA (Universal Test & Operations PHY Interface for ATM) Interface.
is used as the data path interface between the IDT77105 and the 860SAR.

Two - cell Transmit and Receive FIFOs.

Two Loop Back modes.
Line loop back mode Enables the user to connect its instrument to board (IDT77105), send data and get it back.
PHY loop back Mode Enables the user to send data from the 860SAR via the utopia bus and get it back.

The Receive data bus and Transmit data bus can be connected together.

LED interface for status signaling support the Unshielded Transmission Convergence (UTP)
Category 3 (CAT 3) Physical Media.

Interface to standard magnetics.

4•9 E1 2.048Mbps or T1 1.544Mbps

The 860SAR also implements the ATM protocol in serial mode, via one of the SCCs. This serial interface is E1 or T1 (DS1). The 860SAR perform the AAL5, AAL0, SAR and TC sublayer. In order to perform the E1/T1 we use DS2180AQ for T1 or DS2181AQ for E1 they both use the same socket, which mean if the user wants to use T1 he will put DS2180AQ in the socket or if he wants to use E1 he will put the DS2181AQ in the socket (U13). The DS2180/DS2181 is controlled by the 860SAR via the SPI port, via this port the 860SAR read and write to the framer internal registers. The ATM data is transferred by the 860SAR TDMb port pins according to the next table.

Table 4-2 MPC860SAR-PHY E1/T1 Signals

E1/T1 Signal	860SAR PIN PORT
L1TCLKB	PA0
L1RCLKB	PA2
L1RXDB	PA10
L1TXDB	PA11
L1RSYNCB	PC6
L1TSYNCB	PC7

Another two devices are used for the line interface one for receive DS2187 and the second is for the transmit DS2186. The selection from E1 or T1 has been done by dip switch (DS1(8)).

4•9•1 DS2180 T1 / DS2181 FRAMER.

The DS2180 is used to perform T1 transceiver. DS2181 is used to perform E1 framer. The ATM data from the 860SAR is transferred over the T1 line. The DS2180/DS2181 scramble and descrambling the in and out data, it is also provide the RSYNC signal from the incoming data. It is also provide an interrupt to indicate of a line problems. Through the SPI the 860SAR can read the internal registers. NOTE: that for a T1 the DS2180 should be in U13 or DS2181 for E1.

4•9•2 DS2187 RECEIVER and DS2186 TRANSMITER Line Interface

The DS2186 and DS2187 are line interface they can work with E1 and T1. The E1/T1 selection is done by DS1(8).

4•9•2•1 DS2186 Transmit Line Interface.

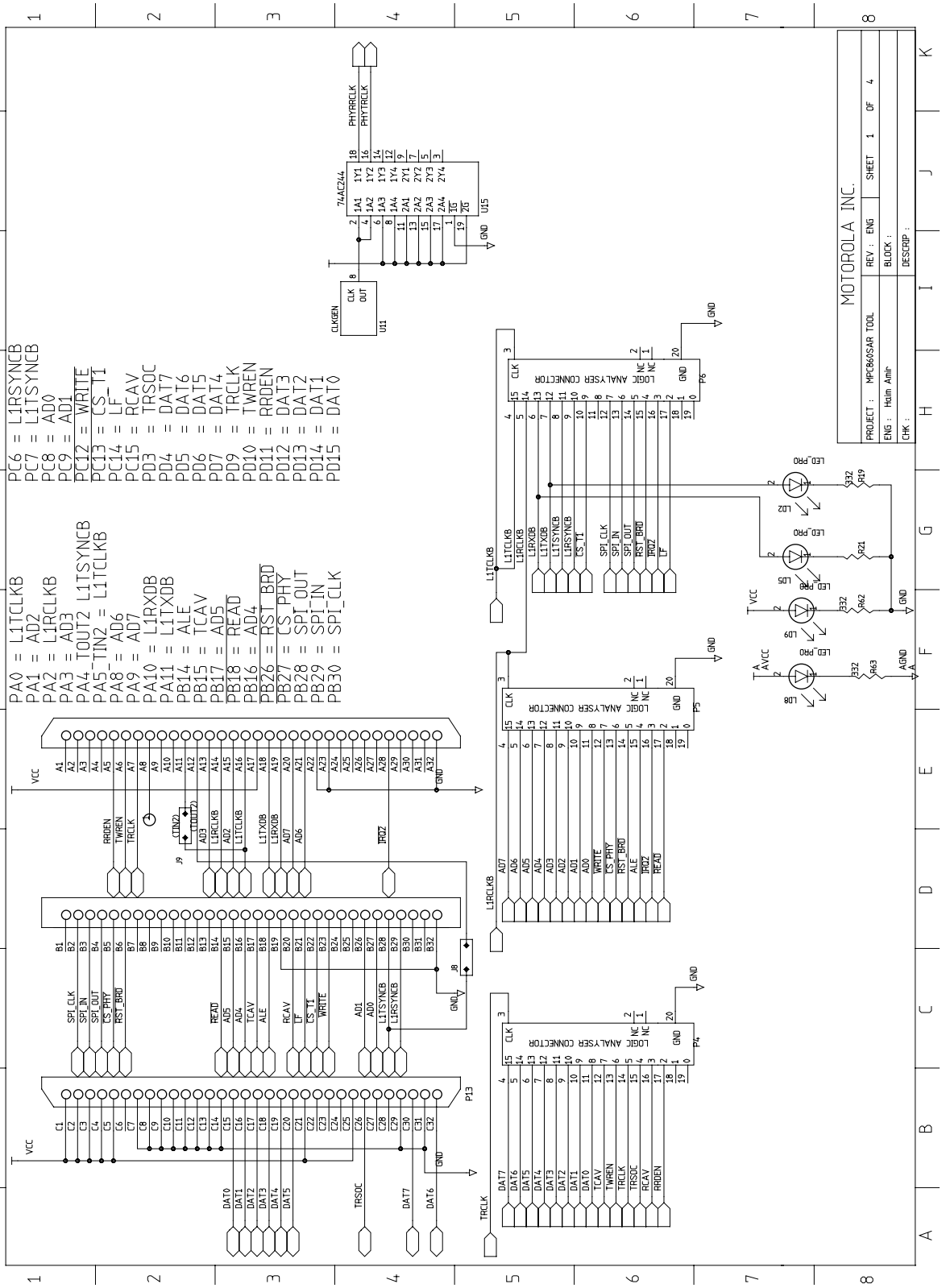
The device is compatible with all types of twisted pair cable and also a variety of line length. It is possible to perform a line loop back for the in coming data. In the line loop back it gets its data from LNEG and LPOS. The DS2186 designed to operate in NRZ if the user wants to perform the B8ZS he should program the DS2180/DS2181 for such a thing.

4•9•2•2 DS2187 Receive Line Interface.

The device extracts clock and data from twisted pair. The DS2187 has two mods of operations.
1. is when there is no line connection in this mode the DS2187 supplies the RCLK from its internal clock oscillator.
2. When there is a line connection the device recover the T1/E1 clock from the in coming data and out put it on the RCLK pin. Actually this is the main clock in the T1/E1 operation in the most of the user uses.

4•10 SCHEMATCS DESCRIPTION

FIGURE 4-6 SHEET #1 ADS and LOGIC connectors

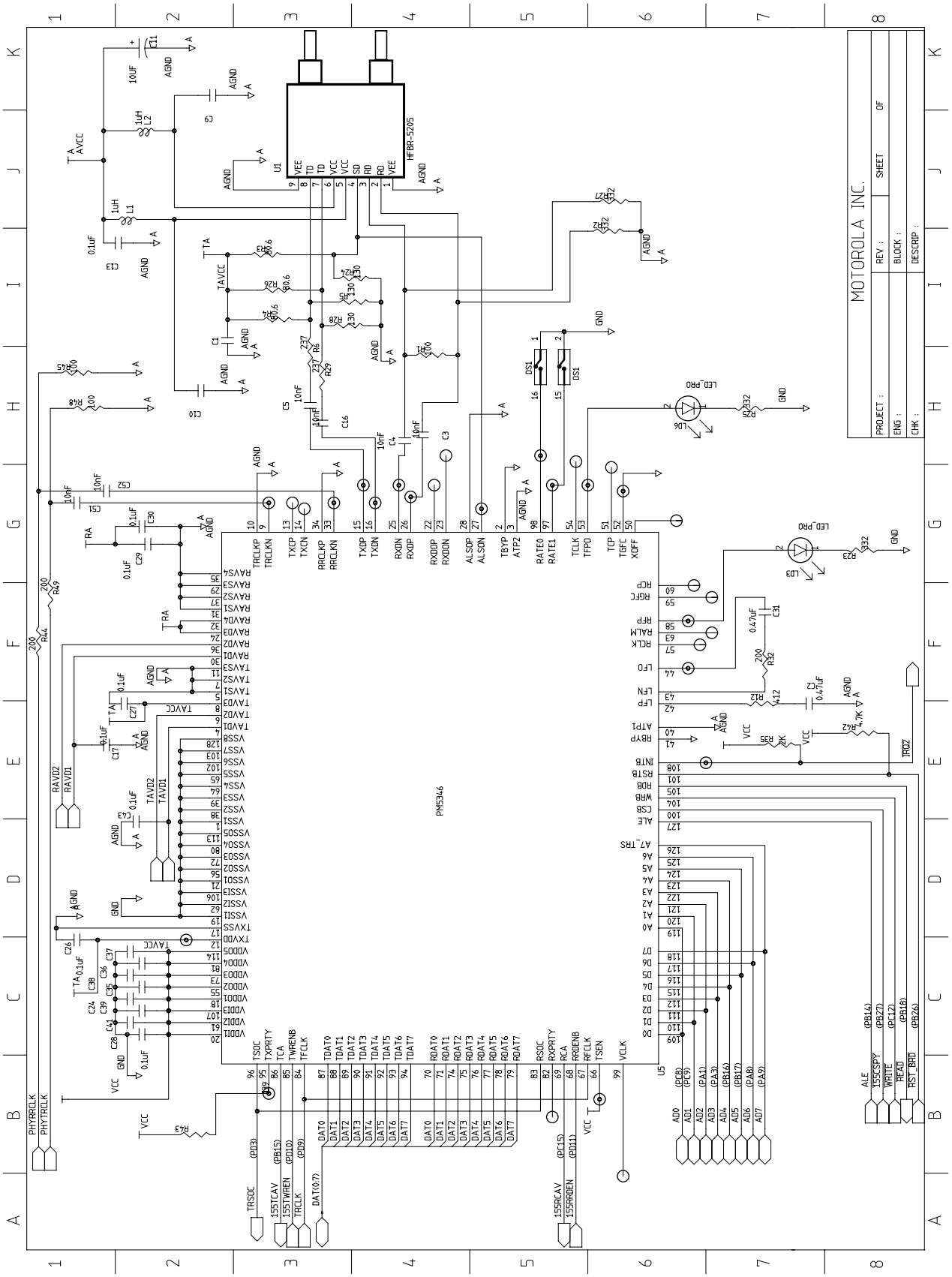


4•10•1 SHEET #1 ADS and LOGIC connectors.

Sheet #1 consist of the M860ADS (or 8xxFADS) ports connector, Logic analyzer connectors.
The ADS connector consist all the pins that needed to operate the board.

Note that all the pins are ports pins and the user can not use these pins for his HW application.
TIN2, TOUT2, L1TCLKB and L1TSYNCB The only pins he can use for general I/O are the TIN2, TOUT2, L1TCLKB and L1TSYNCB under the following conditions.
If the DS2187 RCLK signal and DS2180/81 RSYNC are used by jumpers, J6 and J7, connecting pins 1, 2 for L1TCLKB and L1TSYNCB. In this case TOUT2 and TIN2 can be used for user general I/O.
L1TCLKB and L1TSYNCB can also be used for general I/O if the user set the 860SAR SIMOD REGISTER bit CRTB, by setting this bit the user force internally the incoming L1RCLKB to L1TCLKB and L1RSYNC to L1TSYNCB. In this case the pins PA4, PA5, PA11 and PC7 are free to the user's use.
TIN2 and TOUT2 together with U12 has been made for getting external clock to the L1TCLKB. The board will be supply with two clock oscillators one is a 1.544Mhz for T1 and the second is a 2.048Mhz for E1. By connecting J9 pins 1,2 the 860SAR gets a clock to TIN2 pin and generating TOUT2, by connecting J8 pins 1, 2 TOUT2 is forced to L1TSYNCB and to the T1/E1 circuit.
SIGNAL LIST. The list of all the 860SAR ports and there relation to the board signals is in this sheet.
LOGIC ANALYZER All the require signals are connected to a logic analyzer connectors, the signals are splitted to groups. The groups are: UTOPIA bus consist of the data bus and all the utopia control pins, These pins are in P4.
Control bus consist of the needed pins to read and write from and to the PM5346 and IDT77105, these pins are in P5.
E1/T1 pins. This connector consist all the E1/T1 pins include the control SPI port pins.

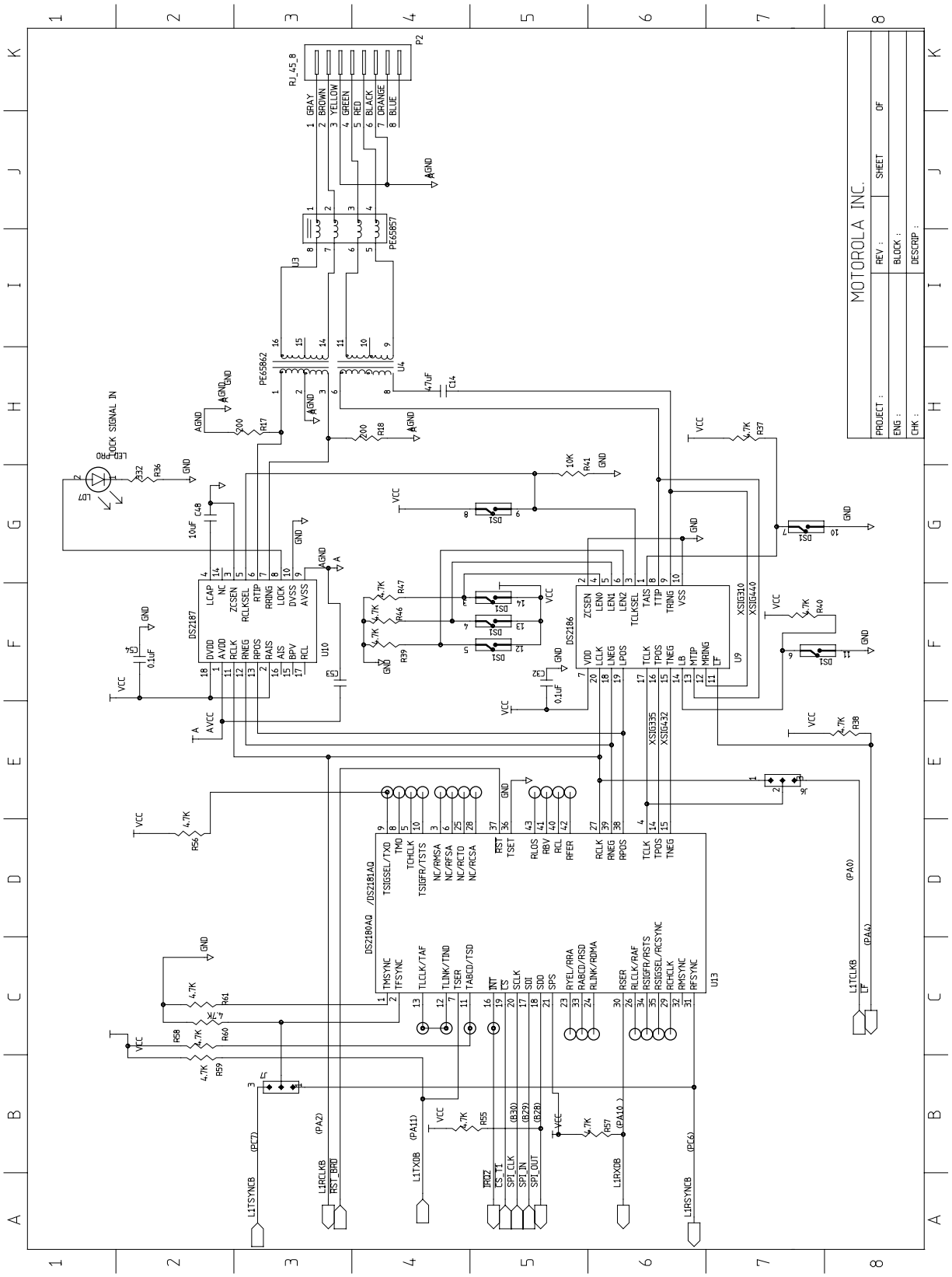
FIGURE 4-7 SHEET #2 ATM155.52/51.84Mbps Transceiver.



4•10•2 SHEET #2 ATM155.52/51.84Mbps.

Sheet #2 has the PM5346, S/UNI-LITE and the line optical transceiver, HFBR-5205.
DS1(1,2) are select the frequency operation of the ATM line, if this dip switches are off the PM5346 is configured to operate in 155.52Mbps if DS1(2) is ON it will configure the PM5346 to 51.8Mbps.
NOTE: The in coming optical line (Line Out) from the user target should be connected to RX in the optical line transceiver and the Line in to the user target should be connected to the TX of the line optical transceiver.

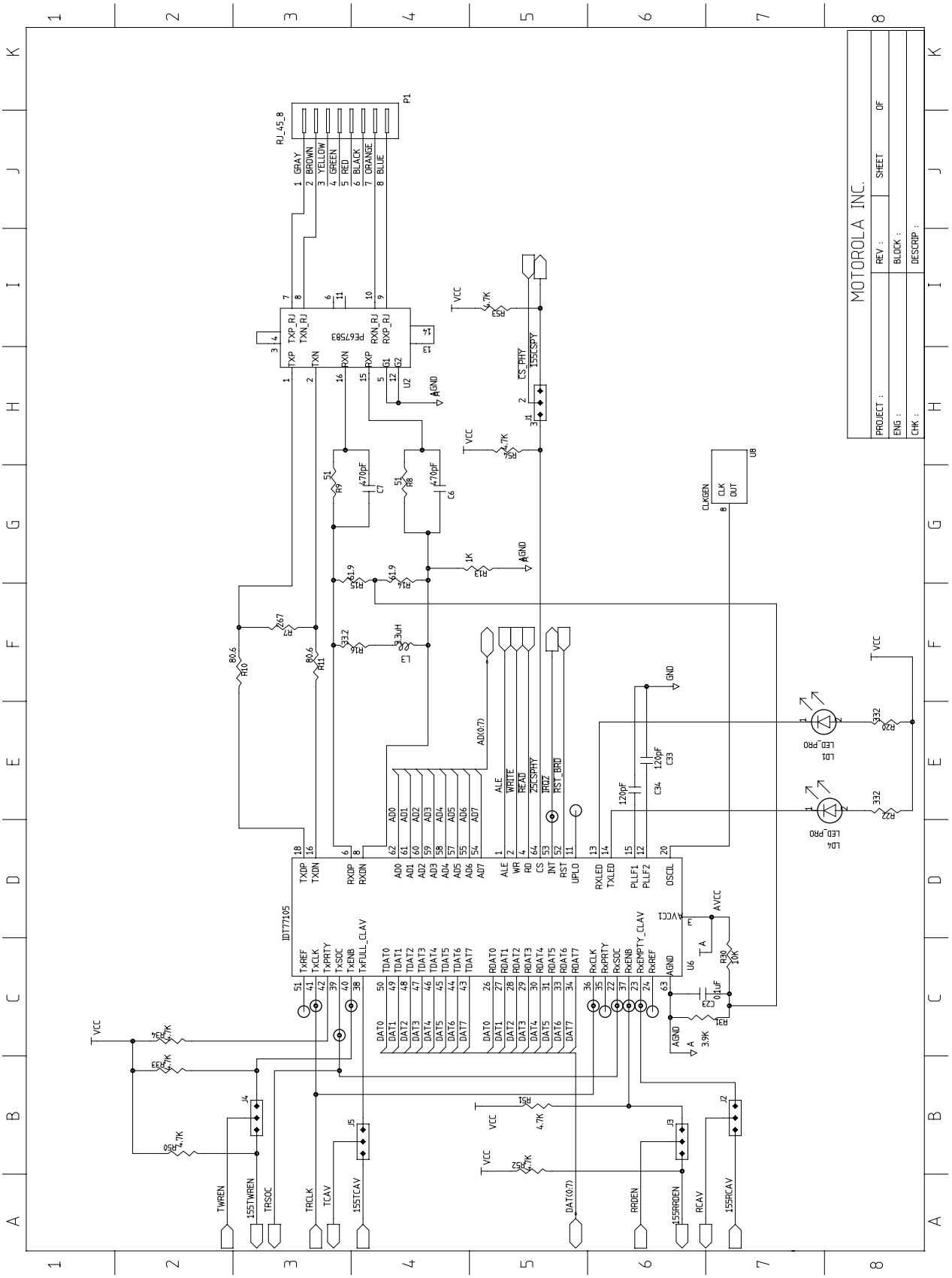
FIGURE 4-8 E1/T1



4•11 Sheet #3

Sheet #3 consist the E1/T1 circuit includes the framer, DS2181/DS2180 and the line interface drivers for transmit DS2186 and for receive DS2187.
The DS2187 recover the RCLK from the in coming data, the RCLK is routed to the board. The RCLK signal can be use for the TCLK by connecting J6 pins 1, 2. The clock recovery depend on DS1(8) this dip switch cause to the DS2187 to output the right clock for E1 (ON) or for T1 (OFF). The DS2187 has a lock signal pin, this pin connected to LED7 it indicates when a line with data is connected to the board.
The DS2186 is the line transmitter. It can be config to a line loop back, (DS1(6)) by setting this dip switch to off the LNEG and LPOS are transmitted to the TTIP and TRING signals.
The DS2186 support a different line length. DS1(1,2,3) confides the line length. The default is ON. ON. OFF the options length are shone in the previous chapters.
DS2180/DS2181 (U13) Actually the user should use one of them. If T1 was chosen the device should be DS2180 if E1 was chosen the device should be DS2181. The DS2180/DS2181 produce the RSYNC signal it is possible to use this signal to the TSYNC by connecting J7 pins 1, 2 and config the 860sar to use the TSYNC from the RSYNC.
The DS2180/DS2181 is controlled by the SPI port. Through this port the user can read and write the internal register and config the device.

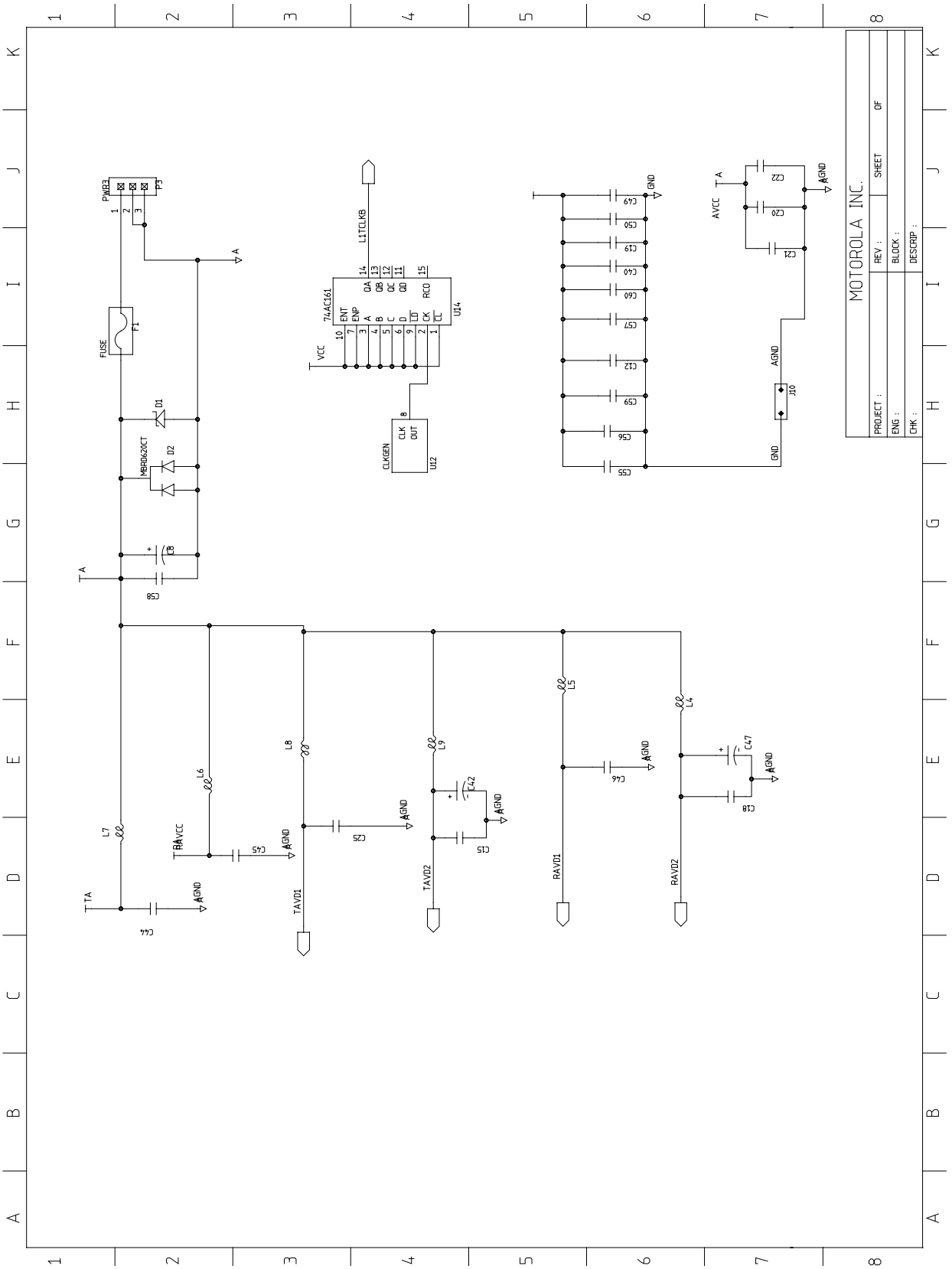
FIGURE 4-9 SHEET #4 ATM25.6Mbps



4•12 Sheet #4

Sheet #4 consist the ATM25.6Mbps it implemented by the IDT77107 device and PE67583 Magnetics for the line interface. Five jumpers are in this draw they made to select the ATM155M or ATM25M if all the five jumpers are connected in pins 1,2 the ATM155M is selected otherwise the ATM25M is selected.
NOTE: the input control pins of the IDT77105 and PM5346 are puled up to prevent data bus collision.

FIGURE 4-10 SHEET #5 POWER



4•13 SHEET #5

SHeet #5 consist of the POWER circuit. The power circuit compose of DIGITAL power and ANALOG power. The PM5346 requires 6 separate analog power: RAVD1, RAVD2, TAVD1, TAVD2, transmit analog (TA) and receive analog (RA). The separate has been done by a ferrit beeds as shown in the draw above. The Analog VCC (A) is for the rest of the analog power of the board.

CHAPTER 5 - SUPPORT INFORMATION

5•1 INTRODUCTION

This chapter provides the interconnection signals and the parts list of the MPC860SAR-PHY board.

5•2 INTERCONNECT SIGNALS

The MPC860SAR-PHY board interconnects with external devices through the following connectors:

- U1 is the optical line transceiver (HFBR 5205) for the ATM155.52/51.84Mbps.
- P1 is a 8 pin, RJ-45 connector for the ATM25.6Mbps connect as a user interface.
- P2 is a 8 pin, RJ-45 connector for the E1/T1 2.048/1.544Mbps.
- P3 is 3 pin connector for 5v analog power supply input: GND (x2) and +5V
- PD4 - PD6 are 3x20 pin, male connectors, compatible with HP logic analyzer connectors, that provides all the signals of the Utopia, SPI and E1/T1 signals monitoring.

Table 5-1 MPC860SAR-PHY Parts List

Table 5-1 PART LIST

Reference	Value/NAME	MSILPRTNUM	Total
C1 C9 C10 C12 C13 C15 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C32 C35 C36 C37 C38 C39 C40 C41 C43 C44 C45 C46 C49 C50 C53 C54 C55 C56 C57 C58 C59 C60	0.1uF	021-00064	42
C2 C31	0.47uF	021-00113	2
C3 C4 C5 C16 C51 C52	10nF	021-00070	6
C6 C7	470pF	021-00066	2
C8 C14	47UF	023-00037	2
C11 C42 C47 C48	10UF	023-00027	4
C33 C34	120pF	021-00069	2
D1	1SMC5.0AT3	048-1SMC12AT3	1
D2	MBRD620CT	048-MBRD640CT	1
DS1		040-00027	1
F1	2.5A	065-00???	1
F1	HOSE	015-00014	1
J1 J2 J3 J4 J5 J6 J7	JH3	028-00151	7
J8 J9	JMP2P	028-00155	2/1
L1 L2 L4 L5 L6 L7 L8 L9	1uH	024-00013	8
L3	3.3uH	024-00026	1
LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8 LD9	LED 1mA	048-01005	9
P1 P2	RJ_45_8	009-00236	2
P3	PWR3	028-00094	1
P3	PWR3	009-00208	1
P4 P5 P6	LOGIC20CON	028-00182	3

Table 5-1 PART LIST

Reference	Value/NAME	MSILPRTNUM	Total
P13	96CONN FEMAL	028-00144	1
R1 R45 R48	100	006-00240	3
R2 R19 R20 R21 R22 R23 R25 R27 R36 R62 R63	332	006-00237	11
R3 R4 R10 R11 R26	80.6	006-00315	5
R5 R24 R28	130	006-00337	3
R6 R29	237	006-00336	2
R7	267	006-00342	1
R8 R9	51.1	006-00221	2
R12	412	006-00338	1
R13	1K	006-00257	1
R14 R15	61.9	006-00340	2
R16	33.2	006-00286	1
R17 R18 R32 R44 R49	200	006-00296	5
R30 R41	10K	006-00235	2
R31	3.9K	006-00308	1
R43 R46 R47 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61	4.7K	006-00261	22
R35	2K	006-00???	1
U1	HFBR-5205	051-HFBR-5205	1
U2	PE67583	051-PE67583	1
U3	PE65857	051-PE65857	1
U4	PE65862	051-PE65862	1
U5	PM5346	051-PM5346	1
U6	IDT77105	051-IDT77105	1
U8	32Mhz CLKGEN	048-00087	1
U9	DS2186	051-DS2186	1
U10	DS2187	051-DS2187	1
U11	19.44/6.48Mhz CLKGEN	048-00092 048-00093	1+1
U12	1.544/2.048Mhz CLKGEN	048-00094 048-00095	1+1
U12 U8 U11 SOCKET	14 PIN SOCKET SMD	009-00???	1
U13	DS2180AQ	051-DS2180AQ	1
U13 44 PIN SOCKET	44 PIN SOCKET	009-003?????	1
U15	74AC244	051-74AC244	1

Table 5-1 The MPC860SAR-PHY nettlist

/0486 U11(8) U15(4) U15(2);

/0609 LD9(1) R62(1);
/0621 LD5(1) R21(1);
/0622 LD2(1) R19(1);
/0631 I63(1) P13(A8);
/0686 LD8(1) R63(1);
/0744 J8(2) P13(A12);
/0745 J9(2) P13(A11);
/1375 C16(2) R29(2);
/1377 R4(1) R5(2) R6(1) U1(8);
/1378 C5(2) R6(2);
/1383 R26(1) R28(2) R29(1) U1(7);
/1386 C4(2) R1(2) R27(2) U1(3);
/1393 C3(2) R1(1) R2(2) U1(2);
/1442 C10(2) L1(2) U1(5);
/1448 C9(2) L2(2) U1(6);
/1461 C51(2) R48(2) R49(1);
/1462 C52(2) R44(1) R45(2);
/1508 C31(1) R32(1);
/1510 R12(1) U5(42);
/1512 C2(2) R12(2);
/1621 C31(2) I14(1) U5(44);
/1622 R32(2) U5(43);
/1626 I1(1) R3(1) R24(2) U1(4) U5(27);
/1628 C3(1) I2(1) U5(26);
/1629 C4(1) I4(1) U5(25);
/1630 C16(1) I6(1) U5(16);
/1631 C5(1) I8(1) U5(15);
/1637 I18(1) U5(54);
/1639 I10(1) U5(51);
/1640 I12(1) U5(50);
/1642 I5(1) U5(22);
/1643 I3(1) U5(23);
/1644 I7(1) U5(13);
/1645 I15(1) U5(14);
/1647 I16(1) U5(57);
/1648 I24(1) U5(63);
/1650 I17(1) U5(59);
/1651 I20(1) U5(60);
/1652 C51(1) I22(1) U5(9);
/1655 C52(1) I21(1) U5(33);
/1658 I32(1) U5(99);
/1669 DS1(16) I40(1) U5(98);
/1670 DS1(15) I41(1) U5(97);

/1728 I19(1) LD3(2) U5(58);
/1729 I11(1) LD6(2) U5(53);
/1730 LD3(1) R23(1);
/1731 LD6(1) R25(1);
/1739 I39(1) R43(1) U5(95);
/2302 R17(2) U4(1) U10(6);
/2304 R18(1) U4(3) U10(7);
/2305 U3(8) U4(16);
/2307 U3(6) U4(11);
/2311 C14(1) U4(8);
/2312 C48(1) U10(4);
/2344 DS1(5) R39(2) U9(6);
/2356 DS1(4) R46(2) U9(5);
/2401 DS1(3) R47(2) U9(4);
/2453 U9(19) U10(13) U13(38);
/2494 P2(1) U3(1);
/2495 P2(2) U3(2);
/2496 P2(4) U3(3);
/2497 P2(5) U3(4);
/2499 U3(7) U4(14);
/2501 U3(5) U4(9);
/2517 DS1(6) R40(2) U9(14);
/2535 I48(1) U13(29);
/2536 I52(1) U13(35);
/2537 I51(1) U13(34);
/2538 I44(1) U13(26);
/2542 I58(1) U13(8);
/2543 I59(1) U13(5);
/2544 I54(1) U13(10);
/2545 I64(1) U13(43);
/2546 I61(1) U13(41);
/2547 I60(1) U13(40);
/2548 I62(1) U13(42);
/2550 I46(1) U13(24);
/2551 I49(1) U13(33);
/2552 I47(1) U13(23);
/2555 I50(1) I55(1) U13(13) U13(12);
/2556 I53(1) R56(2) U13(9);
/2559 I56(1) R58(2) U13(11);
/2568 DS1(9) R41(1) U9(3) U10(5);
/2576 LD7(1) R36(1);
/2577 LD7(2) U10(8);
/2594 I65(1) U13(3);

/2595 I66(1) U13(6);
/2596 I45(1) U13(25);
/2597 I43(1) U13(28);
/2623 R61(2) U13(1);
/2625 J7(2) R60(2) U13(2);
/2656 J6(2) U9(17) U13(4);
/3292 R10(1) U6(18);
/3293 R7(2) R11(2) U2(2);
/3298 R11(1) U6(16);
/3304 C34(1) U6(15);
/3305 C33(1) U6(12);
/3309 L3(1) R16(2);
/3318 C7(1) R9(1) R15(1) R16(1) U6(6);
/3319 C7(2) R9(2) U2(16);
/3323 R7(1) R10(2) U2(1);
/3325 C6(1) L3(2) R8(1) R13(1) R14(2) U6(8);
/3327 C6(2) R8(2) U2(15);
/3332 U2(13) U2(14);
/3333 U2(4) U2(3);
/3344 C23(2) R14(1) R15(2) R30(2) R31(2);
/3349 P1(1) U2(7);
/3350 P1(2) U2(8);
/3374 J5(3) U6(38);
/3429 LD4(1) U6(14);
/3430 LD1(1) U6(13);
/3431 LD4(2) R22(1);
/3432 LD1(2) R20(1);
/3460 I29(1) U6(24);
/3461 I23(1) U6(11);
/3462 I34(1) U6(51);
/3468 R34(1) U6(42);
/3491 I42(1) J3(3) R51(1) U6(37);
/3492 I28(1) J2(3) U6(23);
/3493 I35(1) J4(3) R33(1) U6(40);
/3512 P1(7) U2(10);
/3513 P1(8) U2(9);
/3524 I36(1) U6(35);
/4312 F1(2) P3(1);
/4437 U12(8) U14(2);
/25CSPHY~ J1(3) R54(2) U6(64);
/155CSPY~ J1(1) R53(2) U5(100);
/155RCAV J2(1) U5(69);
/155RRDEN J3(1) R52(1) U5(68);

/155TCAV J5(1) U5(86);
/155TWREN J4(1) R50(1) U5(85);
/AD0 P5(11) P13(B27) U5(119) U5(109) U6(62);
/AD1 P5(10) P13(B26) U5(120) U5(110) U6(61);
/AD2 P5(9) P13(A15) U5(111) U5(121) U6(60);
/AD3 P5(8) P13(A13) U5(112) U5(122) U6(59);
/AD4 P5(7) P13(B16) U5(123) U5(115) U6(58);
/AD5 P5(6) P13(B15) U5(124) U5(116) U6(57);
/AD6 P5(5) P13(A21) U5(125) U5(117) U6(55);
/AD7 P5(4) P13(A20) U5(126) U5(118) U6(54);
/AGND C1(1) C2(1) C8(2) C9(1) C10(1) C11(2) C13(1) C15(1) C17(2)
C18(1) C20(1) C21(1) C22(1) C23(1) C25(1) C26(1) C27(1) C29(2)
C30(2) C42(2) C43(1) C44(1) C45(1) C46(1) C47(2) C53(2) C58(1)
D1(2) D2(1) D2(3) J10(1) P2(3) P2(6) P3(3) P3(2) R2(1) R5(1)
R13(2) R17(1) R18(2) R24(1) R27(1) R28(1) R31(1) R45(1) R48(1)
R63(2) U1(1) U1(9) U2(5) U2(12) U4(2) U5(7) U5(28) U5(31) U5(29)
U5(3) U5(37) U5(34) U5(17) U5(5) U5(35) U5(11) U5(10) U5(40) U6(63)
U10(9);
/ALE P5(15) P13(B18) U5(127) U6(1);
/AVCC C8(1) C11(1) C13(2) C20(2) C21(2) C22(2) C53(1) C58(2) D1(1) D2(4)
F1(1) L1(1) L2(1) L4(1) L5(1) L6(1) L7(1) L8(2) L9(1) LD8(2) R30(1)
U6(5) U6(9) U6(3) U6(7) U10(1);
/CS_PHY~ J1(2) P5(13) P13(B5);
/CS_T1~ P6(10) P13(B22) U13(19);
/DAT0 P4(11) P13(C15) U5(87) U5(70) U6(26) U6(50);
/DAT1 P4(10) P13(C16) U5(88) U5(71) U6(27) U6(49);
/DAT2 P4(9) P13(C17) U5(74) U5(89) U6(48) U6(28);
/DAT3 P4(8) P13(C18) U5(90) U5(75) U6(29) U6(47);
/DAT4 P4(7) P13(C19) U5(91) U5(76) U6(30) U6(46);
/DAT5 P4(6) P13(C20) U5(92) U5(77) U6(31) U6(45);
/DAT6 P4(5) P13(C32) U5(93) U5(78) U6(44) U6(33);
/DAT7 P4(4) P13(C30) U5(94) U5(79) U6(43) U6(34);
/GND C12(1) C19(1) C24(1) C28(1) C32(2) C33(2) C34(2) C35(1) C36(1)
C37(1) C38(1) C39(1) C40(1) C41(1) C48(2) C49(1) C50(1) C54(2)
C55(1) C56(1) C57(1) C59(1) C60(1) DS1(11) DS1(2) DS1(1) DS1(10)
I13(1) J10(2) P4(20) P5(20) P6(20) P13(C9) P13(C29) P13(C12) P13(C10)
P13(C31) P13(C11) P13(A32) P13(A23) P13(B32) P13(B19) P13(C13) P13(A22)
P13(C8) P13(C14) P13(C7) R19(2) R21(2) R23(2) R25(2) R36(2) R39(1)
R41(2) R46(1) R47(1) R60(1) R61(1) R62(2) U5(39) U5(52) U5(102) U5(47)
U5(19) U5(48) U5(38) U5(49) U5(64) U5(2) U5(113) U5(21) U5(62) U5(103)
U5(46) U5(106) U5(65) U5(128) U5(1) U5(80) U5(72) U5(56) U5(45) U5(41)
U6(32) U6(21) U6(19) U8(7) U9(2) U9(10) U10(3) U10(10) U11(7) U12(7)
U13(22) U13(36) U14(8) U15(10) U15(1);

/IRQ2~ I27(1) I33(1) I57(1) P5(16) P6(16) P13(A28) R35(1) U5(108) U6(53) U13(16);
/L1RCLKB J6(1) P5(3) P6(5) P13(A14) U9(20) U10(11) U13(27);
/L1RSYNCB J7(1) P6(9) P13(B29) U13(31);
/L1RXDB LD5(2) P6(6) P13(A19) R57(2) U13(30);
/L1TCLKB J6(3) J9(1) P6(4) P6(3) P13(A16) U14(14);
/L1TSYNCB J7(3) J8(1) P6(8) P13(B28);
/L1TXDB LD2(2) P6(7) P13(A18) R59(2) U13(7);
/LF~ P6(17) P13(B21) R38(2) U9(11);
/PHYRRCLK R44(2) U15(18);
/PHYTRCLK R49(2) U15(16);
/PRTY_OUT I31(1) U5(82);
/RAVCC C29(1) C30(1) C45(2) L6(2) U5(24) U5(32);
/RAVD1 C17(1) C46(2) L5(2) U5(30);
/RAVD2 C18(2) C47(1) L4(2) U5(36);
/RCAV J2(2) P4(16) P13(B20);
/RDATA67 U9(18) U10(12) U13(39);
/READ~ P5(17) P13(B14) U5(105) U6(4);
/RRDEN J3(2) P4(17) P13(A5);
/RST_BRD~ P5(14) P6(15) P13(B6) R42(1) U5(101) U6(52) U13(37);
/SPI_CLK P6(12) P13(B2) U13(20);
/SPI_IN P6(13) P13(B3) U13(17);
/SPI_OUT P6(14) P13(B4) R55(2) U13(18);
/TAIS DS1(7) R37(2) U9(1);
/TAVCC C1(2) C26(2) C27(2) C44(2) I9(1) L7(2) R3(2) R4(2)
R26(2) U5(8) U5(12);
/TAVD1 C25(2) C43(2) L8(1) U5(4);
/TAVD2 C15(2) C42(1) L9(2) U5(6);
/TCAV J5(2) P4(12) P13(B17);
/TRCLK I26(1) I38(1) P4(3) P4(14) P13(A7) U5(67) U5(84) U6(36) U6(41);
/TRSOC I30(1) I37(1) P4(15) P13(C26) U5(83) U5(96) U6(22) U6(39);
/TWREN J4(2) P4(13) P13(A6);
/VCC C12(2) C19(2) C24(2) C28(2) C32(1) C35(2) C36(2) C37(2) C38(2)
C39(2) C40(2) C41(2) C49(2) C50(2) C54(1) C55(2) C56(2) C57(2)
C59(2) C60(2) DS1(14) DS1(12) DS1(13) DS1(8) I25(1) LD9(2) P13(A17)
P13(C2) P13(C1) P13(C5) P13(C25) P13(C3) P13(C4) P13(C21) R20(2) R22(2)
R33(2) R34(2) R35(2) R37(1) R38(1) R40(1) R42(2) R43(2) R50(2) R51(2)
R52(2) R53(1) R54(1) R55(1) R56(1) R57(1) R58(1) R59(1) U5(81) U5(73)
U5(20) U5(61) U5(55) U5(66) U5(107) U5(114) U5(18) U6(56) U6(25) U8(14)
U8(11) U9(7) U10(2) U10(18) U11(14) U11(11) U12(14) U12(11) U13(21) U13(44)
U14(4) U14(6) U14(7) U14(3) U14(9) U14(5) U14(10) U14(16) U14(1) U15(8)
U15(13) U15(11) U15(20) U15(6) U15(17) U15(19) U15(15);
/WRITE~ P5(12) P13(B23) U5(104) U6(2);
/XSIG310 C14(2) U9(9) U9(12);

/XSIG335 U9(16) U13(14);
/XSIG432 U9(15) U13(15);
/XSIG440 U4(6) U9(8) U9(13);
/XSIG454 U6(20) U8(8)

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