

KIT33660EFEVBE Evaluation Board

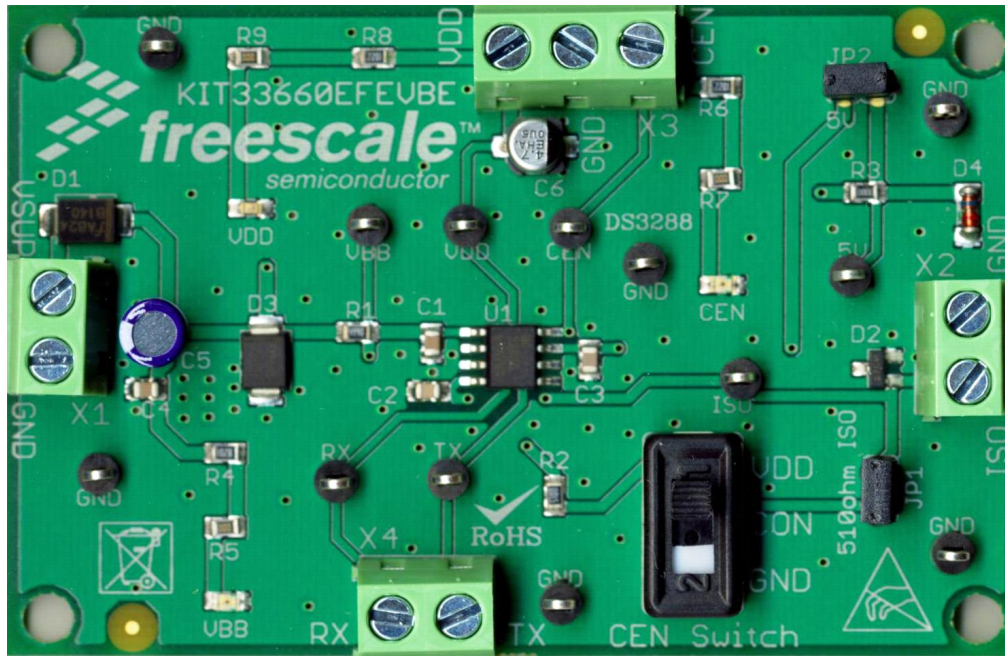


Figure 1. KIT33660EFEVBE

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1 Kit Contents / Packing List

- KIT33660EFEVBE Evaluation Board

2 Important Notice

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

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3 Kit Introduction

This evaluation board allows the user to implement the functionality of the SMARTMOS MC33660 ISO9141 transceiver in various configurations to quickly evaluate the device's feature set.

The evaluation board comes with an on-board 5.0 V source via a zener diode with a resistor in series, to optionally provide Chip Enable (CEN) and/or VDD input voltage by a simple jumper and three-position switch configuration. Transitioning from Normal to Sleep mode and vice versa is made simple with a three-position switch. The status of VBB, VDD, and CEN can be visually monitored via on-board LEDs. The ISO Bus signal is provided through a terminal block connector with simple slave or master configuration via jumper settings.

An isolated terminal block connector is implemented for the user to provide power to the board with an external DC power supply. TX and RX signals are routed on a separate terminal block connector and the user has the option to connect an external DC power supply for CEN and VDD for greater system flexibility.

3.1 Evaluation Board Features

- Nominal operating supply voltage range of 8.0 to 18 V
- Individually routed power supply inputs for VBB, VDD, and CEN, to separate transceiver and external regulator current consumptions
- On-board 5.0 V source to optionally provide Chip Enable (CEN) and/or VDD input voltage by a simple jumper and three-position switch configuration
- CEN mode transition functionality is accessible through a three-position switch or external voltage input
- VBB, VDD, and CEN status is indicated by an LED
- Slave or master configuration via jumper setting
- Test point for every pin

3.2 Device Description/Features

- Operates over wide supply voltage of 8.0 to 18 V
- Operating temperature of -40 to 125 °C
- ISO K line pin protected against shorts to battery
- Thermal shutdown with hysteresis
- ISO K line pin capable of high currents
- ISO K line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components
- Sleep mode: No V_{BAT} current drain with V_{DD} at 5.0 V
- Low current drain during operation with V_{DD} at 5.0 V

4 Required Equipment

To use this kit you will need:

- Power supply: minimum 8.0 V and 100 mA current
- +5.0 VDC power supply (optional)
- Any piece of equipment/board that is capable of producing TX and/or ISO9141 messages

5 KIT33660EFEVBE Setup Configuration

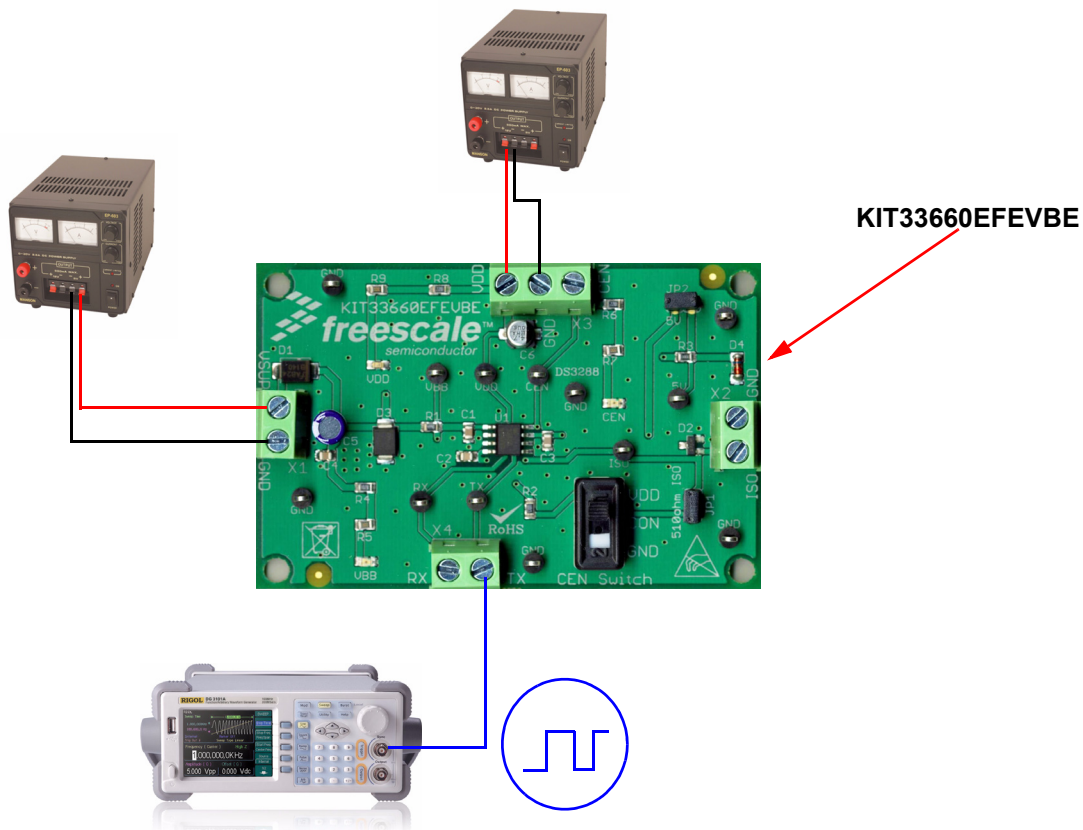


Figure 2. KIT33660EFEVBE Setup Configuration Diagram

6 Hardware Configuration

KIT33660EFEVBE operates with a single 8.0 V minimum power supply, and a simple jumper and switch configuration, to enable device states and make use of an on-board 5.0 V source.

6.1 Board Implementation

For Standard EVB configuration, set up the jumpers and switch as shown in [Figure 3](#). If the jumper and switch configuration is in accordance with [Section 6.2](#), the VBB, VDD, and CEN LEDs must be ON at startup. If ISO communication will be exercised, the user has the option to configure the EVB as a master via the 510 ohm ISO (JP1) jumper.

There are several device features that can be evaluated via simple jumper and switch configurations. Some examples are: Normal to Sleep mode transitions and vice versa, VDD status via LED, and ISO communication.

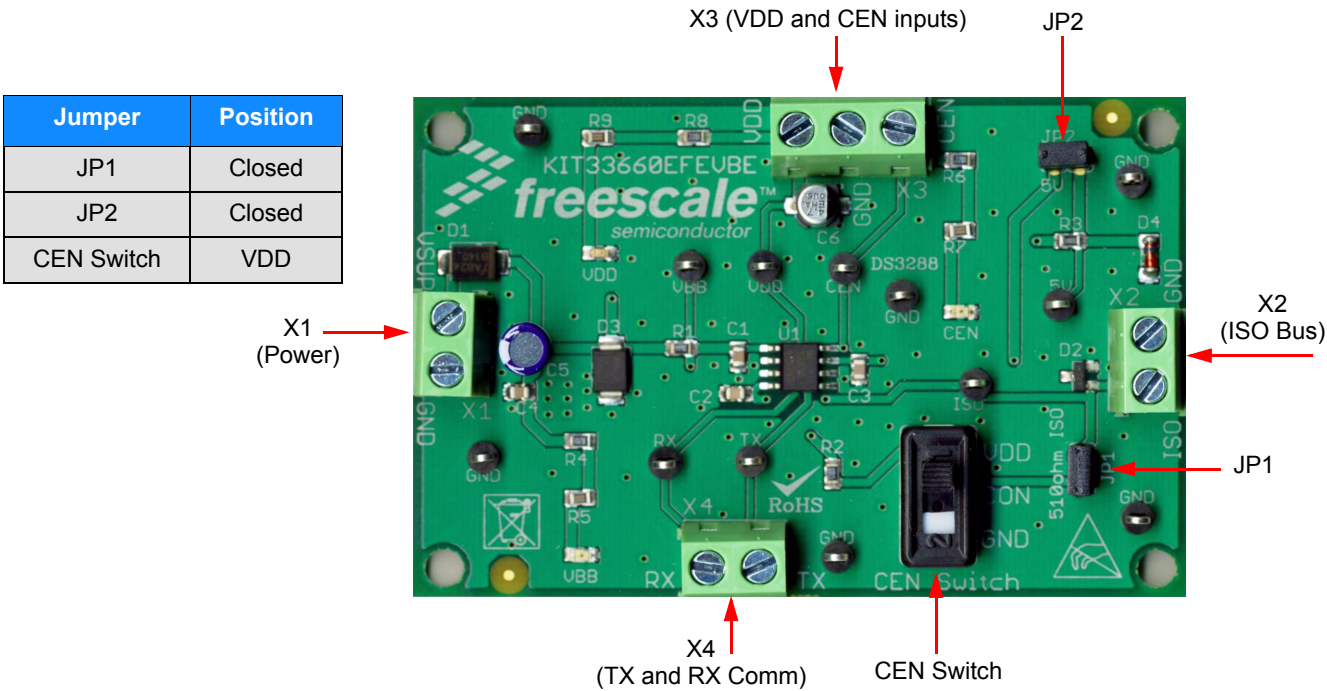


Figure 3. Jumper and Switch Settings

6.2 Jumper, Resistor, and Switch Connections

Name	Description
JP1	510 ohm ISO (pull-up resistor to VBB) Jumper closed -> Master Configuration
JP2	5.0 V source (via zener diode and resistor connected to VBB) Jumper closed -> 5.0 V source connected to VDD
CEN Switch	CEN input VDD position -> CEN is connected to VDD CON position -> CEN is connected to X3 block connector terminal CEN GND position -> CEN is connected to GND
R5	LED for VBB state
R7	LED for CEN state
R9	LED for VDD state

6.3 Power Supply and Input/Output Connectors

The two-pin terminal block (X1) serves as the main power terminal to supply a minimum of 8.0 V to operate the KIT33660EFEVBE. VDD and CEN can be accessed externally through the three-terminal block (X3), or they can be supplied by the on-board 5.0 V source.

The ISO bus signal is accessible through the two-pin terminal block (X2), and communication to and from optional microcontroller to transceiver can be accessed through the two-terminal block (X4) for TX and RX.

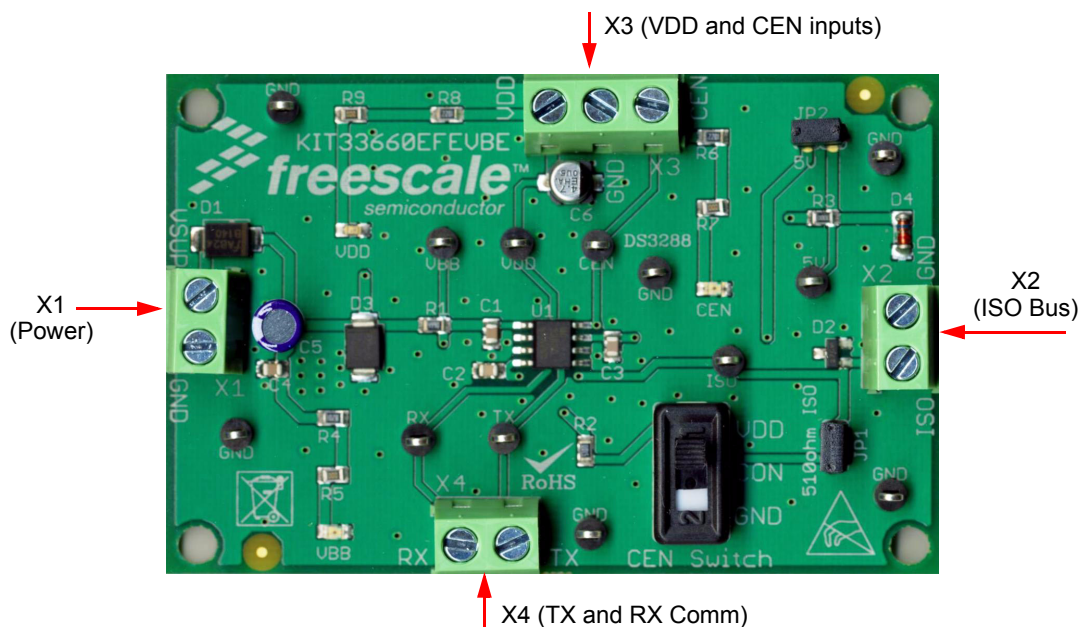


Figure 4. Power Supply and Input/Output Control Connectors

9 Board Layout

9.1 Assembly Top Layer

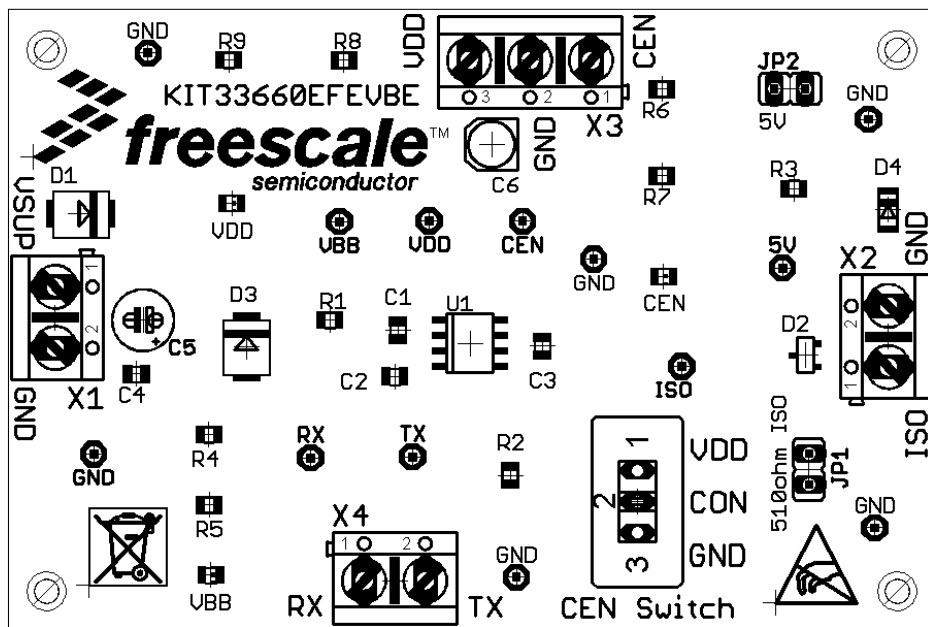


Figure 6. Assembly Top Layer

9.2 Top Layer Routing

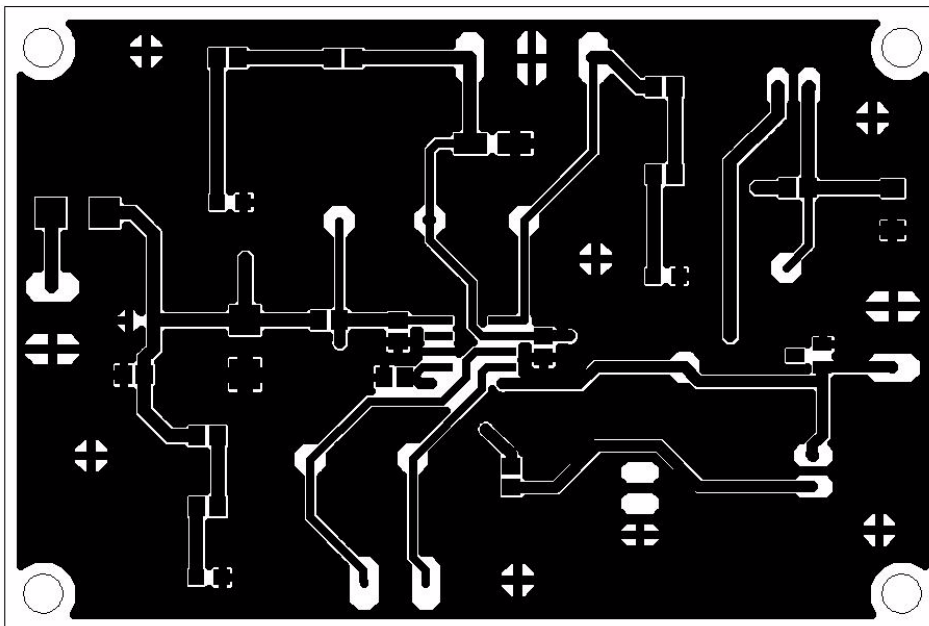


Figure 7. Top Layer Routing

9.3 Bottom Layer Routing

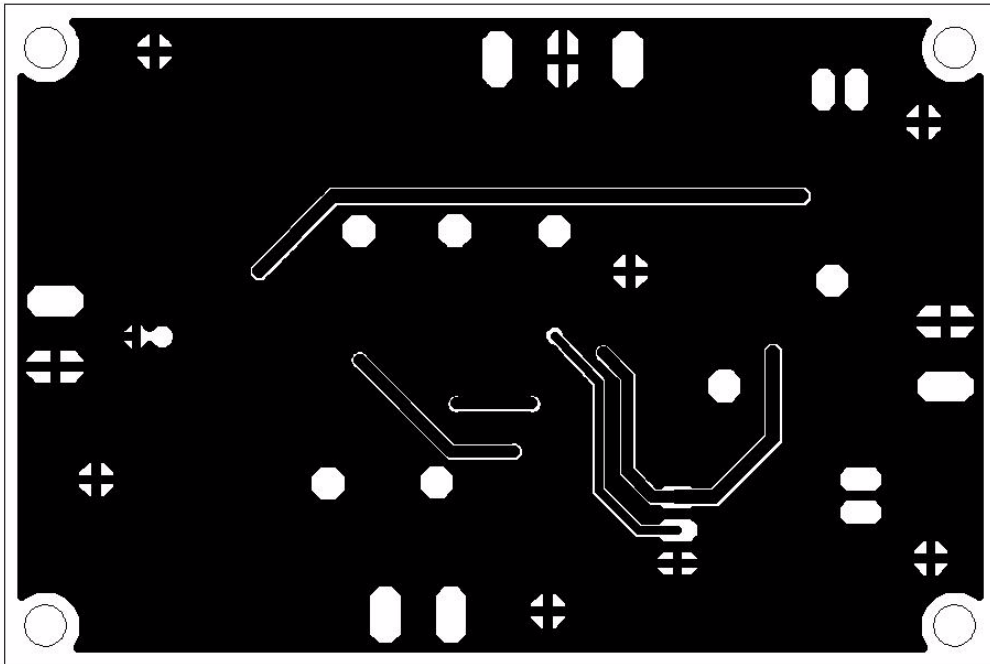


Figure 8. Bottom Layer Routing

10 KIT33660EFEVBE Bill of Material

 Table 1. KIT33660EFEVBE Bill of Materials ⁽¹⁾

QTY	PART REFERENCE	DEVICE or VALUE	PART DESCRIPTION
FREESCALE COMPONENT			
1	U1	MC33660EF	ISO9141 Transceiver
CAPACITOR			
1	C1	0.01 μ F / 50 V	SMT 0805
1	C2	4700 pf / 50 V	SMT 0805
1	C3	1000 pf / 50 V	SMT 0805
1	C4	100 nF / 50 V	SMT 0805
1	C5	10 μ F 100 V electrolytic	ECA-2AM100 Panasonic
1	C6	4.7 μ F 25 V electrolytic	EEE-HA1E4R7AR Panasonic
RESISTOR			
1	R1	499 ohm	0805 1%
1	R2	510 ohm	0805 1%
1	R3	330 ohm	0805 1%
1	R4	8.2 k	0805 1%
3	R5, R7, R9	0	0805
2	R6, R8	2.2 k	0805 1%
DIODE			
1	D1	MBRS140	1.0 amp rectifier
1	D2	MMBZ27VCLT1G	275 V 225 mW TVS
1	D3	1SMB5940BT3G	43 V 3.0 W Zener
1	D4	FLZ5V1A	Zener
1	CEN	Green LED	805
1	VDD	Orange LED	805
1	VBB	Red LED	805
CONNECTOR			
3	X1, X2, X4	2 pos Terminal Block	AK500/2 or comparable
1	X3	3 pos Terminal Block	AK500/3 or comparable
1	CEN Switch	25139NLDH	Apem Slide switch

Note:

1.Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

11 References

Following are locations where you can obtain information on other Freescale products and application solutions.

Description	URL
Reference Web Sites	Reference URL Locations
MC33660 Data Sheet	http://www.freescale.com/files/analog/doc/data_sheet/MC33660.pdf
Application Notes	http://www.freescale.com/files/analog/doc/app_note/AN2409.pdf
Freescale's Web Site	http://www.freescale.com
Freescale's Analog and Power Management Web site	http://www.freescale.com/analog
Freescale's Automotive Applications Web site	http://www.freescale.com/automotive

12 Revision History

Revision	Date	Description of Changes
2.0	8/2014	<ul style="list-style-type: none"> • Updated kit contents/packing list • Added revision history page • Updated back page

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