USB Compliance Checklist

Peripheral Silicon
(excluding hubs)

July 19, 1999

USB Device Product Information

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Vendor Name	Motorola
Vendor Street Address	
Vendor City, State, Zip	
Vendor Phone Number	
Vendor Contact, Title	
Product Name	
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Introduction

This is a checklist to help in design reviews of ASICs and Components for Peripherals to check their compliance with Universal Serial Bus Specification, Revision 1.0.

This checklist is also used to qualify a USB product for the System Integrator List by creating a paper trail of testing for USB compliance.

USB Protocol Checklist

The reference setup for this checklist is a USB link with one USB on each side of it. This checklist specifies behavior expected from these USB agents to satisfy chapter 8 of the USB protocol. One of these two agents is the controlling agent (host or hub) and the other is the controlled agent (device or hub). Except for a few noted items, both types of agents need to adhere to the same requirements. The hub is a special entity because its upstream ports act like a device and its downstream ports act like a host, and it is covered in a separate checklist. For the purposes of this checklist, the terms host and hub downstream port are equivalent as are the terms device and hub upstream/root port. Hub specific requirements are listed in the hub chapter.

This checklist is organized in two broad sections. The first section lists expected or normal behavior from an USB agent when it drives the bus or receives from the bus . So tests in this section need to be done in two parts - ensure that the agent drives the correct signals and ensure that the agent accepts correct signaling (correctness by design and correctness by test). The second section lists expected behavior of an USB agent when it sees an error or abnormal condition on the bus (test of design robustness). Any deviation from this checklist should be noted and explained in the explanations area. These lists are organized starting with the smallest signal entity on the bus and ending at the transfer level.

Some definitions of terms used in the checklist. Note that some terms are overloaded (e.g. data) and definition should be derived from context. Bit order is from left to right unless specified otherwise.

Sense: The relationship between D+ and D- voltages for J state on a USB link e.g. on a fullspeed link, D+ > D- ; on a low-speed link D+ < D-.
NZB: NrZ bit; smallest data structure referenced in spec; represented as 1, 0 and S (single-ended 0) e.g. 1
NIB: NrzI bit; smallest data structure referenced in spec; represented as J, K and 0 (single-ended 0) e.g. J
Field: the next higher form of data structure; can be represented as NIBs or NZBs e.g. sync field is KJKJKJKK or 00000001
Packet: is the most referenced data structure; is built out of fields e.g. Token packet
Phase: of a transaction is made up of 0 or 1 packet e.g. token phase

Transaction: is the basic unit for unidirectional data transfer and is a set of packets; for unidirectional endpoints (bulk, interrupt, iso) this is the final level of communication with protocol implications e.g. OUT transaction
Stage: is a set of one or more unidirectional transactions e.g. data stage
Transfer: is a unit of bi-directional data transfer and is built out of stages. It is used by bi-directional endpoints only. e.g. control transfer
Turnaround time: time between an agent seeing the EOP for the previous packet and starting to drive the bus for a new packet i.e. J period after 0 of the EOP. This time also applies to the period between packets when the host is driving both packets.
Time-out period: amount of time that an agent awaiting a response waits before invalidating the transaction
Target: could be a pipe in the host or endpoint in a device

The addendum lists test scenarios which can be used to develop tests for the items in the checklist as well as some useful Perl programs.

Design-and-Test section:

Bitstream

A bitstream is a set of bits from J,K, 0 (nrzi) or 0,1,S(nrz)

Name	Test description	Spec sec	Status
BSD 1	Is >=2.5 us of NIB 0 anywhere in a bitstream recognized on the root port of a device as a USB RESET?	7.1.4.3	yes ✓ no___
BSD 2	Is >=2.5 us of NIB 0 anywhere in a bitstream recognized by the host or the downstream port of a hub as a disconnect event?	7.1.4.1	yes ✓ no___
BSD 3	Is >=2.5 us of NIB J recognized by the host or a downstream port of a hub as a connect event?	7.1.4.1	yes ✓ no___
BSD 4	Is >=20 ms of NIB K followed by an EOP recognized as an end of resume event by a target?	11.5.1	yes ✓ no___
BSD 5	Does any transition from the J state on the root port of a suspended device wakeup the device?	7.1.4.5	yes ✓ no___
BSD 6	Is the possibility of a NIB 1 <1 bit time during bus transitions accounted for?	7.1.13	yes ✓ no___
BSD 7	Is the sense of signaling on a link either full-speed or low-speed but not both?	11.2.5	yes ✓ no___
BSD 8	Does the sense of signaling on a link correspond to speed of link?	7.1.4	yes ✓ no___
BSD 9	Is the bitstream on the bus nrzi encoded?	7.1.5	yes ✓ no___
BSD 10	Does the bitstream on the bus implement bit stuffing prior to transmission?	7.1.6	yes ✓ no___
BSD 11	Does the CRC bitstream on the bus implement bit stuffing?	8.3.5	yes ✓ no___
BSD 12	Is bit stuffing implemented even if a stuffed bit is required after the last bit of the packet?	8.3.5	yes ✓ no___
BSD 13	Is bit stuffing done after the CRC computation on the transmitted bit stream?	8.3.5	yes ✓ no___
BSD 14	Is nrzi encoding done after the bit stuffing on the transmitted bit stream?	7.1.6	yes ✓ no___
BSD 15	Is nrzi->nrz decoding done before bit unstuffing?	7.1.6	yes ✓ no___
BSD 16	Is bit unstuffing done before the bitstream is parsed?	7.1.6	yes ✓ no___

Field

A field can be

sync	- 8 bit field with NZB value 00000001
PID	- listed in Table 8-1 of spec
address	- 7 bit field
endpoint	- 4 bit field
frame number	- 11 bit field
token CRC	- 5 bit field
data	- 0 to 1023 byte field
data CRC	- 16 bit field
EOP	- 3 bit field with NIB value 00J

Name	Test description	Spec sec	Status
FLD 1	Is the sync field as measured on the bus wires correct i.e. NIB KJKJKJKK?	8.2	yes ✓ no___
FLD 2	Is the packet type in the PID one of those listed in Table 8-1	8.3.1	yes ✓ no___
FLD 3	Is the PID check the one's complement of the packet type field	8.3.1	yes ✓ no___
FLD 4	Is the token CRC generated with the polynomial NZB 00101 on address-endpoint/frame number fields	8.3.5.1	yes ✓ no___
FLD 5	Does the CRC computation on a token/SOF bitstream leave a residual of NZB 01100 at the EOP	8.3.5.1	yes ✓ no___
FLD 6	Is the data CRC generated with the polynomial NZB1000000000000101 on the data field	8.3.5.2	yes ✓ no___

FLD 7	Does the CRC computation on a data packet bitstream leave a residual of NZB 1000000000001101 at the EOP	8.3.5.2	yes ✓ no___
FLD 8	Is the 7-bit address field sent out LSB first on the bus	8.3.2.1	yes ✓ no___
FLD 9	Is the 4-bit endpoint field sent out LSB first on the bus	8.3.2.2	yes ✓ no___
FLD 10	Is the 11-bit frame number field sent out LSB first on the bus	8.3.3	yes ✓ no___
FLD 11	Is each data byte in the data field sent out LSB first	8.3.4	yes ✓ no___
FLD 12	Is the CRC shift register contents inverted to form the CRC field	8.3.5	yes ✓ no___
FLD 13	Is the CRC field sent out MSB first	8.3.5	yes ✓ no___
FLD 14	Is the EOP correctly constituted i.e. NIB 00J	7.1.11.2	yes ✓ no___
FLD 15	Does a full-speed receiver (on a non-hub device) recognize 82ns to 2.5 us of NIB 0 followed by a J transition as a valid EOP	7.1.12	yes ✓ no___
FLD 16	Does a low-speed receiver (on a non-hub device) recognize 670 ns to 2.5 us of NIB 0 followed by a J transition as a valid EOP	7.1.12	yes ✓ no___
FLD 17	Does a low speed device recognize low-speed keepalive strobes	11.2.5.1	yes ✓ no___
FLD 18	Does a low speed device support one control endpoint and at most two other endpoint numbers	8.3.2.2	yes ✓ no___
FLD19	Are the endpoints on a low speed device either control or interrupt type	8.3.2.2	yes ✓ no___

Packet

A packet is made up of fields which are formatted as described in sec. 8.4 of spec and can be one of the following:

PRE - sync PID
SOF - sync PID timestamp token CRC EOP
Token - sync PID endpt token CRC EOP
data - sync PID data..... data dataCRC EOP
handshake - sync PID EOP

Name	**Test description**	Spec sec	Status
PKD 1	Is the PRE packet 16 bits long	8.6.5	yes ✓ no___
PKD 2	Is the PRE packet constituted as sync followed by PID	8.6.5	yes ✓ no___
PKD 3	Is the Token packet 32 bits + EOP	8.4.1	yes ✓ no___
PKD 4	Is the token constituted as sync followed by PID followed by address followed by endpoint followed by token CRC followed by EOP	8.4.1	yes ✓ no___
PKD 5	Is the SOF packet 32 bits + EOP	8.4.2	yes ✓ no___
PKD 6	Is the SOF constituted as sync followed by PID followed by frame number followed by token CRC followed by EOP	8.4.2	yes ✓ no___
PKD 7	Is the handshake packet 16 bits + EOP	8.4.4	yes ✓ no___
PKD 8	Is the handshake constituted as sync followed by PID followed by EOP	8.4.4	yes ✓ no___
PKD 9	Is the data packet an integral number of bytes (4 to 1027) + EOP	8.4.3	yes ✓ no___
PKD 10	Is the data packet constituted as sync followed by PID followed by 0 to 1023 bytes of data followed by data CRC followed by EOP	8.4.3	yes ✓ no___
PKD 11	Is the data payload of a low speed packet limited to 8 bytes	8.6.5	yes ✓ no___

Transaction

Transactions are sets of packets used for unidirectional data transfer and can be one of the following: (host phase in italics; device phase in regular font)

SOF
setup data ack
out data ack/nak/stall
out data0
in data *ack*
in data0/nak/stall
pre setup pre data ack
pre out pre data ack/nak/stall
pre in data *pre ack*
pre in nak/stall

Name	Test description	Spec sec	Status
TRD 1	Does the device implement default address of 0 on device reset	8.3.2.1	yes ✓ no___
TRD 2	Does the device implement a bi-directional control endpoint 0 for every address	8.3.2.2	yes ✓ no___
TRD 3	Does the generated packet fit the phase of the transaction as listed above	8.5,8.6.5	yes ✓ no___
TRD 4	Is the turnaround time of a packet-sourcing agent greater than 2 bit times	7.1.15	yes ✓ no___
TRD 5	Is the turnaround time of a packet-sourcing agent less than 6.5 (7.5 with integrated cable) bit times	7.1.15	yes ✓ no___
TRD 6	Is the time-out period at an agent awaiting response greater than 16 bit times	7.1.16	yes ✓ no___
TRD 7	Is the time-out period at an agent awaiting response less than 18 bit times	7.1.16	yes ✓ no___
TRD 8	Is an unsuccessful (NAK or time-out in non-token phase) transaction retried	8.6.2-4	yes ✓ no___
TRD 9	Does the retried transaction use the same data PID as the original transaction	8.6.2-4	yes ✓ no___
TRD 10	Do interrupt endpoints used in rate feedback mode toggle the sequence bit without regard to presence or type of handshake	8.5.3	yes ✓ no___ see note 0
TRD 11	Do handshakes conform to order of precedence detailed in tables of Sec. 8.4.5	8.4.5	yes ✓ no___ see note 1
TRD 12	Are low speed transactions limited to those needed to support interrupt and control endpoints	8.6.5	yes ✓ no___
TRD 13	Does an ISO endpoint synthesize frame markers to replace SOFs which may be lost due to bus error	5.10.6	yes ✓ no___ see note 0
TRD 14	Does an ISO pipe handle holes/bubbles in pipe which may arise during suspend-resume operation		yes ✓ no___

Transfer

Transfers are data structures used by bi-directional (control endpoints). The transfer is made up of stages which are sets of unidirectional transactions. They can be one of:

setup0 *out1* *out0* *out1* ... *out0/1* in1
setup0 *in1* *in0* *in1* ... *in0/1* out1
setup0 in1

Transactions in italics constitute the data stage ; there may or may not be a data stage between the setup stage and status stage. Suffix of 0 or 1 indicates the data PID used in the transaction

Name	Test description	Spec sec	Status
TFD 1	Does the setup stage use a data0 PID	8.5.2	yes ✓ no___
TFD 2	Does the status stage use a data1 PID	8.5.2	yes ✓ no___
TFD 3	Does the data stage always start with a data1 PID	8.5.2	yes ✓ no___
TFD 4	Are all the transactions of the data stage in the same direction	8.5.2	yes ✓ no___
TFD 5	Is there a change of direction when entering the status change	8.5.2	yes ✓ no___
TFD 6	Is the data packet used in the status stage 0 bytes in length	8.5.2	yes ✓ no___

Test for robustness Section:

Bitstream

A compliant bitstream is a set of bits from J,K,0 (nrzi) or 0,1,X(nrz)

Name	Test description	Status
BST 1	Is a single ended NIB 1 of >= 1 bit time ignored by the target	yes ✓ no___
BST 2	Does an agent ignore a truncated (up to 50%) first bit of the sync field without impacting the rest of the bitstream	yes ✓ no___
BST 3	Is the state of the differential receiver ignored during single ended signal state	yes ✓ no___
BST 4	Does the target reject bitstreams of length <1 bit time without impacting future transactions	yes ✓ no___
BST 5	Does the target adjust to the difference in frequency and phase between incoming clock and its internal clock	yes ✓ no___
BST 6	Is a packet with a bit-stuff error rejected by the target	yes ✓ no___
BST 7	Is a bitstream (which is not part of a packet) with bit stuff error ignored by the target	yes ✓ no___
BST 8	Does the target reject packets with bit stuff error at the last bit of the packet	yes ✓ no___
BST 9	Is bit stuffing implemented even if stuffed bit is after the last bit of the packet	yes ✓ no___
BST 10	Can the device handle more than one USB RESET with no intervening packets correctly	yes ✓ no___

Field

A compliant field can be one of:

sync	- 8 bit field with NZB value 00000001
PID	- listed in Table 8-1 of spec
address	- 7 bit field
endpoint	- 4 bit field
frame number	- 11 bit field
token CRC	- 5 bit field
data	- 0 to 1023 byte field
data CRC	- 16 bit field
EOP	- 3 bit field with NIB value 00J

Name	Test description	N/A	Status
FLT 1	Is the sync field recognized as valid even if up to two initial bits of it are corrupted (Actually, only the last 3 bits (JKK) need to be decoded).		yes ✓ no___
FLT 2	Is a packet with packet type not listed in Table 8-1 ignored by the target		yes ✓ no___
FLT 3	Is a packet with corrupt PID (PID check error) ignored by the target		yes ✓ no___
FLT 4	Is a token with bad CRC ignored by the target		yes ✓ no___
FLT 5	Is a CRC error on a data packet recognized by the target		yes ✓ no___
FLT 6	Does a full speed receiver reject a NIB 0 of duration less than 40 ns as part of an EOP		yes ✓ no___
FLT 7	Does a low speed receiver reject a NIB 0 of duration less than 330 ns as part of an EOP		yes ✓ no___

Packet

A compliant packet is made up of fields which are formatted as described in sec. 8.4 of spec and can be one of the following:

PRE - sync PID
SOF - sync PID timestamp tokenCRC EOP
Token - sync PID addr endpt tokenCRC EOP
data - sync PID data..... data data CRC EOP
handshake - sync PID EOP

Name	Test description	N/A	Status
PKT 1	Is a token whose address field doesn't match any address in the device ignored by the device		yes ✓ no___
PKT 2	Is a token whose endpoint field doesn't match any endpoint in the address ignored by the device		yes ✓ no___
PKT 3	Is a token which doesn't match direction of endpoint ignored by the device		yes ✓ no___
PKT 4	Is a SETUP token to a unidirectional endpoint ignored by the device		yes ✓ no___
PKT 5	Is every endpoint capable of handling 0 length data packet in its assigned direction(s)		yes ✓ no___
PKT 6	Does an ISO endpoint use 0 length data packet if fresh frame data is not available		yes __ no ✓ see note 2
PKT 7	Is a packet whose length doesn't match standard length for packet type rejected by target		yes ✓ no___
PKT 8	Does the measurement of packet length take into account the possibility of jitter in the EOP		yes ✓ no___
PKT 9	Is a bitstream not constituted according to packet rules described in last section rejected by the target		yes ✓ no___

Transaction

A compliant transaction can be one of the following: (host phase in italics; device phase in regular)
SOF
setup data ack
out data ack/nak/stall
out data0
in data *ack*
in data0/nak/stall
pre setup pre data ack
pre out pre data ack/nak/stall
pre in data *pre ack*
pre in nak/stall

Name	Test description	N/A	Status
TRT 1	Is a packet which doesn't fit the current phase of a transaction rejected by the target		yes ✓ no___
TRT 2	Does the receipt of a token always start a new transaction (and end a pending transaction)		yes ✓ no___
TRT 3	Does a target ignore data packet with same PID as previous data packet to the endpoint but successfully complete (ack) the transaction		yes ✓ no___ see note 3
TRT 4	Does a time-out or error in any phase cause the transaction to be terminated		yes ✓ no___
TRT 5	Is a transaction always started with a token		yes ✓ no___
TRT 6	Is the data toggle implemented independently for each unidirectional endpoint		yes ✓ no___
TRT 7	Does the source of ISO data ignore handshake without impacting subsequent transactions		yes ✓ no___
TRT 8	Can the target handle consecutive packets in the same direction with >=2 bit times of interpacket gap		yes ✓ no___

Transfer

Transfers are data structures used by bi-directional (control endpoints). The transfer is made up of stages which are sets of unidirectional transactions. A compliant transfer can be one of:

setup0 *out1 out0 out1 ... out0/1* in1
setup0 *in1 in0 in1 ... in0/1* out1
setup0 in1

Transactions in italics constitute the data stage ; there may or may not be a data stage between the setup stage and status stage. Suffix of 0 or 1 indicates the data PID used in the transaction

Name	Test description	N/A	Status
TFT 1	Does a target receiving an unexpected data PID ignore the data but still successfully complete(ack) the transaction		yes ✓ no___
TFT 2	Does the receipt of a non-zero length data packet in the status stage cause the transfer to be terminated with an error indication		yes ✓ no___ see note 0

USB Signals and Timing Checklist

General Rules:

Name	Test description	NA	Status
EL1	Single-ended receivers recognize voltage below 0.8 V as a logic low?		yes__ no__
EL2	Single-ended receivers recognize voltage above 2.0 V as a logic high?		yes__ no__
EL3	Differential receivers recognize differential voltages of 200 mV between 0.8 and 2.5 volts?		yes__ no__
EL4	Do active data line outputs drive to 2.8 volts with a 15 KΩ load to ground?		yes__ no__
EL5	Do active data line outputs drive to 0.3 volts with a 1.5 KΩ load to 3.6 volts?		yes__ no__
EL6	Capacitance on each data line is a maximum of 20 pF (without cable)?		yes__ no__
EL7	Does the device accept a truncated bit time (down to half of a bit time) as the first bit of the SYNC field?		yes__ no__
EL8	Does the device recognize a single-ended zero of 2.5 µs or greater on its root port as a device reset?		yes__ no__
EL9	Does the device recognize any non-idle state on its root port as a resume signal?		yes__ no__
EL10	Do all downstream ports sink 200 µA ±5% at 3.0V when not driving the bus (15 KΩ resistor to ground present)?		yes__ no__ n/a__
EL11	Are open downstream ports pulled to ground?		yes__ no__ n/a__
EL12	Does the device recognize a single-ended zero of 2.5 µs or greater on any of its downstream ports as a disconnect?		yes__ no__ n/a__
EL13	Does the device recognize a non single-ended zero of 2.5 µs or greater on any of its downstream ports as a connect?		yes__ no__ n/a__
EL14	Is the pullup at the root port connected to a supply which is controlled logically as an AND of Vbus and device VCC?		yes__ no__ n/a__

Driver Port Characteristics - Full Speed Ports: This section is N/A __✓__.

Applicable to any port which can operate at 12 Mb/s, up or downstream.
This includes the host, full speed devices and all hub ports, including the root port.

EL15	Is the differential source resistance between 28Ω and 43 Ω?	yes__ no__
EL16	Is the pull-down source resistance between 28Ω and 43 Ω?	yes__ no__
EL17	Are data line rise times are greater than 4.0 ns and less than 20 ns?	yes__ no__
EL18	Are data line fall times are greater than 4.0 ns and less than 20 ns?	yes__ no__
EL19	Are the rise and fall times matched to within 10%?	yes__ no__
EL20	Do the data lines cross over each other between 1.3 and 2.0 volts?	yes__ no__
EL21	Is the bus idle state D+ between 3.0 and 3.6V and D- at ground?	yes__ no__
EL22	Is there a pull-up resistor on the D+ data line of the device's root port?	yes__ no__
EL 23	Does the combination of the device's pullup resistor and the 15KΩ pulldown resistor upstream yield a voltage which is at least 2.0V when the bus is idle?	yes__ no__
EL 24	Does the combination of the device's pullup resistor and the 15KΩ pulldown resistor upstream yield a voltage which does not exceed 3.6V when the bus is idle?	yes__ no__
EL25	When Vbus is disconnected from the device, does the D+ source no current?	yes__ no__
EL26	When Vbus is present on the device, is the magnitude of the leakage current (device not driving) from the D- data line less than 10 µA for input voltages between 0.0 and 3.3 volts?	yes__ no__

Driver Port Characteristics - Low Speed Ports: This section is N/A __✓__.

Applicable to any port which can operate at 1.5 Mb/s, up or downstream.
This includes the host, low speed devices and all downstream hub ports.

EL 27	Data line rise times are greater than 75 ns and less than 300 ns?	yes__ no__
EL 28	Data line fall times are greater than 75 ns and less than 300 ns?	yes__ no__
EL 29	Are the rise and fall times matched to within 20%?	yes__ no__
EL 30	Do the data lines cross over each other between 1.3 and 2.0 volts?	yes__ no__
EL 31	At bus idle is D- between 3.0 and 3.6V, and is D+ at ground?	yes__ no__
EL 32	Does the combination of the device's pullup resistor and the 15KΩ pulldown resistor upstream yield a voltage which is at least 2.0V when the bus is idle?	yes__ no__
EL 33	Does the combination of the device's pullup resistor and the 15KΩ pulldown resistor upstream yield a voltage which does not exceed 3.6V when the bus is idle?	yes__ no__
EL 34	When Vbus is disconnected from the device, does the D- source no current?	yes__ no__
EL 35	When Vbus is present on the device, is the magnitude of the leakage current (device not driving) from the D+ data line less than 10 µA for input voltages between 0.0 and 3.3 volts?	yes__ no__

Data Source Timings - Full Speed Ports: This section is N/A ✓ .

Applicable to a device operating at 12 Mb/s, up or downstream which acts as the source of data. This includes the host, full speed devices and the root hub port when the hub or embedded function is the addressed device.

EL 36	Is the transmission data rate between 11.97 and 12.03 Mb/s?	yes__ no__
EL 37	Does the high speed device operate correctly with frame lengths between 0.9995ms and 1.0005 ms?	yes__ no__
EL 38	Is the differential driver jitter less than ±3.5 ns?	yes__ no__
EL 39	Is the differential driver jitter for paired transitions[3] less than ±4.0 ns?	yes__ no__
EL 40	Is the EOP width between 160 ns and 175 ns at the transmitter?	yes__ no__
EL 41	Is the timing skew due to the transition to the EOP on the last differential bit(s) between -2.0 ns and 5.0 ns at the transmitter?	yes__ no__
EL 42	Is the receiver data jitter tolerance at least ± 18.5 ns?	yes__ no__
EL 43	Is the receiver jitter tolerance for paired transitions[3] at least ± 9.0 ns?	yes__ no__
EL 44	Does the device accept a single-ended zero of 1 FS bit time as an EOP?	yes__ no__
EL 45	Does the device reject as an EOP a single-ended zero of 40 ns or less?	yes__ no__

Data Source Timings - Low Speed Ports: This section is N/A ✓ .

Applicable to a device operating at 1.5 Mb/s, up or downstream. This includes the host and low speed devices.

EL 46	Is the transmission data rate between 1.4775 and 1.5225 Mb/s?	yes__ no__
EL 47	Is the differential driver jitter less than ±95 ns? (n/a for host devices)	yes__ no__ n/a__
EL 48	Is the differential driver jitter for paired transitions[3] less than ±150 ns? (n/a for host devices)	yes__ no__ n/a__
EL 49	Is the EOP width between 1.25 µs and 1.5 µs at the transmitter?	yes__ no__
EL 50	Is the timing skew due to the transition to the EOP on the last differential bit(s) between -40 ns and 100 ns at the transmitter?	yes__ no__
EL 51	Is the receiver data jitter tolerance at least ± 75 ns? (n/a for host devices)	yes__ no__ n/a__
EL 52	Is the receiver jitter tolerance for paired transitions[3] at least ± 45 ns? (n/a for host devices)	yes__ no__ n/a__
EL 53	Does the device accept a single-ended zero of 1 LS bit time as an EOP?	yes__ no__
EL 54	Does the device reject as an EOP a single-ended zero of 330 ns or less?	yes__ no__

Suspend And Resume

SU 1	Does a USB peripheral enter the suspend state after 3.0 ms of continuous J on its bus	yes_✓ no__ see note 4
SU 2	If a peripheral is bus powered does its average suspend current remain below 500 µa	yes__ no__ na_✓__
SU 3	If a peripheral is bus powered does its peak suspend current remain below 100 ma	yes__ no__ na_✓_
SU 4	If a peripheral is low powered does it recognize LS keep alive signaling and remain awake?	yes_✓ no__ na__
SU 5	Does a peripheral start its wake-up if the bus state changes from the J->K or J->SE0 states	yes_✓ no__
SU 6	Is a peripheral fully awake within 10 ms of having received a resume event from upstream?	yes_✓ no__
SU 7	Does a peripheral recognize a K->EOP->J transition as end of resume signaling?	yes_✓ no__

All USB devices must be capable of going into resume upon seeing a continuous idle on the bus for 3.0 ms or more. Similarly, all USB devices must be capable of receiving resume and waking up. USB peripherals may implement remote wake-up as an option.

Remote Wake-up

SU 8	Is the peripheral capable of supporting remote wake-up	yes_✓ no__ na__
SU 9	Does the peripheral drive K signaling upstream for at least 10ms, but not more than 15 ms to initiate a remote wake-up event	yes_✓ no__ na__
SU 10	Does a remote wake-up device wait at least 5.0 ms from when the bus entered the idle state before initiating remote resume signaling?	yes_✓ no__ na__

Reset

RST 1	Does a peripheral reject SE0 pulses of less than 2.5 µsec as not being reset?	yes_✓ no__
RST 2	Does a peripheral recognize all SE0 pulses greater than 5.5µs as resets	yes_✓ no__
RST 3	Does a suspended peripheral wake up and recognize reset signaling within 10ms from the start of reset?	yes_✓ no__
RST 4	Does a peripheral respond to a reset by transitioning to the *default* state?	yes_✓ no__ see note 0
RST 5	Does a peripheral draw no more than 100 ma during reset?	yes_✓ no__
RST 6	Does a peripheral draw less than 100 ma from upstream after reset is completed?	yes_✓ no__
RST 7	At the end of reset are the peripheral's D+ and D- floating?	yes_✓ no__

Notes:

1. All of the items in this checklist have been taken from Chapter 7 of the USB Specification, Rev. 1.0, in particular, Section 7.3. These specifications are explained in Section 7.1.
2. All voltages are referenced from the USB ground of the device being tested.
3. See USB Specification Rev. 1.0, Chapter 7, Section 7.1.11.1 for explanation of paired transitions.

Explanations:

note 0
This function is implemented by s/w.

note 1
In the case of OUT token, the USB channel will respond with NACK if the FIFO is full. It is always assumed that a BD is available to the be used by the CPM to store the data when it is read from the FIFO.

note 2
The token will be ignored if a fresh packet is not available.

note 3
The packet will be transferred to the s/w. The s/w should ignore it based on the repeated PID.

note 4
The 3.0 ms timer is handled by the s/w. The h/w generates an indication when to start the timer and when to stop it.

This section should be used to explain any “no” or “n/a” answers or clarify any answers on checklist items above.
Please key explanation to item number.

Explanations:

This section should be used to explain any “no” or “n/a” answers or clarify any answers on checklist items above.
Please key explanation to item number.