MC33FS8415GJKS

Configuration report for FS8415 OTP program ID: GJ rev C

Rev 1.0 — 23 November 2021 **Report**

1 General description

The FS85/FS84 device family is developed in compliance with ASIL D process, FS84 is ASIL B capable and FS85 is ASIL D capable. All device options are pin to pin and software compatible.

The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

Note: All parametric information is maintained in FS84_FS85 datasheet

2 Features and benefits

• 60 V DC maximum input voltage for 12 V and 24 V applications
• VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
• Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
• **Based on device options:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
• **Based on device options:** low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
• BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
• EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
• 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
• Standby OFF mode with very low sleep current (10 µA typ)
• 2x input pins for wake-up detection and battery voltage sensing
• Device control via 32 bits SPI or I2C interface with CRC
• Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
• Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
• Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

3 Applications

- Radar
- Vision
- ADAS domain controller
- Radio
- V2x
- Infotainment

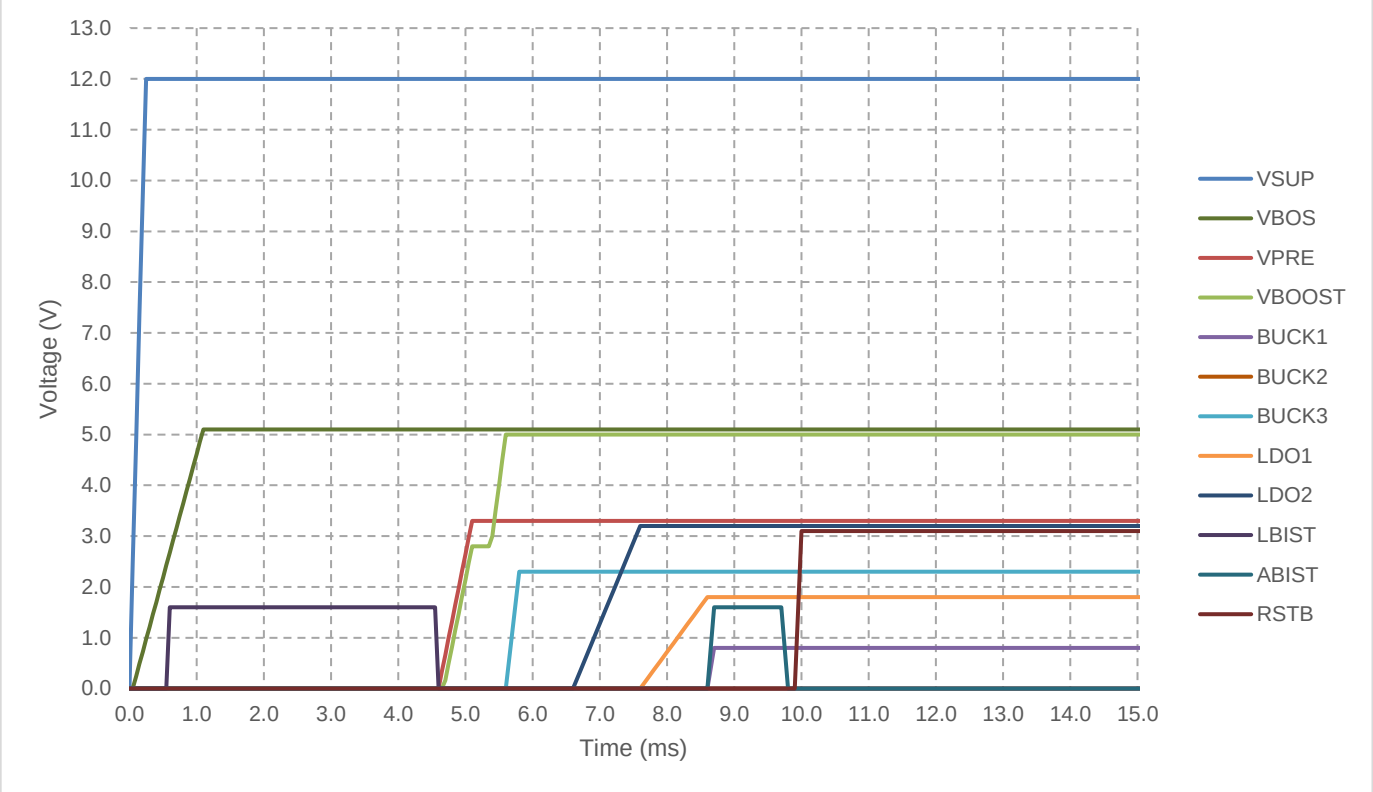
4 Ordering information

Table 1. Ordering Information

Type number[1]	Package		
	Name	Description	Version
MC33FS8415GJKS	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-23

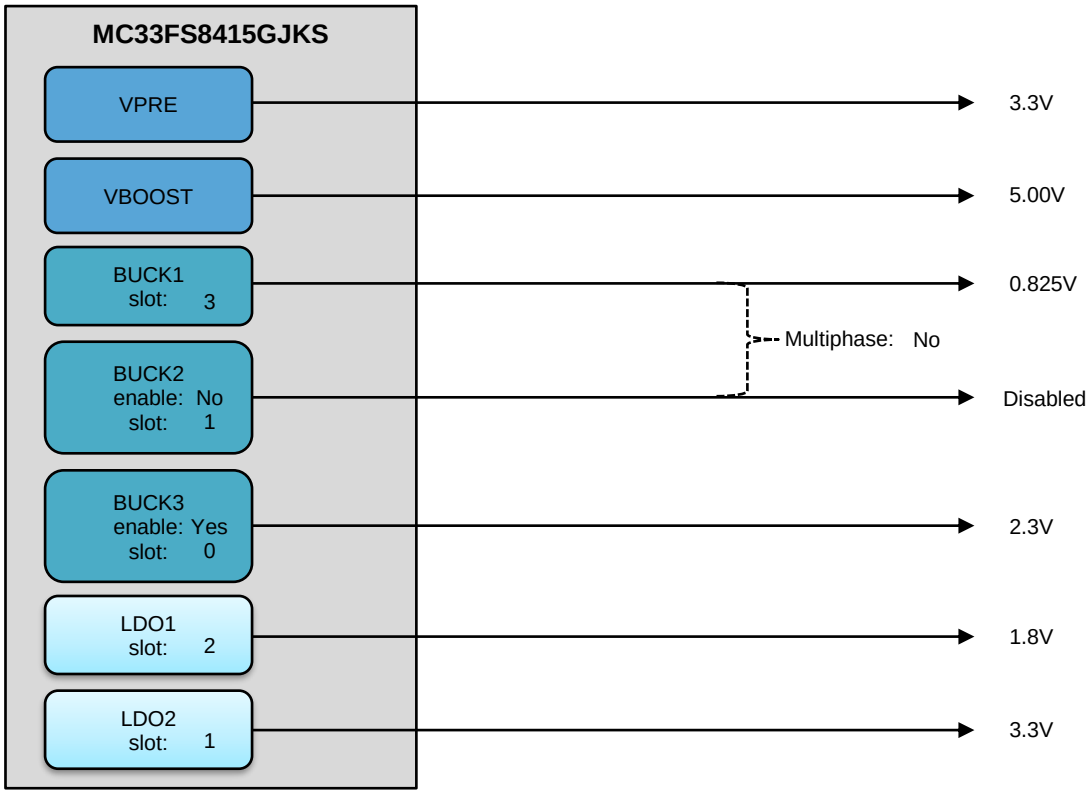
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



Note: VBOS is set at 5.1 V and RSTB at 3.2 V or 4.9 V to differentiate from regulators on the graph

6 Hardware configuration diagram



7 OTP configuration

Table 2. Main OTP configuration

Functional block	Feature	OTP selection
VPRE	Output voltage	3.3V
	Slope compensation	50mV/µs
	Current limitation	80mV
	High Side slew rate	PU/PD/900mA
	Low Side slew rate	PU/PD/900mA
	Switching frequency	455KHz
	Phase shifting	delay 0
	Turn OFF delay	32ms
	VPRE mode	Force PWM

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
VBOOST	Enabled	Yes
	Output voltage	5.00V
	Slope compensation	125mV/µs
	Slew rate	500V/µs
	Compensation resistor	750kohms
	Compensation capacitor	125pF
	Switching frequency	2.22MHz
	Phase shifting	delay 0
	Behavior in case of TSD	BOOST Shutdown
BUCK1	Output voltage	0.825V
	Inductor	1µH
	Current limitation	4.5A
	Compensation network	65 GM
	Switching frequency	2.22MHz
	Phase shifting	delay 6
	Behavior in case of TSD	BUCK1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 3
	Soft start ramp	7.81mV/µs
BUCK2	Enabled	No
	Output voltage	1.8V
	Inductor	1µH
	Current limitation	4.5A
	Compensation network	65 GM
	Switching frequency	2.22MHz
	Multiphase with Buck1	No
	Phase shifting	delay 0
	Behavior in case of TSD	BUCK2 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 1
	Soft start ramp	7.81mV/µs

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
BUCK3	Enabled	Yes
	Output voltage	2.3V
	Inductor	1µH
	Current limitation	4.5A
	Compensation resistor	Default
	Gain control	Default
	Switching frequency	2.22MHz
	Phase shifting	delay 3
	Behavior in case of TSD	BUCK3 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 0
	Soft start ramp	10.4mV/µs
LDO1	Output voltage	1.8V
	Current limitation	400mA
	Behavior in case of TSD	LDO1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 2
LDO2	Output voltage	3.3V
	Current limitation	400mA
	Behavior in case of TSD	LDO2 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 1
Miscellaneous	Power up/down slot duration	1000µs
	PSYNC	Disabled
	PLL enabled	Yes
	Deep Fail Safe (autoretry)	Infinite
	VSUP power-up threshold	4.9V for Vpre < 4.5V
	Regulator assigned to VDDIO	VPRE
	I2C address	0x20
	Device ID	00000001

Table 3. Fail-safe OTP configuration

Functional block	Feature	OTP selection
VCOREMON	Monitoring Voltage	0.825V
	OVTH	104.5%
	UVTH	95.5%
	OV_DGLT	25µs
	UV_DGLT	25µs
	SVS_CLAMP	No SVS

Table 3. Fail-safe OTP configuration (continued)

Functional block	Feature	OTP selection
VDDIOMON	Monitoring Voltage	3.3V
	OVTH	105%
	UVTH	95%
	OV_DGLT	25µs
	UV_DGLT	25µs
VMON1	OVTH	106%
	UVTH	94%
	OV_DGLT	25µs
	UV_DGLT	25µs
VMON2	OVTH	106%
	UVTH	94%
	OV_DGLT	25µs
	UV_DGLT	25µs
VMON3	OVTH	106%
	UVTH	94%
	OV_DGLT	25µs
	UV_DGLT	25µs
VMON4	OVTH	106%
	UVTH	94%
	OV_DGLT	25µs
	UV_DGLT	25µs
PGOOD	VCOREMON	Yes
	VDDIOMON	Yes
	VMON1	Yes
	VMON2	Yes
	VMON3	Yes
	VMON4	Yes
	RSTB	No
ABIST1	VCOREMON	Yes
	VDDIOMON	Yes
	VMON1	Yes
	VMON2	Yes
	VMON3	Yes
	VMON4	Yes

Table 3. Fail-safe OTP configuration (continued)

Functional block	Feature	OTP selection
Safety enable	VMON1	Yes
	VMON2	Yes
	VMON3	Yes
	VMON4	Yes
	FCCU	Yes
	ERRMON	No
	WATCHDOG	Simple WD
	FLT_RECOVERY	Yes
I2C	I2C address	0x21

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Date of release: 23 novembre 2021

Document identifier: R_MC33FS8415GJKS_Rev_C