AH1021

Application Hints - High speed CAN transceiver TJA1049

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Summary

The intention of this application hints document is to provide the necessary information for hardware and software designers for creation of automotive applications using the new high speed CAN transceiver TJA1049. It further on describes the advantages in terms of characteristics and functions offered to a system and how the system design can be simplified by replacing the TJA1040 by the TJA1049 HS-CAN transceivers from NXP.

Revision history

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01.00	20100528	Initial version

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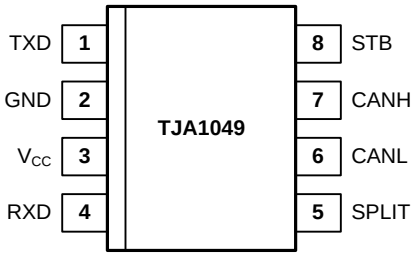
1. Introduction

The TJA1049 provides the physical link between the protocol controller and the physical transmission medium according to the ISO11898 ([13], [14]) and SAE J2284 [15]. This ensures full interoperability with other ISO11898 compliant transceiver products. It is a 100% drop-in replacement to its predecessor TJA1040.

Compared to the TJA1040 the TJA1049 from NXP Semiconductors offer

- a significantly improved ESD robustness,
- a further reduction in electromagnetic emission (EME)
- beside an improved electromagnetic immunity (EMI),
- a higher voltage robustness in order to full support 24V applications
- and a predictable undervoltage behavior at all supply conditions.

TJA1049 – High speed CAN transceiver with Standby Mode *(page 10 ff.)*



- Successor of the TJA1040 high speed CAN transceiver
- Normal Mode (transmit / receive CAN data)
- Standby Mode (low power mode with CAN wake-up capability)
- SPLIT pin for recessive bus level stabilization
- Bus dominant time-out function in Standby Mode
- Undervoltage detection on pin V_{CC}

Fig 1. Pin configuration and short functional description of the TJA1049

2. Basics of high speed CAN applications

2.1 Example of a high speed CAN application

Fig 2 illustrates an example of a high speed CAN application. Several ECUs (Electronic Control Units) are connected via stubs to a linear bus topology. Each bus end is terminated with 120Ω (R_T), resulting in the nominal 60Ω bus load according to ISO11898. The figure shows the split termination concept, which is helpful when improving the EMC of high speed CAN bus systems. The former single 120Ω termination resistor is split into two resistors of half value ($R_T/2$) with the center tap connected to ground via the capacitor C_{spl}.

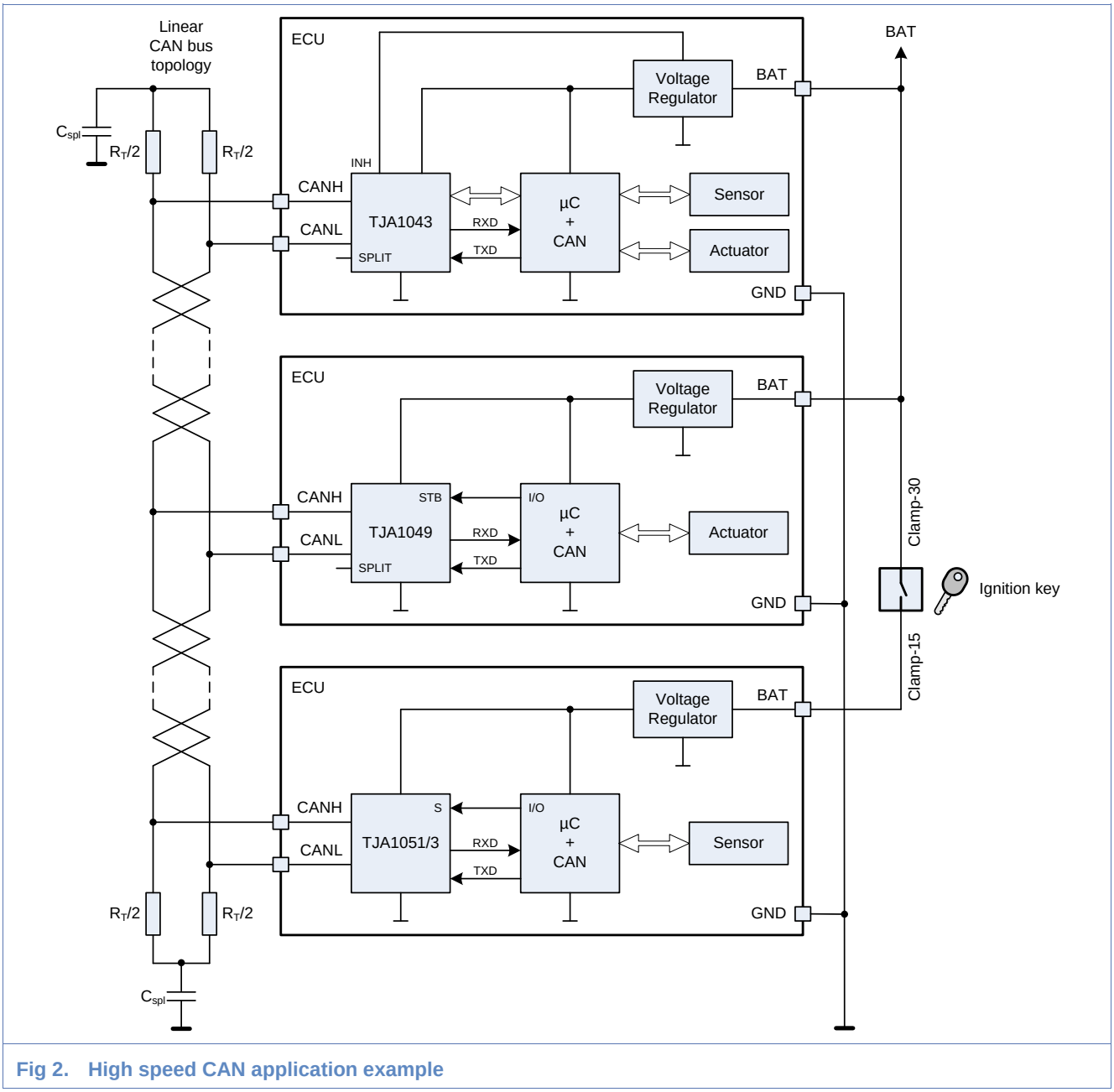


Fig 2. High speed CAN application example

The block diagram in Fig 2 describes the internal structure of an ECU. Typically, an ECU consists of a standalone transceiver (here the TJA1049, TJA1043 and TJA1051/E) and a host microcontroller with integrated CAN-controller, which are supplied by one or more voltage regulators. While the high speed CAN transceiver needs a +5 V supply to support the ISO11898 bus levels, new microcontroller products are increasingly using lower supply voltages like 3,3 V. In this case a dedicated 3,3 V voltage regulator is necessary for the microcontroller. The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability.

Depending on the selected transceiver different mode control pins (e.g. STB, S, EN) are connected to I/O pins of the host microcontroller for operation mode control. The split termination approach can be further improved using the pin SPLIT of the TJA1049 or TJA1043 for DC stabilization of the common mode voltage (see Section 4.1).

In the case of the TJA1043 there is an additional INH signal line (indicated in Fig 2) controlling the voltage regulator. Leaving control over the voltage regulator(s) for V_{CC} and µC supply voltage to the TJA1043 allows for an extremely low ECU quiescent current as required in Clamp-30 applications (see Section 1.1).

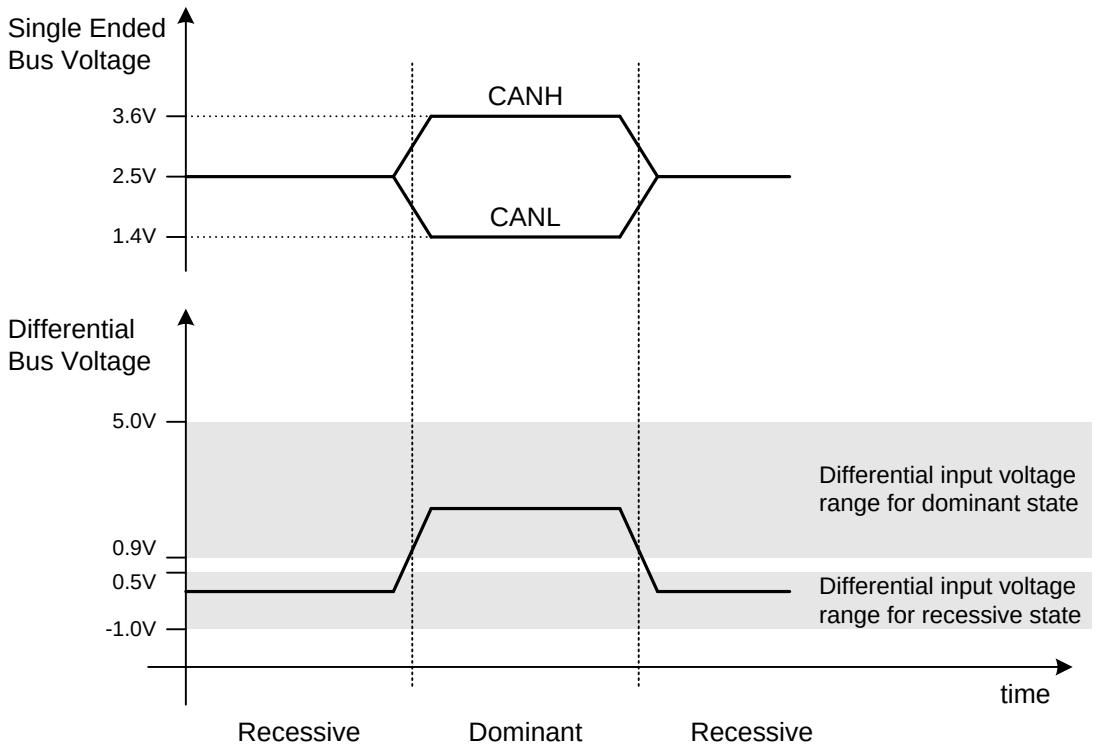


Fig 3. Nominal bus levels according to ISO11898

The protocol controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within each NXP high speed CAN transceiver sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition. In the recessive state (Fig 3) the CANH and CANL pins are biased to a voltage level of $V_{CC}/2$. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line (Fig 3). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. This is illustrated in Fig 4 showing the high speed CAN driver block diagram.

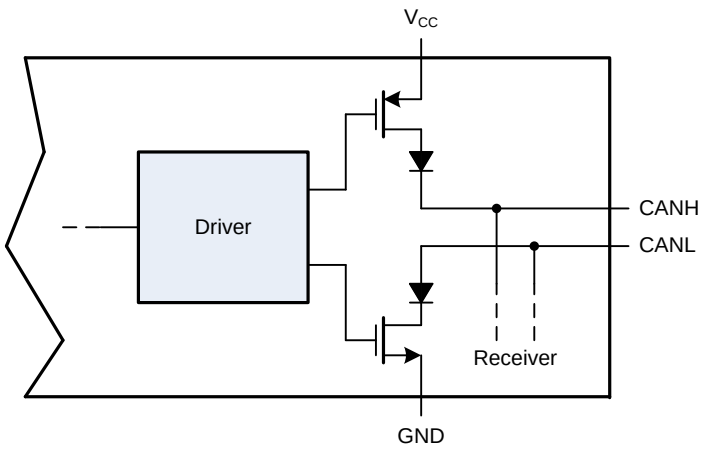


Fig 4. High speed CAN driver block diagram

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

2.2 Power management depended high speed CAN transceiver selection

In-vehicle high speed CAN networks come with different requirements, depending on the implemented application. First of all, high speed CAN is the ideal choice for all applications which require a high data throughput (up to 1 Mbit/s).

From the ECU power management point of view four different application areas can be distinguished.

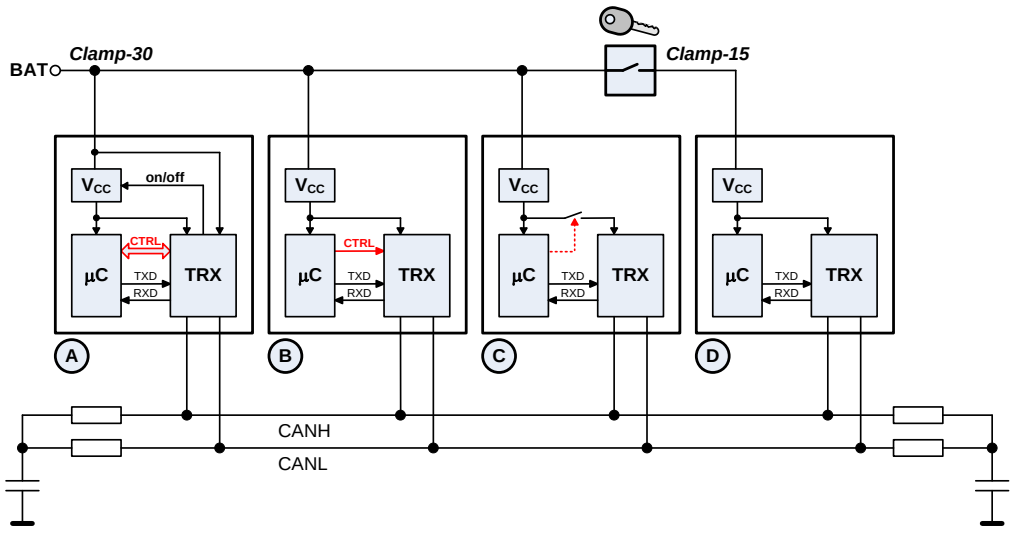


Fig 5. Target applications for HSCAN transceivers

Type A – Available all time - Applications, which have to be available all time, even when the car is parked and ignition-key is off, are permanently supplied from a permanent battery supply line, often called “Clamp-30”. However, those nodes need the possibility to reduce the current consumption for power saving by control of the local ECU supply (V_{CC}). These type A applications allow switching off the entire supply system of the ECU including the microcontroller supply while keeping the wake-up capability via CAN possible.

The TJA1043 from NXP Semiconductors [6] is the first choice for these applications. It can be put into its Sleep Mode (all V_{CC} and V_{IO} supplies off), which allows reducing the total current consumption of the entire ECU down to typically 20uA, while keeping the capability to receive wake-up events from the bus and to restart the application.

Type B – Always active microcontroller - Those applications, which need an always-active microcontroller, are permanently supplied from the battery supply line “Clamp-30” using a continuously active V_{CC} supply. In order to reduce the ECU power consumption, the transceiver needs to be set into a mode with reduced supply current while its supply stays active.

Here the Standby Mode of the TJA1049 and TJA1048 [8] offers the best choice. During Standby Mode the device reduces the transceiver supply current (via V_{CC} and V_{IO}) to a minimum, while still monitoring the CAN bus lines for bus traffic.

If monitoring the bus traffic is not required the TJA1051/E [10] is the best selection. The TJA1051/E can be switched into Off Mode. During Off Mode the device reduces the

transceiver supply current (as in Standby Mode of the TJA1049) and additionally disengages from the bus (zero load).

Type C – Always active microcontroller & controlled transceiver supply - Dedicated applications, which need an always-active microcontroller and therefore are permanently supplied from the “Clamp-30” line, additionally come with a microcontroller controlled transceiver voltage supply. In contrast to type B applications, further current can be saved, because the transceiver becomes completely un-powered by microcontroller control. These applications require absolute passive bus behavior of the transceiver, while its voltage supply is inactive. This is important in order not to affect the remaining bus system, which might continue communication.

Most suitable for such kind of applications are the TJA1049 variants, the TJA1051 variants as well as the TJA1048. All named HSCAN transceiver types disengage from the bus, if unpowered and thus behave absolutely passive.

Type D – Only active at ignition-key switched on - Applications, which do not need to be available with ignition-key off, are simply switched off and become totally un-powered during ignition-key off. They are supplied from a switched battery supply line, often called “Clamp-15”. This supply line is only switched on with ignition-key on. Depending on system requirements, e.g. partial communication of the still supplied nodes during ignition-key off, these un-powered nodes need to behave passively towards the remaining bus, similar to type C applications.

As for type C applications, it is recommended to use the TJA1049 variants, the TJA1051 variants as well as the TJA1048 due to their absolutely passive behavior to the bus when becoming unpowered.

3. The TJA1049 – High speed CAN transceiver with Standby Mode

3.1 Main features

The TJA1049 is the high speed CAN transceiver providing a low power mode (called Standby Mode) beside a Normal Mode.

- TJA1049 – 100% backwards compatible with the TJA1040:

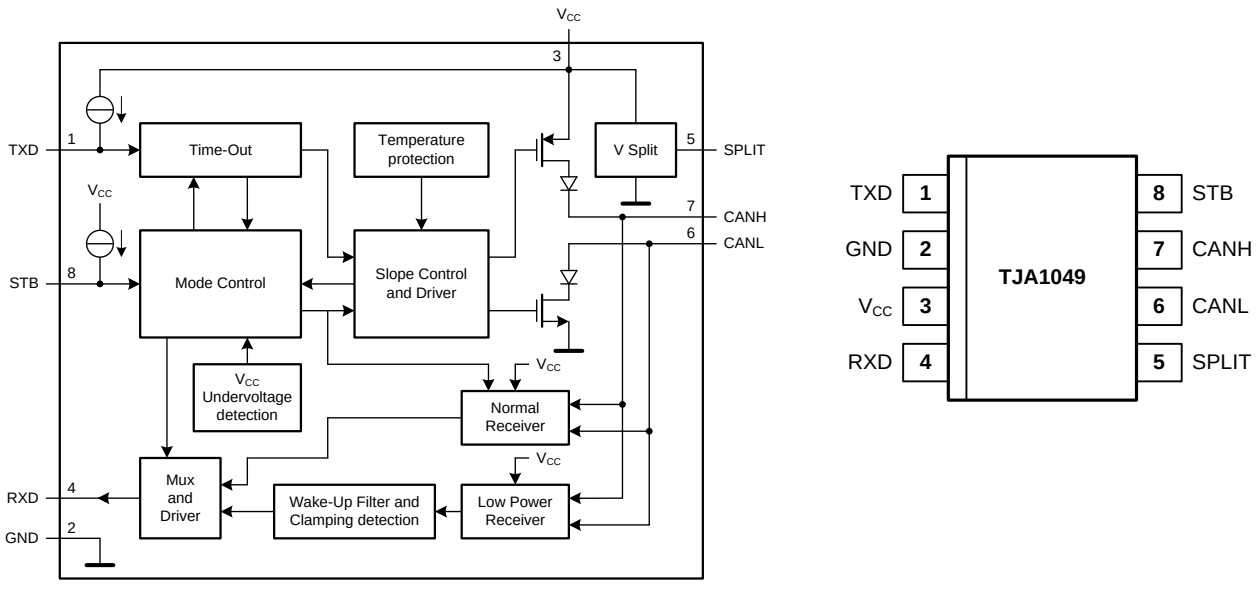


Fig 6. Block diagram and pinning of the TJA1049

3.2 Operation modes

The TJA1049 offers 2 different power modes, Normal Mode and Standby Mode which are directly selectable. Taking into account the undervoltage detection a third power mode is available, the so-called OFF Mode. Fig 7 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

Table 1. Characteristics of the different modes

Operating mode	STB pin	V_{CC} < $V_{uvd(stb)}$	V_{CC} < $V_{uvd(swoff)}$	RXD pin		Bus bias	SPLIT pin	TXD pin	CAN driver
				Low	High				
Normal	0	no	no	Bus dominant	Bus recessive	$V_{CC}/2$	$V_{CC}/2$	0	dominant [1]
								1	recessive
Standby	1	X	no	Wake-up request detected	No wake-up request detected	GND	float	X	off
	X	yes	no						
OFF	X	X	yes	-	-	float	float	X	off

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter.

3.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin STB to LOW.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- Pin RXD reflects the normal CAN Receiver.
- SPLIT is biased to $V_{CC}/2$.
- V_{CC} undervoltage detectors for Standby Mode ($V_{uvd(stb)(VCC)}$) and for Off Mode ($V_{uvd(swoff)(VCC)}$) are active.

3.2.2 Standby Mode

The Standby Mode is used to reduce the power consumption of the TJA1049 significantly. In Standby Mode the TJA1049 is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages.

Only a low power CAN receiver is active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin.

To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal Mode. The Standby Mode is selected setting pin STB to HIGH or by standby undervoltage detection on pin V_{CC} ($V_{CC} < V_{uvd(stb)(VCC)}$). Due to an internal pull-up function on the STB pin it is the default mode if pin STB is unconnected.

In Standby Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is active.
- CANH and CANL are biased to GND.
- SPLIT is floating (lowest leakage current on SPLIT pin).
- Pin RXD reflects the low-power CAN Receiver.
- V_{CC} undervoltage detectors for Standby Mode ($V_{uvd(stb)(VCC)}$) and for Off Mode ($V_{uvd(swoff)(VCC)}$) are active.

3.2.3 OFF Mode

The non-operation OFF Mode is introduced offering total passive behaviour to the CAN bus system. The OFF Mode is entered by off undervoltage detection on pin V_{CC} (V_{CC} < $V_{uvd(swoff)(VCC)}$).

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- SPLIT is floating (lowest leakage current on SPLIT pin).
- V_{CC} undervoltage detectors for Standby Mode ($V_{uvd(stb)(VCC)}$) and for Off Mode ($V_{uvd(swoff)(VCC)}$) are active.

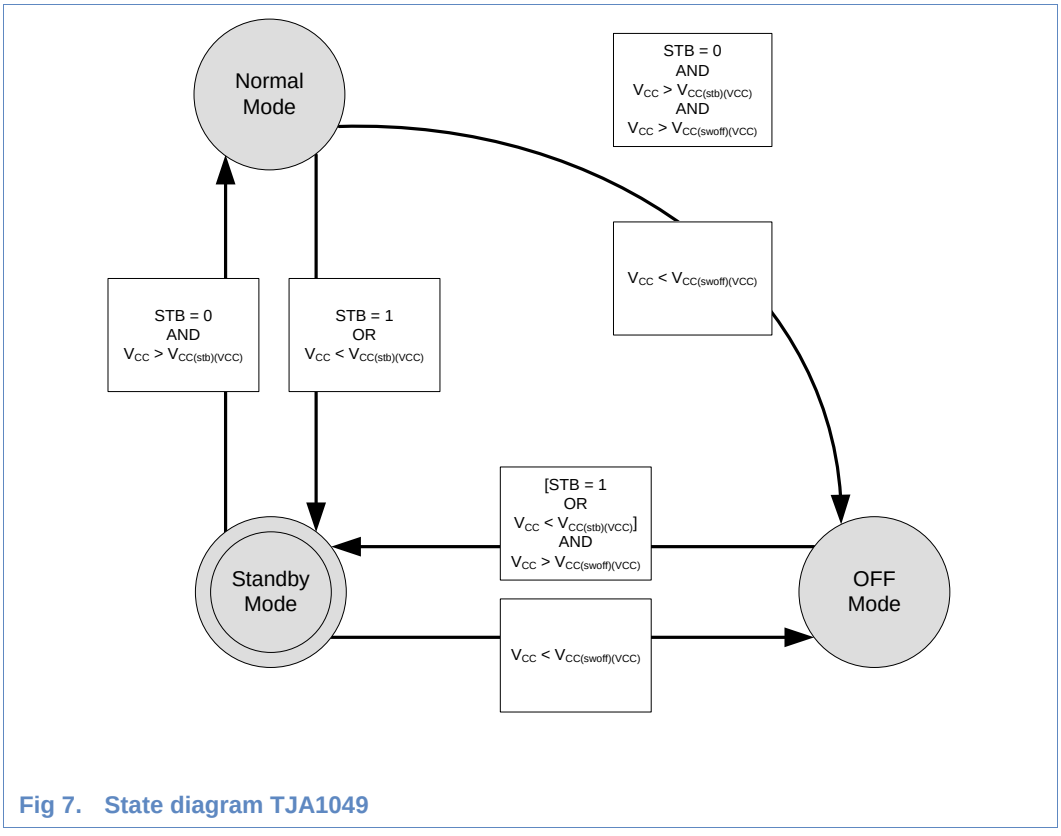


Fig 7. State diagram TJA1049

3.3 System fail-safe features

3.3.1 TXD dominant clamping detection in Normal Mode

The TXD dominant clamping detection prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{to(dom)TXD}$ the transmitter is disabled. According to the CAN protocol only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 40 kbit/s.

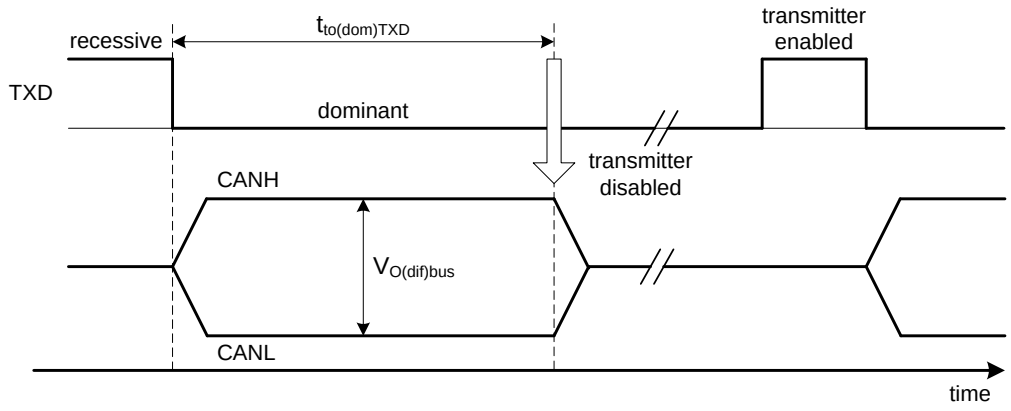


Fig 8. TXD dominant clamping in Normal Mode

3.3.2 Bus dominant clamping prevention at entering Normal Mode

Before transmitting the first dominant bit to the bus in Normal Mode the TXD pin once needs to be set HIGH in order to prevent a transceiver initially clamping the entire bus when starting up with not well defined TXD port setting of the microcontroller.

3.3.3 Bus dominant clamping detection in Standby Mode

For system safety reasons a new bus dominant timeout function in Standby Mode is introduced in the TJA1049. At any bus dominant condition in Standby Mode the RXD pin gets switched LOW. If the dominant condition holds for longer than the timeout $t_{to(dom)bus}$, the RXD pin gets set HIGH again in order to prevent generating a permanent wake-up request at a bus failure condition. Consequently a system can now enter the Standby Mode even with a permanently dominant clamped bus.

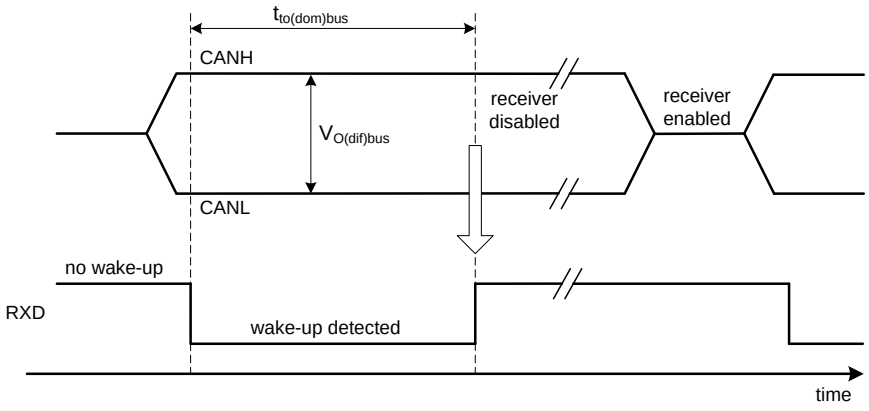


Fig 9. Bus dominant clamping in Standby Mode

3.3.4 Undervoltage detection & recovery

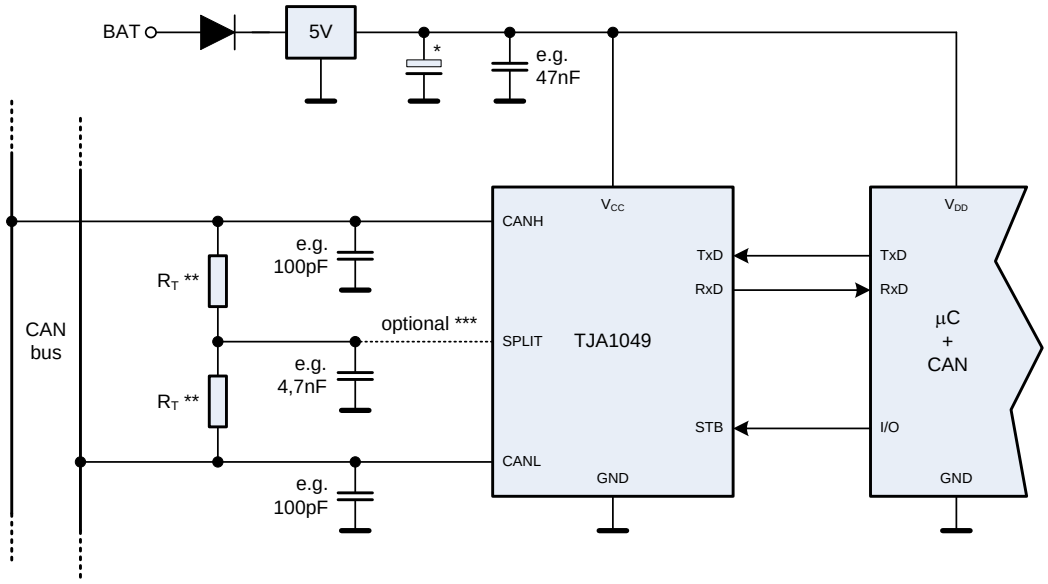
Compared to its predecessor TJA1040, the TJA1049 takes advantage of high precision integrated undervoltage detection on its supply pin (see Table 2). Without this function undervoltage conditions might result in unwanted system behavior, if the supply leaves the specified range. (e.g. the bus pins might bias to GND).

Table 2. TJA1049 mode control at undervoltage conditions

Undervoltage condition		HS-CAN with Standby Mode
$V_{CC} < V_{uvd(stb)}$	$V_{CC} < V_{uvd(swoff)}$	TJA1049
no	no	Normal or Standby
yes	no	Standby
no	yes	not applicable
yes	yes	OFF

4. Hardware application

Fig 10 shows how to integrate the TJA1049 within a typical application. There is a dedicated 5V regulator supplying the TJA1049 transceiver on its V_{CC} supply pin (necessary for proper CAN transmit capability).



* Size of capacitor depends on regulator.
** For bus line end nodes RT = 60Ohm in order to support the „Split termination concept“
For stub nodes an optional "weak" termination of e.g. RT = 1,3kOhm can be foreseen, if required by the OEM.
*** Optional common mode stabilization by a voltage source of $V_{CC}/2$ at the pin SPLIT.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 10. Typical application with TJA1049 and a 5V microcontroller

4.1 Supply pin V_{CC}

The V_{CC} supply provides the current needed for the transmitter and receiver of the high speed CAN transceiver. The V_{CC} supply must be able to deliver current of 65 mA for the transceiver (see chapter 4.1.1).

Typically a capacitor between 47nF and 100nF is recommended being connected between V_{CC} and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand. For reliability reasons it might be useful to apply two capacitors in series connection between V_{CC} and GND. A single shorted capacitor (e.g. damaged device) cannot short-circuit the V_{CC} supply.

Using a linear voltage regulator, it is recommended to stabilize the output voltage with an additional bypass capacitor (see chapter 4.1.2) that is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in chapter 4.1.2, while in chapter 4.1.1 the average V_{CC} supply current is calculated for thermal load considerations of the V_{CC} voltage regulator. This can be done in absence and in presence of bus short-circuit conditions.

4.1.1 Thermal load consideration for the V_{CC} voltage regulator

The averages V_{CC} supply current can be calculated in absence and in presence of bus short-circuit conditions. Assuming a transmit duty cycle of 50% on pin TXD the maximum average supply current in absence of bus failures calculates to:

$$I_{CC\_norm\_avg} = 0.5 \bullet (I_{CC\_REC\_MAX} + I_{CC\_DOM\_MAX})$$

Table 3. Maximum V_{CC} supply current in recessive and dominant state

Device	$I_{CC\_REC\_MAX}$ [mA]	$I_{CC\_DOM\_MAX}$ [mA]
TJA1049	10	70

In presence of bus failures the V_{CC} supply current for the transceiver can increase significantly. The maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ flows in the case of a short circuit from CANH to GND. Along with the CANH short circuit output current $I_{O(SC)}$ the maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ calculates to about 120mA. This results in an average supply current of 65mA in worst case of a short circuit from CANH to GND. The V_{CC} voltage regulator must be able to handle this average supply current.

4.1.2 Dimensioning the bypass capacitor of the voltage regulator

Depending on the power supply concept, the required worst-case bypass capacitor and the extra current demand in the case of bus failures can be calculated.

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Dimensioning the capacitor gets very important with a shared voltage supply between transceiver and microcontroller. Here, extra current demand with bus failures may not lead to an unstable supply for the microcontroller. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{CC} supply current I_{CC_REC}.

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max} = (I_{CC\_DOM\_MAX} - I_{CC\_REC\_MIN})$$

In presence of bus failures the maximum extra supply current may be significantly higher.

Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max\_sc} = (I_{CC\_DOM\_SC\_MAX} - I_{CC\_REC\_MIN})$$

Example:

With $I_{CC\_dom\_sc\_max}$ = 120 mA (estimated) and $I_{CC\_rec\_min}$ = 2 mA the maximum extra supply current calculates to

$\Delta I_{CC\_max\_sc}$ = 118 mA

In the case of a short circuit from CANH to GND, the bus is clamped to the recessive state, and according to the CAN protocol the uC transmits 17 subsequent dominant bits on TXD. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times. The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the V_{CC} supply current becomes reduced to the recessive one.

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Whereas ΔV_{max} is the maximum allowed voltage drop at pin V_{CC} and t_{dom_max} is the dominant time of 17 bit times at 500kbit/s.

Table 4. Average V_{CC} supply current (assuming 500kbit/s)

Device	$\Delta I_{CC\_max\_sc}$	t_{dom_max}	ΔV_{max}	C_{BuFF}
TJA1049	108mA	34µs	0,5V	≈ 10µF

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

4.2 TXD pin

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show very fast slopes, it may cause a degradation of the EMC performance. Depending on the OEM an optinal series resistor of up to 1kΩ within the TXD line between transceiver and microcontroller might be useful. Along with pin capacitance this would help to smooth the edges for some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

4.3 RXD pin

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of up to 1 kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

4.4 Mode control pin STB

This input pin is a mode pin and used for mode control. They are typically directly connected to an output port pin of a microcontroller.

4.5 Bus Pins CANH / CANL

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination, illustrated in Fig 12. EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω (or 62Ω) instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4,7nF to 47nF.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Additionally it is recommended to load the CANH and CANL pin each with a capacitor of about 100pF close to the connector of the ECU (see Fig 11). The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

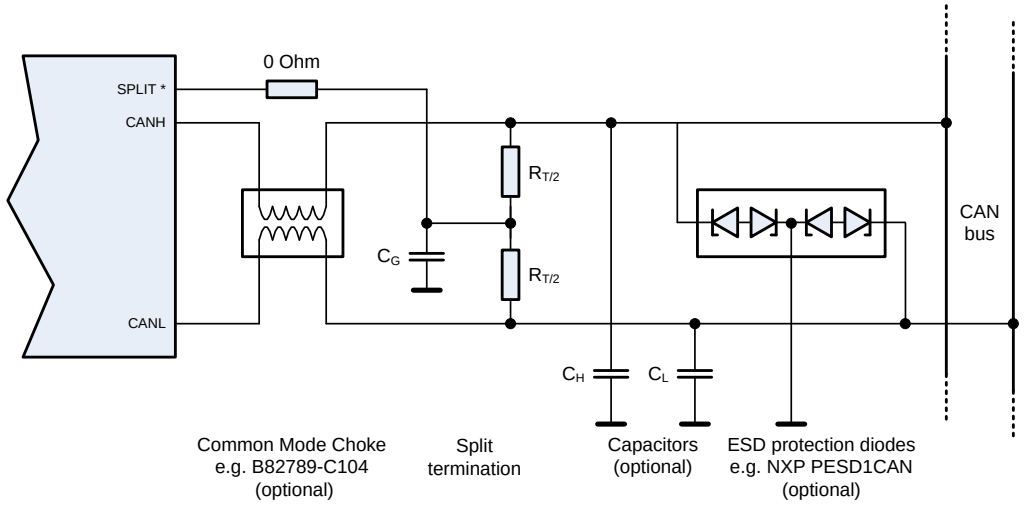
OEMs might have dedicated circuits prescribed in their specifications. Please refer to the corresponding OEM specifications for individual details.

5. EMC aspects of high speed CAN

Achieving a high EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry and PCB layout) is also very important.

The possibilities to further improve the EMC performance include differential and common mode filters, shielded twisted pair cable and ESD protections diodes. Additionally the PCB layout is critical to maximize the effectiveness of the EMC improvement circuit. All additional circuits could distort the signal waveform and they are also limited by the physical layer specifications.

This chapter presents some application hints (all are referenced to Fig 11) aiming to exploit the outstanding EMC performance of the TJA1049 high speed CAN transceivers.



* TJA1042, TJA1043 only.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 11. Optional circuitry at CANH and CANL

5.1 Common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry get effectively attenuated while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances without adding a large amount of distortion on CAN lines.

Former transceiver devices usually needed a common mode choke to fulfill the stringent emission and immunity requirements of the automotive industry when using unshielded twisted-pair cable. The TJA1049 has the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

Besides the RF noise reduction the stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with stray inductance lower than 500nH. Bifilar wound chokes typically show an even lower stray inductance. Fig 11 shows an application, using a common mode choke. As shown the choke shall be placed nearest to the transceiver bus pins.

5.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND (C_H and C_L) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish a RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500kbit/s, call for a value of lower than 100pF (see also SAE J2284 and ISO11898). At a bit rate of 125kbit/s the capacitor value should not exceed 470pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the optional ESD clamping diodes as shown in Fig 11.

5.3 ESD protection diodes

The TJA1049 is designed to withstand ESD pulses of up to

- ±8kV according to the IEC61000-4-2 and
- ±8kV according to the Human Body Model
- ±300V according to the Machine Model
- ±500V according to the Charged Device Model

at bus pins CANH, CANL and pin SPLIT and thus typically does not need further external measures. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL line.

NXP Semiconductors offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The so-called PESD1CAN [11] and PESD2CAN [12] protection devices featuring a very fast diode structure with very low capacitance (typ. 11pF), is compliant to IEC61000-4-2 (level 4), thus allowing air and contact discharge of more than 15kV and 8kV, respectively. Tests at an independent test house have confirmed typically more than 20kV ESD robustness for ECUs equipped with the PESD1CAN and a choke. To be most effective the PESD1CAN diode shall be placed close to the connector of the ECU as shown in Fig 11.

5.4 Power supply buffering

Emission and immunity of transceivers also depend on signal dynamic behaviour. The capacitors placed at voltage supply pins buffer the voltage and provide the sharp rise current needed during the transition from recessive to dominant state. To calculate the size of the capacitance please refers to chapter 4.1.2.

5.5 Split termination concept

The transceiver is connected to the bus via pins CANH and CANL. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Practice has shown that effective reduction of emission can be achieved by a modified bus termination concept called split termination. Instead of a one-resistor termination it is highly recommended using the split termination, illustrated in Fig 12. In addition this concept contributes to higher immunity of the bus system.

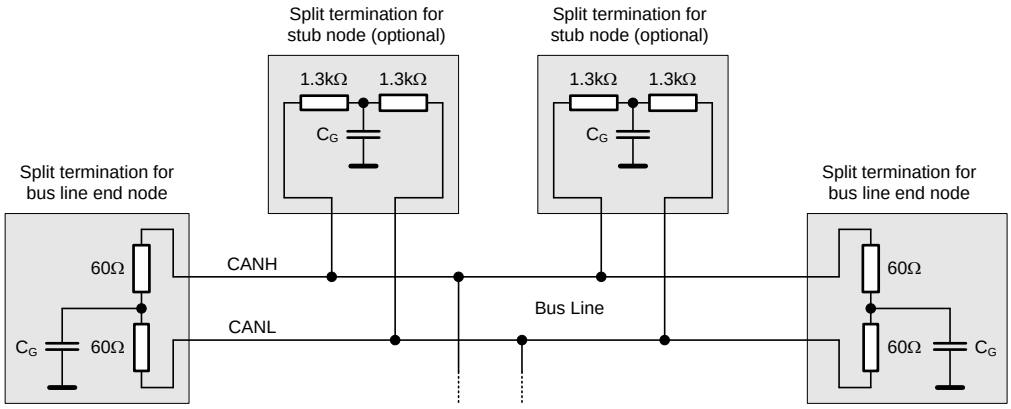


Fig 12. Typical split termination concept

Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the bus load of all the termination resistors stays within the specified range from 45Ω to 65Ω. As an example for up to 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value is 1.3 kΩ. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. Together with the resistors this termination concept works as a low pass filter. The recommended value for this capacitor is in the range of 4,7nF and 47nF.

In case of many high-ohmic stub nodes it can be considered to increase the main bus termination of 2 times 60Ω towards 2 times 62Ω or more. Since an automotive bus system is never “ideal” with respect to “beginning” and “end”, the overall termination is always a compromise. With that in mind, it might even be considered to have just one central bus termination in the star point of a system using 2 times 31Ω as an example.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: < 2 %).

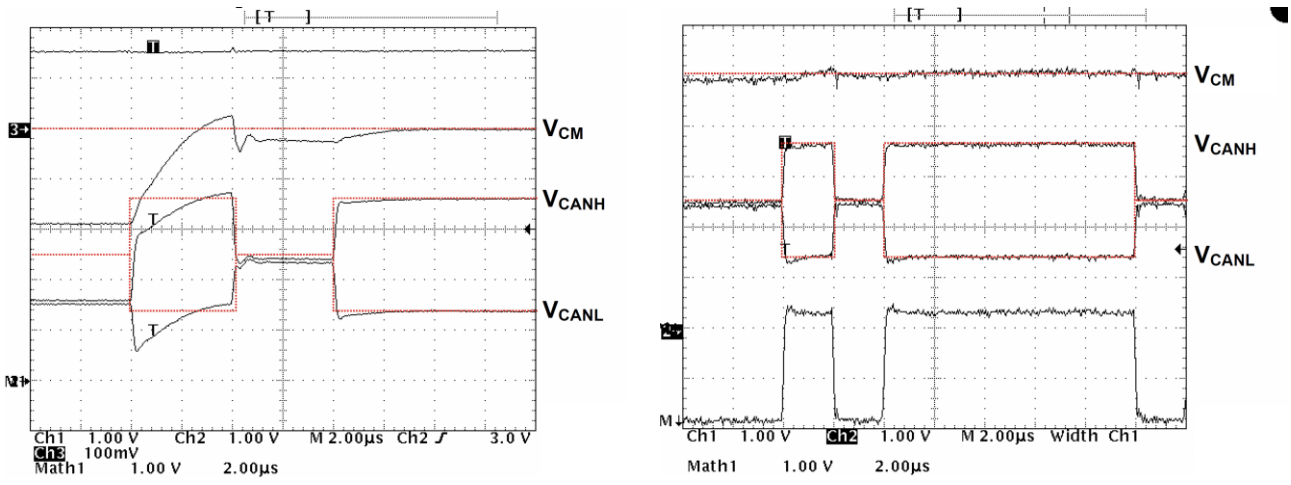
Generally the termination strategy is prescribed by the individual OEM. Please refer to the corresponding specifications for details.

5.6 Summary of EMC improvements

The TJA1049 has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the system performance is still not sufficient, there will be the option to use additional measures like the SPLIT pin, common mode chokes, capacitors and ESD clamping diodes.

5.7 Common mode stabilization via SPLIT pin

The high impedance characteristic of the bus during recessive state leaves the bus vulnerable to even small leakage currents, which may occur with un-powered competitor high speed CAN transceivers of ECUs within the bus system. As a result the common mode voltage can show a significant voltage drop from the nominal $V_{CC}/2$ value. Subsequent transmitting of the first dominant bit of a CAN-message (Start-of-Frame Bit) the common mode voltage would restore to its nominal value, leading to a large common mode step and increasing emission.



(1) Common mode 'jump' at the start of each CAN message without using SPLIT pin

(2) Common mode 'jump' effectively reduced using SPLIT pin

Fig 13. Signal common mode stabilization using SPLIT pin

The TJA1049 provides means for common mode stabilization by offering a voltage source of nominal $V_{CC}/2$ at the pin SPLIT. In fact the common mode stabilization via pin SPLIT of the TJA1049 significantly improves the EMC performance. It should be used if there are un-powered nodes while other nodes keep communicating. The DC stabilization aims to oppose this degradation and helps improving the emission

performance. With no significant leakage currents from the bus, the pin SPLIT can be left open. According to the data sheet [6] the maximum impedance of the voltage source can be calculated to about 2kΩ.

5.8 GND offset and Common mode range

Bus systems in automotive have to deal with ground-offsets between the various nodes. This means that each node can “see” different single-ended bus voltages on the bus lines according to their own ground level, whereas the differential bus voltage remains unaffected.

The TJA1049 allows a maximum single-ended voltage at CANH of +12 V, while the maximum allowable single-ended voltage of CANL is -12 V. With single-ended bus voltages within this range, it is guaranteed that the differential receiver threshold voltage lies between 0.5 and 0.9 V in Normal Mode. The allowable single-ended voltage range is known as the common mode range of the differential receiver. Even the ISO11898-5 [14] calls for a common mode range from -12 V to +12 V.

Slightly exceeding the specified common mode range does not lead immediately to communication failures, but significant exceeding has to be avoided. There is a limitation for tolerable ground-offsets. The relation between the common mode range and the maximum allowable ground-offset is illustrated in Fig 14 and Fig 15. Fig 14 shows the case where the ground level of a transmitting node 2 lies above that of a receiving node 1. In this case the maximum allowable ground-offset corresponds to the maximum single-ended voltage of 12 V for CANH with respect to the ground level of the receiving node. The maximum allowable ground-offset can be derived from Fig 14 to be 8V ($GND_{transmit}$ - $GND_{receive}$).

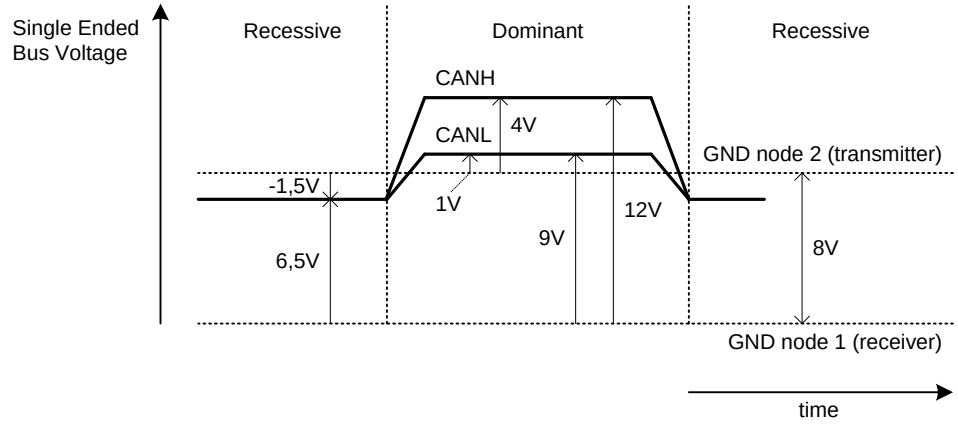


Fig 14. Ground level of the transmitting node 2 lies above that of the receiving node 1

Fig 15 shows the case where the ground level of the sending node 1 lies below that of the receiving node 2. In this case the maximum allowable ground-offset corresponds to the minimum single-ended voltage of -12 V for CANL with respect to the ground level of the receiving node 2. The maximum allowable ground-offset can be derived from Fig 15 to be -13V ($GND_{transmit}$ - $GND_{receive}$). As each node in a bus system acts temporarily as transmitter, the maximum allowable ground-offset for the TJA1049 between any two nodes is limited to 8V.

In recessive bus state each node tries to pull the bus lines according to their biasing and ground level resulting in an average recessive bus voltage. In the example of Fig 14 the recessive bus voltage is found to be around 6,5V with respect to the ground level of the receiving node and -1,5V with respect to the ground level of the sending node.

The two examples in Fig 14 and Fig 15 indicate that ground-offsets in a bus system disturb significantly the symmetrical character of CANH and CANL with respect to the recessive voltage level. This implies the generation of unwanted common mode signals, which increase electromagnetic emission. Since emission is very sensitive towards ground-offsets, appropriate system implementation has to prevent ground-offset sources.

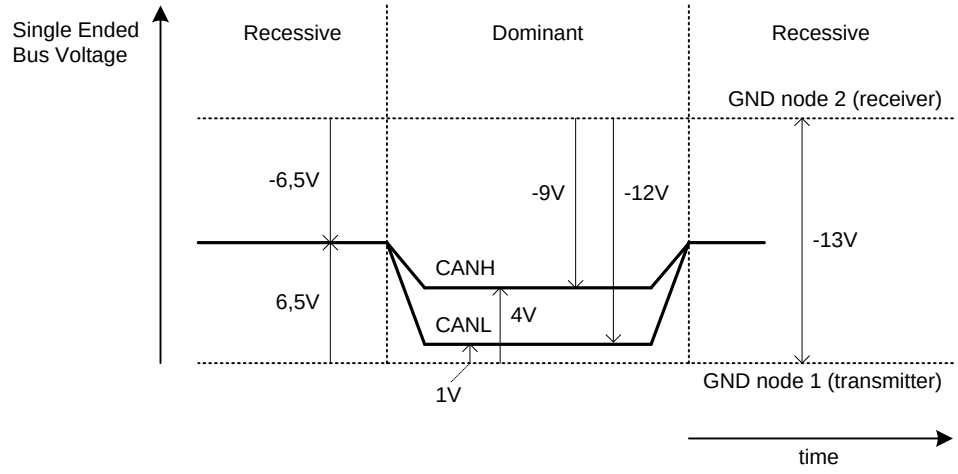


Fig 15. Ground level of the transmitting node 2 lies below that of the receiving node 1

Remark: From static (DC) point of view such high voltage shifts are not considered in automotive applications between different nodes. Nevertheless under electromagnetic interferences (dynamically) a high Common Mode Range enhances the immunity of a high speed CAN transceiver because of dynamic ground offsets between nodes.

5.9 PCB layout rules (check list)

Following guidelines should be considered for the PCB layout.

- When a common mode choke is used, it should be placed close to the transceiver bus pins CANH and CANL.
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed 10cm.
- Avoid routing other “off-board” signal lines parallel to the CANH/CANL lines on the PCB due to potential “single ended” noise injection into CAN wires.
- The ESD protection should be connected close to the ECU connector bus terminals.
- Place the V_{CC} capacitor close to transceiver pin.
- The track length between communication controller / µC and transceiver should be as short as possible
- The ground impedance between communication controller (µC) and transceiver should be as low as possible.
- Avoid applying filter elements into the GND signal of the µC or the Transceiver. GND has to be the same for Transceiver and µC.

6. Bus network aspects of high speed CAN

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

6.1 Maximum number of nodes

The number of nodes, which can be connected to a bus, depends on the minimum load resistance a transceiver can drive. The TJA1049 provides an output drive capability down to a minimum load of $R_{L,min}$ = 45Ohm for V_{CC} > 4,75 V. The overall busload is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver's differential input resistance $R_{i(dif)}$. The DC circuit model of a bus system is shown in Fig 16. For worst case consideration the bus line resistance R_W is considered to be zero. This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T,\min} * R_{i(dif),\min}}{n_{\max} * R_{T,\min} * 2R_{i(dif),\min}} \geq R_{L,\min}$$

Rearranged to n_{max}:

$$n_{\max} \leq R_{i(dif),\min} * \left(\frac{1}{R_{L,\min}} - \frac{2}{R_{T,\min}} \right)$$

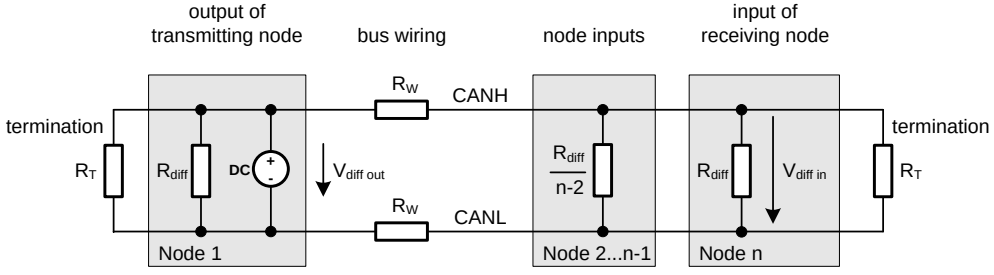


Fig 16. DC circuit model for a bus system according to ISO11898

Table 5 gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Table 5. Maximum number of nodes (see data sheets for $R_{dif,min}$ and $R_{L,min}$)

Transceiver	$R_{i(dif),min}$(kOhm)	$R_{L,min}$(Ohm)	Nodes (maximum) ($R_{T,min}$=118Ohm)	Nodes (maximum) ($R_{T,min}$=130Ohm)
TJA1049	19	45	100	129

6.2 Maximum bus line length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. Loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line.
2. Relative oscillator tolerance between nodes.
3. Signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to [16]).

Effects 1 and 2 result in a value for the maximum bus line length with respect to the CAN bit timing [16]. Effect 3, on the other hand, results in a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Table 6. Maximum bus line length for some standards

Specification	Data rate		
	125 kBit/s (BT tol. = +/- 1,25%)	250 kBit/s (BT tol. = +/- 0,75%)	500 kBit/s (BT tol. = +/- 0,5%)
SAE J2284	50 m	50 m	33 m
TJA1049	80 m	80 m	40 m

(BT tol. = Bit Time Tolerance)

Table 6 gives the maximum bus line length for the bit rates 125 kbit/s, 250 kbit/s and 500 kbit/s, along with values specified in the SAE J2284 [15] standard associated to CAN. The calculation is based on effects 1 and 2 assuming a minimum propagation delay between any two nodes of 200 ns and a maximum bus signal delay of 8 ns/m. Notice that the stated values apply only for a well-terminated linear topology. Bad signal quality because of inadequate termination can lower the maximum allowable bus line length.

6.3 Topology

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 7 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard. Notice that SAE J2284 specifies the twist rate r_{twist} in addition.

Table 7. Physical media parameters of a pair of wires (shielded or unshielded)

Parameter	Notation	Unit	ISO11898			SAE J2284		
			Min.	Typ.	Max.	Min.	Typ.	Max.
Impedance	Z	Ohm	95	120	140	108	120	132
Length-related resistance	R_{Length}	mOhm/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5,5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

Ringing due to signal reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol features:

- Only recessive to dominant transitions are used for resynchronization.
- Resynchronization is allowed only once between the sample points of two bits and only, if the previous bit was sampled and processed with recessive value.
- The sample point is programmable to be close to the end of the bit time.

Linear topology

The high speed CAN standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via not terminated drop cables or stubs to the bus. To keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0.3 m at 1 Mbit/s. The corresponding SAE standard, J2284-500, recommends keeping the stub length below 1 m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same [15] . Table 8 along with Fig 17 illustrate the topology requirements of the SAE J2284-500 standard. At lower bit rates the maximum distance between any two ECUs as well as the ECU cable stub lengths may become longer.

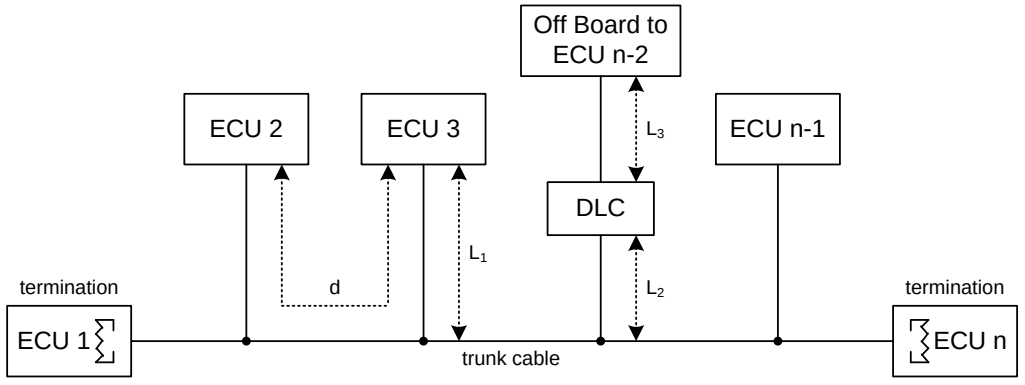


Fig 17. Topology requirements of SAE J2284

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length.

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is sometimes used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology.

Table 8. ECU topology requirements of SAE J2284-500

Parameter	Symbol	Unit	Min.	Nom.	Max.
ECU cable stub length	L1	m	0	-	1
In-vehicle DLC cable stub length	L2	m	0	-	1
Off board DLC cable stub length	L3	m	0	-	5
Distance between any two ECUs	D	m	0,1	-	33

Note: It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system setup.

7. Appendix

7.1 Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the TJA1049 HS-CAN transceiver are short-circuited to supply voltages like V_{BAT}, V_{CC}, GND or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 9.

Table 9. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

Table 10. TJA1049 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	Undervoltage detected; TRX enters Off Mode
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) SPLIT	D	Bus charged to V_{BAT} level; Bit timing violation possible	D	Bus charged to V_{CC} level; Bit timing violation possible
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit iming violation possible
(8) STB	A	Limiting value exceeded	C	Normal Mode not selectable

Table 11. TJA1049 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode	C	V_{CC} undervoltage detected; TRX enters Off Mode
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) SPLIT	D	Bus discharged to GND level; Bit timing violation possible	D	No DC common mode stabilization
(6) CANL	C	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) STB	D	Standby Mode not selectable	C	Normal Mode not selectable

Table 12. TJA1049 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode
V_{CC} - RXD	C	RXD clamped recessive
SPLIT - CANL	D	Degration of EMC; Bit timing violation possible
CANL - CANH	B	No bus communication
CANH - STB	C	TRX is not able to enter Normal Mode if the bus is driven dominant

7.2 Upgrading hints TJA1040 – TJA1049

Characteristics

In Table 13 an overview on the changed and thus improved characteristics of the TJA1049 is given.

Table 13. Improved characteristics of the TJA1049

Characteristics	HS-CAN with Standby Mode	
	2nd generation	3rd generation
	TJA1040	TJA1049
Voltage robustness, CAN bus	-27V to +40V	-58V to +58V
Voltage robustness, other pins	-0,3V to +6V	-0,3V to +7V
ESD robustness IEC61000-4-2	~ +/-2kV	+/-8kV
ESD robustness HBM	+/-6kV	+/-8kV
Loop Delay (TXD-RXD)	255ns	220ns
Shutdown junction temperature	~165°C	~190°C

In order to offer full 24V application support e.g. for truck applications the bus related pins CANH, CANL (and SPLIT) offer an extended voltage robustness from -58V to +58V. All I/O pins are robust up to 7V DC voltage.

Excellent ESD protection on the bus related pins offers more than state-of-the-art robustness of -/+8kV according to the standard IEC61000-4-2 (C = 150pF, R = 330Ohm). Beside of this also the ESD robustness according the HBM (Human Body Model) got increased. With this excellent ESD robustness the TJA1049 is the first-choice to be used without externally applied ESD protection measures.

A much smaller loop delay from TXD to RXD allows to build larger network topologies.

The over temperature protection is extended to a higher threshold in order to allow the TJA1049 to be used even in frequently high temperature applications (e.g. gear box applications).

Functionality

Fig 14 shows the advantages of the TJA1049 from functional point of view. Items that are covered in the previous chapter are not mentioned in the detailed description below.

Table 14. Improved functionality of TJA1049

Features	HS-CAN with Standby Mode	
	2nd generation	3rd generation
	TJA1040	TJA1049
Full 24V application support	-	√
Gap-less behaviour at supply undervoltage	-	√
EMC optimized CAN slopes for big networks	-	√
Bus dominant clamping detection in Standby Mode	-	√
RXD – V_{CC} reverse supply protection In Standby Mode	-	√
Receiver hysteresis for improved noise robustness	-	√
STB input pin glitch filter	-	√

Hardware

The TJA1049 offers very low ElectroMagnetic Emission (EME), very high ESD robustness and voltage robustness on their bus pins.

With these new features it is up to the hardware developer to consider the following hardware simplifications:

- Remove common mode choke, because the Electro Magnetic Emission is very low even without choke.
- Remove ESD protection components (e.g. ESD diodes), because ESD pin robustness is higher than required by main OEMs.
- If the TJA1049 is to be used to replace the TJA1040 in 24V applications (e.g. trucks) external applied zener diodes on the CAN pins to keep the voltage below 30V get redundant, because the new voltage robustness is specified up to -/+58V.

Software

From software point of view no changes need to be implemented in order to replace the TJA1040 by its successors.

8. Abbreviations

Table 15. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
DLC	Data Link Control
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESD	Electrostatic Discharge
FMEA	Failure Mode and Effects Analysis
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board

9. References

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