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Errata to MPC8568E PowerQUICC III™ Integrated Processor Family Reference Manual, Rev. 1

This errata describes corrections to the *MPC8568E PowerQUICC III™ Integrated Processor Family Reference Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No. **Changes**

2.4, 2-67 In Table 2-11, "Memory Map," add SRDSCR0 and SRDSCR1 after CLKOCR, as follows:

Table 2-11. Memory Map

Offset	Register	Access	Reset	Section/Page
Debug Control				
0xE_0E00	CLKOCR—Clock out control register	R/W	All zeros	21.4.1.28/21-31
0xE_0F04	SRDSCR0—SerDes control register 0	R/W	*nn*00_*nn*00	21.4.1.29/21-32
0xE_0F08	SRDSCR1—SerDes control register 1	R/W	All zeros	21.4.1.30/21-33

2.5, 2-72 Update Table 2-13, "Detailed QUICC Engine Block Memory Map," as follows:

- Change offsets for SIRERC1–SIRHRC1 to SI1_BASE + 0x38–SI1_BASE + 0x3B.
- Change offsets SI1_BASE + 0x34–SI1_BASE + 0x37 and SI1_BASE + 0x3C–SI1_BASE + 0x3F to reserved.

- Change offset for UCCSx in slow protocol to UCCx_BASE + 0x18.
- Add QUICC Engine microcode revision number register (CEURNR) at offset 0x01B8. **NOTE: See *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM) for CEURNR.**
- Add overrun condition in Rx FIFO counter register (RxDiscOV) at offset UCCx_BASE + 0x1C6.
- Change offsets 0x4080–0x4400 to reserved.

3.1, 3-9 — In Table 3-1, “MPC8568E Signal Reference by Functional Block,” change PC19 to correlate with IIC2_SDA.

3.4.4, 3-49 — In Table 3-10, “Port F Dedicated Pin Assignment,” for PF13, change “SP1:SPIMISO” to “SPI1:SPIMOSI.”

4.3.1.1.2, 4-5 — In Table 4-5, “CCSRBAR Bit Settings” add clarification for BASE_ADDR (bits 8–23) field description from: “Identifies the16 most-significant address bits of the window,” to: “Identifies the16 most-significant address bits of the 36-bit window.”

4.4.3.1, 4-11 — Modify Table 4-9, “CCB Clock PLL Ratio,” as follows:

Table 4-9. CCB Clock PLL Ratio

Functional Signals	Reset Configuration Name	Value (Binary)	CCB Clock : SYSCLK Ratio
LA[28:31] Default (1111)	cfg_sys_pll[0:3]	0000	16 : 1
		0001	Reserved
		0010	2 : 1
		0011	3 : 1
		0100	4 : 1
		0101	5 : 1
		0110	6 : 1
		0111	Reserved
		1000	8 : 1
		1001	9 : 1
		1010	10 : 1
		1011	Reserved
		1100	12 : 1
		1101	20: 1
		1110	Reserved
		1111	Reserved (default)

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4.4.3.2, 4-15 Modify Table 4-10, “e500 Core Clock PLL Ratios,” as follows:

Table 4-10. e500 Core Clock PLL Ratios

Functional Signals	Reset Configuration Name	Value (Binary)	e500 Core: CCB ClockRatio
LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$ Default (111)	cfg_core_pll[0:2]	000	4 : 1
		001	9 : 2 (4.5:1)
		010	Reserved
		011	3 : 2 (1.5 : 1)
		100	2 : 1
		101	5 : 2 (2.5:1)
		110	3 : 1
		111	7 : 2 (3.5 : 1)(default)

4.4.4.2.1, 4-26 Append the following sentence to the first paragraph and eliminate the remainder of the section: “See the *MPC8568E Integrated Processor Hardware Specifications* for specific supported frequencies.”

6.10.2, 6-26 In Figure 6-33, “Hardware Implementation-Dependent Register 1 (HID1),” change Access from “Supervisor read/write” to “Supervisor Mixed.”

9.3.2.1, 9-7 In Table 9-3, “Memory Interface Signals—Detailed Signal Descriptions,” change signal description of MA[15:0] from:

“Assertion/Negation—The address is always driven when the memory controller is enabled. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}n$ is active).”

to:

“Assertion/Negation—The address lines are only driven when the controller has a command scheduled to issue on the address/CMD bus; otherwise they will be at high-Z. It is valid when a transaction is driven to DRAM (when $\overline{\text{MCS}}n$ is active).”

9.5.12, 9-67 Change the first sentence of the third paragraph to say the following: “If a multi-bit error is detected for a read, the DDR memory controller logs the error and generates the interrupt, and transfer error acknowledge (TEA) is asserted internally on the CSB bus (if enabled, as described in Section 9.4.1.26, “Memory Error Disable (ERR_DISABLE)”).”

13.3.1.15, 13-29 In Table 13-21, “LBCR Field Descriptions,” modify AHD (bit 10) field description, as follows:

Address hold disable. Removes part of the hold time for LAD with respect to LALE in order to lengthen the LALE pulse.

0 During address phases on the local bus, the LALE signal negates one platform clock period prior to the address being invalidated. At 33.3 MHz,

	this provides 3 ns of additional address hold time at the external address latch. 1 During address phases on the local bus, the LALE signal negates 0.5 platform clock period prior to the address being invalidated. This halves the address hold time, but extends the latch enable duration. This may be necessary for very high frequency designs.
13.3.1.16, 13-31	In Table 13-22, “LCRR Field Descriptions,” remove “additional” from EADC (bits14–15) field description.
13.4.4, 13-57	Add the following statement to end of first paragraph: “A gap of 2 dead LCLK cycles is present on the UPM interface between UPM transactions.”
13.5.3, 13-82	Add the following note after the first paragraph: “It may not be possible to write to 16-bit devices on the local bus using 16-bit transactions on one of the external peripheral interfaces. Refer to the chapter describing the specific external interface controller for more information.”
13.5.6.2.2, 13-105	In paragraph beginning, “The remaining issue is the synchronization of the UPM cycles...” change parenthetical in final sentence from “(GPL[0:4] are 1 when inactive, GPL5 is 0 when inactive)” to “(LGPL*n* are 1 when inactive).”
15.4, 15-7	In Table 15-1, “eTSEC*n* Network Interface Signal Properties,” for RGMII and RTBI protocols, changed description of RX_ER from “Unused, output driven low” to “Unused.”
15.4, 15-8	In Table 15-1, “eTSEC*n* Network Interface Signal Properties,” modify statement in the signal descriptions for TSEC*n*_TXD[7:4] and TSEC*n*_TXD[3:0] from: “unused, output driven zero” to: “unused.”
15.5.2, 15-16	In Table 15-4, “Module Memory Map,” change reset value for RQFCR from “All zeros,” to “undefined.”
15.5.2, 15-20	In Table 15-4, “Module Memory Map,” change the access for CAR1 and CAR2 registers from Read only to w1c.
15.5.3.1.3, 15-24	Add the following sub-bullet to end of bulleted list: — Special function interrupts are: MSRO, MMRD, and MMRW.
15.5.3.1.3, 15-25	In Table 15-7, “IEVENT Field Descriptions,” replace second sentence of the CRL (bit 14) field description to say the following “The frame is discarded without being transmitted and the queue halts (TSTAT[THLT*n*] set to 1).”
15.5.3.1.6, 15-32	In Table 15-10, “ECNTRL Field Descriptions,” update AUTOZ (bit 18) field description to read as follows: “Automatically zero MIB counter values and carry registers. 0 The user must write the addressed counter zero after a host read. 1 The addressed counter value is automatically cleared to zero after a host read. This is a steady state signal and must be set prior to enabling the Ethernet controller and must not be changed without proper care.”

15.5.3.1.6, 15-32 In Table 15-10, “ECNTRL Field Descriptions,” update CLRCNT (bit 17) field description to read as follows:

“Clear all statistics counters and carry registers.

0 Allow MIB counters to continue to increment and keep any overflow indicators.

1 Reset all MIB counters and CAR1 and CAR2.

This bit is self-resetting.”

15.5.3.1.6, 15-32 In Table 15-10, “ECNTRL Field Descriptions,” update GMIIM bit definition to read as follows:

“GMII interface mode. If this bit is set, a PHY with a GMII interface is expected to be connected. If cleared, a PHY with an MII or RMII or RGMII interface is expected. The user should then set MACCFG2[I/F Mode] accordingly. The state of this status bit is defined during power-on reset. See Section 4.4.3, “Power-On Reset Configuration.”

0 MII or RMII or RGMII mode interface expected

1 GMII mode interface expected”

15.5.3.1.6, 15-33 In Table 15-11, “eTSEC Interface Configurations,” update GMIMM and add footnotes, as follows:

Table 15-11. eTSEC Interface Configurations

Interface Mode	ECNTRL Field							MACCFG2 Field
	FIFM	GMIIM	TBIM[1]	RPM	R100M	RMM	SGMIIM	I/F Mode
FIFO 8-bits	1	0	0	1	0	0	0	—
FIFO 16-bits	1	0	0	0	0	0	0	—
TBI 1Gbps	0	0	1	0	0	0	0	10
RTBI 1Gbps	0	0	1	1	0	0	0	10
GMII 1Gbps[2]	0	1	0	0	0	0	0	10
RGMII 1Gbps	0	1	0	1	0	0	0	10
RGMII 100 Mbps	0	1	0	1	1	0	0	01
RGMII 10 Mbps	0	1	0	1	0	0	0	01
MII 10/100 Mbps	0	0	0	0	0	0	0	01
TMII 200 Mbps	0	0	0	0	0	0	0	01
RMII 100 Mbps	0	0	0	0	1	1	0	01
RMII 10 Mbps	0	0	0	0	0	1	0	01
SGMII 1 Gbps	0	0	1	0	0	0	1	10
SGMII 100 Mbps	0	0	1	0	1	0	1	01
SGMII 10 Mbps	0	0	1	0	0	0	1	01

[1] TBIM bit not supported in this product.
[2] See MII 10/100 Mbps mode for GMII 10/100 Mbps ‘fall-back’ mode.

15.5.3.1.8, 15-34 — In Table 15-13, “DMACTRL Field Descriptions,” change TOD field definition, as follows:

“1 eTSEC immediately fetches a new TxBD from ring 0.”

15.5.3.2.1, 15-37 — In Table 15-15, “TCTRL Field Description,” change TXSCHED field description for 01 state to read as follows: “01 Priority scheduling mode. Frames from enabled TxBD rings are serviced in ascending ring index order.”

15.5.3.3.5, 15-55 — Modify second paragraph of the RBIFX register description, as follows:

“Figure 15-26 describes the definition for the RBIFX register. Note: when the eTSEC is configured to receive frame through the FIFO packet interface, a value of B*n*CTL = 01 is not supported unless RCTRL[PRSFM]=1 and RCTRL[PRSDEP] is configured to parse L2 packets over the FIFO interface. Below is a list of arbitrary extraction requirements:

- Byte extraction level cannot exceed the parser depth: a value of B*n*CTL=10 requires RCTRL[PRSDEP]=1x and a value of B*n*CTL=11 requires RCTRL[PRSDEP]=11.
- For B*n*CTL = 01, B*n*OFFSET = 7 is not supported.
- For values of B*n*CTL=10 or B*n*CTL=11, the controller extracts the defined bytes even if it does not recognize the L3 or L4 header, respectively.
- No L4 extraction is done if a packet is an IPV4 or IPV6 fragment frame.
- If no extraction occurs due to B*n*OFFSET longer than frame data or it is an unsupported B*n*OFFSET, the B*n* extraction values are filled with zeros.”

15.5.3.3.5, 15-56 — In Table 15-30, “RBIFX Field Descriptions,” append the following sentence to the 01 encoding of the field descriptions for bit fields B0CTL (0–1), B1CTL (8–9), B2CTL (16–17), and B3CTL (24–25): “Values of B0OFFSET less than 8 are reserved in FIFO modes.”

In addition, change the definition of the 10 encoding of B*n*CTL as follows: “Byte 0 is located in the received frame at offset B0OFFSET bytes from the byte after the last byte of the layer 2 header.”

In addition, change the definition of the 11 encoding of B*n*CTL as follows: “Byte 0 is located in the received frame at offset B0OFFSET bytes from the byte after the last byte of the layer 3 header.”

15.5.3.3.6, 15-59 — In Figure 15-27, “Receive Queue Filer Table Address Register Definition,” change reset value from “All zeros” to “undefined.”

13.4.4.2, 13-61 — Add the following to the end of the section:

For proper signalling, the following guidelines must be followed while programming UPM RAM words:

- For UPM reads, program UTA and LAST in the same or consecutive RAM words.
- For UPM burst reads, program last UTA and LAST in the same or consecutive RAM words.
- For UPM writes, program UTA and LAST in the same RAM word.
- For UPM burst writes, program last UTA and LAST in the same RAM word.

15.5.3.5.1, 15-68 In Table 15-39, “MACCFG1 Field Descriptions,” add the following note to Tx_Flow and Rx_Flow: “**Note**: Should not be set when operating in Half-Duplex mode.”

15.5.3.5.1, 15-68 In Table 15-39, “MACCFG1 Field Descriptions,” add clarification to Rx Flow (bit 26) and Tx Flow (bit 27) field descriptions, as follows: “Must be 0 if MACCFG2[Full Duplex] = 0.”

15.5.3.5.2, 15-69 In Table 15-40, “MACCFG2 Field Descriptions,” append the following sentence to the PreAM RxEN = 1 field description: “If the preamble is less than 7 bytes, 0’s are prepended to pad it to 7 bytes.”

15.5.3.5.2, 15-70 In Table 15-40, “MACCFG2 Field Descriptions,” update the “Huge Frame” (bit 26) field description, as follows:

Table 15-40. MACCFG2 Field Descriptions

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>26</td><td>Huge Frame</td><td>Huge frame enable. This bit is cleared by default.
0 Limit the length of frames received to less than or equal to the maximum frame length value (MAXFRM[Maximum Frame]) and limit the length of frames transmitted to less than the maximum frame length.
See Section 15.6.7, “Buffer Descriptors,” for further details of buffer descriptor bit updating.
<table>
<tr><th>Frame type</th><th>Frame length</th><th>Packet truncation</th><th>Buffer descriptor updated</th></tr>
<tr><td>Receive or transmit</td><td>> maximum frame length</td><td>yes</td><td>yes</td></tr>
<tr><td>Receive</td><td>= maximum frame length</td><td>no</td><td>no</td></tr>
<tr><td>Transmit</td><td>= maximum frame length</td><td>no</td><td>yes</td></tr>
<tr><td>Receive or transmit</td><td>< maximum frame length</td><td>no</td><td>no</td></tr>
</table>
1 Frames are transmitted and received regardless of their relationship to the maximum frame length. Note that if Huge Frame is cleared, the user must ensure that adequate buffer space is allocated for received frames. See Section 15.5.3.5.5, “Maximum Frame Length Register (MAXFRM),” for further information.</td></tr>
</table>

15.5.3.5.4, 15-72 In Figure 15-39, “Half-Duplex Register Definition,” and Table 15-42, “HAFDUP Field Descriptions,” change “Collision window” field size from 22–31 to 26–31. The reserved field is now 20–25.

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15.5.3.5.5, 15-73	In Table 15-43, “MAXFRM Descriptions,” modify the first paragraph of “Maximum Frame” (bits 16–31) field description, as follows: “This field is set to 0x0600 (1536 bytes) by default and always must be set to a value greater than or equal to 0x0040 (64 bytes), but not greater than 0x2580 (9600 bytes).It sets the maximum Ethernet frame size in both the transmit and receive directions. (Refer to MACCFG2[Huge Frame].) It does not affect the size of packets sent or received via the FIFO packet interface.
15.5.3.5.9, 15-75	Make Figure 15-44, “MII Mgmt Control Register Definition,” write only, as follows:

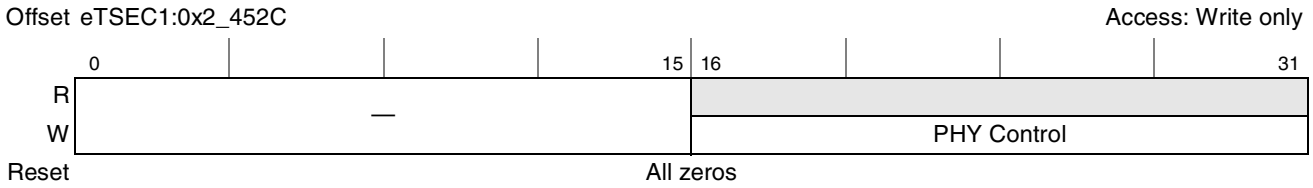

Figure 15-44. MII Mgmt Control Register Definition

15.5.3.6, 15-80	Add the following note before the TR64 register:

NOTE

The transmit and receive frame counters (TR64, TR127, TR 255, TR511, TR1K, TRMAX, and TRMGV) do not increment for aborted frames (collision retry limit exceeded, late collision, underrun, EBERR, TxFIFO data error, frame truncated due to exceeding MAXFRM, or excessive deferral).

15.5.3.6.25, 15-92	In Table 15-79, “TBYT Field Descriptions,” modify TBYT field description by changing second sentence from: “This count does not include preamble/SFD or jam bytes” to: “This count does not include preamble/SFD or jam bytes, except for half-duplex flow control (back-pressure triggered by TCTRL[THDF]=1). For THDF, the sum total of ‘phantom’ preamble bytes transmitted for flow control purposes is included in the TBYT increment value of the next frame to be transmitted, up to 65,535 bytes of frame and phantom preamble.”
15.5.3.6.41, 15-100	In Table 15-95, “TOVR Field Descriptions,” update field description to read as follows: “Transmit oversize frame counter. Increments each time a frame is transmitted which exceeds 1518 (non VLAN) or 11522 (VLAN) with a correct FCS value.”
15.5.3.6.44, 15-102	In Figure 15-95, “Carry Register 1 (CAR1) Register Definition,” change access from Read only to w1c.
15.5.3.6.45, 15-103	In Figure 15-96, “Carry Register 2 (CAR2) Register Definition,” change access from Read only to w1c.
15.5.3.9.2, 15-112	In Table 15-107, “ATTRELI Field Descriptions,” replace EI (bits 18–25) field description with the following: “Extracted index. Points to the first byte, as a

	multiple of 64 bytes, within the receive frame as sent to memory from which to begin extracting data.”
15.5.3.10.2, 15-114	In Figure 15-106, “RFBPTR0–RFBPTR7 Register Definition,” change offset to: “eTSEC1:0x2_4C44+8×*n*; eTSEC2:0x2_5C44+8×*n*”
15.6.2, 15-138	Replace first bullet under “The following restrictions apply in any of the FIFO modes” with the following: • Transferred packets must by no more than 9600 bytes in length. • If RCTRL[PRSFM]=0, received packets must be a minimum of 10 bytes. If RCTRL[PRSFM]=1, received packets must be a minimum of 14 bytes. • Transmitted packets with L2 headers must be a minimum of 14 bytes. Transmitted packets without L2 headers must be a minimum of 10 bytes.
15.6.2.1, 19-138	Update second sentence of third paragraph to say, “The controller completes any frame in progress before stopping transmission and does not commence counting the pause time until transmit is idle.”
15.6.5.3.1, 15-172	Replace Section 15.6.5.3.1, “Priority-Based Queuing (PBQ),” with the following:

“PBQ is the simplest scheduler decision policy. The enabled TxBD rings are assigned a priority value based on their index. Rings with a lower index have precedence over rings with higher indices, with priority assessed on a frame-by-frame basis. For example, frames in TxBD ring 0 have higher priority than frames in TxBD ring 1, and frames in TxBD ring 1 have higher priority than frames in TxBD ring 2, and so on.

The scheduling decision is then achieved as follows:

```
loop
      # start or S/W clear of TSATn
      ring = 0;
      while ring <= 7 loop
       if enabled(ring) and not ring_empty(ring) then
              transmit_frame(ring);
              ring = 0;
       else
              ring = ring + 1;
       endif
      endloop
endloop
```

15.7.1.7, 15-208 In Table 15-167, “8-Bit FIFO Interface Mode Signal Configurations, eTSEC1/2,” remove support for 3.3-V FIFO interface and change title, as follows:

Table 15-167. 8-Bit FIFO Interface Mode Signal Configurations

eTSEC Signals			8-Bit FIFO Interface Frequency [MHz] 155 Voltage [V] 2.5		
Signals	**I/O**	**No. of Signals**	**Signals**	**I/O**	**No. of Signals**
TSEC*n*_GTX_CLK	O	1	FIFO*n*_GTX_CLK	O	1
TSEC*n*_TX_CLK	I	1	FIFO*n*_TX_CLK	I	1
TSEC*n*_TxD[0]	O	1	FIFO*n*_TxD[0]	O	1
TSEC*n*_TxD[1]	O	1	FIFO*n*_TxD[1]	O	1
TSEC*n*_TxD[2]	O	1	FIFO*n*_TxD[2]	O	1
TSEC*n*_TxD[3]	O	1	FIFO*n*_TxD[3]	O	1
TSEC*n*_TxD[4]	O	1	FIFO*n*_TxD[4]	O	1
TSEC*n*_TxD[5]	O	1	FIFO*n*_TxD[5]	O	1
TSEC*n*_TxD[6]	O	1	FIFO*n*_TxD[6]	O	1
TSEC*n*_TxD[7]	O	1	FIFO*n*_TxD[7]	O	1
TSEC*n*_TX_EN	O	1	FIFO*n*_TX_EN	O	1
TSEC*n*_TX_ER	O	1	FIFO*n*_TX_ER	O	1
TSEC*n*_RX_CLK	I	1	FIFO*n*_RX_CLK	I	1
TSEC*n*_RxD[0]	I	1	FIFO*n*_RxD[0]	I	1
TSEC*n*_RxD[1]	I	1	FIFO*n*_RxD[1]	I	1
TSEC*n*_RxD[2]	I	1	FIFO*n*_RxD[2]	I	1
TSEC*n*_RxD[3]	I	1	FIFO*n*_RxD[3]	I	1
TSEC*n*_RxD[4]	I	1	FIFO*n*_RxD[4]	I	1
TSEC*n*_RxD[5]	I	1	FIFO*n*_RxD[5]	I	1
TSEC*n*_RxD[6]	I	1	FIFO*n*_RxD[6]	I	1
TSEC*n*_RxD[7]	I	1	FIFO*n*_RxD[7]	I	1
TSEC*n*_RX_DV	I	1	FIFO*n*_RX_DV	I	1
TSEC*n*_RX_ER	I	1	FIFO*n*_RX_ER	I	1
TSEC*n*_COL	I	1	FIFO*n*_TX_FC	I	1
TSEC*n*_CRS	I/O	1	FIFO*n*_RX_FC	O	1
MDIO	I/O	1	leave unconnected		
MDC	O	1	leave unconnected		
Sum		27	**Sum**		25

15.7.1.8, 15-210 In Table 15-169, “16-Bit FIFO Interface Mode Signal Configurations (eTSECs1 and 2),” remove support for 3.3-V FIFO interface and change title, as follows:

Table 15-169. 16-Bit FIFO Interface Mode Signal Configuration (eTSECs 1 and 2)

eTSEC Signals			16-Bit FIFO Interface Frequency [MHz] 155 Voltage [V] 2.5		
Signals	**I/O**	**No. of Signals**	**Signals**	**I/O**	**No. of Signals**
TSEC1_GTX_CLK	O	1	FIFO1_GTX_CLK	O	1
TSEC1_TX_CLK	I	1	FIFO1_TX_CLK	I	1
TSEC1_TxD[0]	O	1	FIFO1_TxD[0]	O	1
TSEC1_TxD[1]	O	1	FIFO1_TxD[1]	O	1
TSEC1_TxD[2]	O	1	FIFO1_TxD[2]	O	1
TSEC1_TxD[3]	O	1	FIFO1_TxD[3]	O	1
TSEC1_TxD[4]	O	1	FIFO1_TxD[4]	O	1
TSEC1_TxD[5]	O	1	FIFO1_TxD[5]	O	1
TSEC1_TxD[6]	O	1	FIFO1_TxD[6]	O	1
TSEC1_TxD[7]	O	1	FIFO1_TxD[7]	O	1
TSEC1_TX_EN	O	1	FIFO1_TXC[0]	O	1
TSEC1_TX_ER	O	1	FIFO1_TXC[1]	O	1
TSEC1_RX_CLK	I	1	FIFO1_RX_CLK	I	1
TSEC1_RxD[0]	I	1	FIFO1_RxD[0]	I	1
TSEC1_RxD[1]	I	1	FIFO1_RxD[1]	I	1
TSEC1_RxD[2]	I	1	FIFO1_RxD[2]	I	1
TSEC1_RxD[3]	I	1	FIFO1_RxD[3]	I	1
TSEC1_RxD[4]	I	1	FIFO1_RxD[4]	I	1
TSEC1_RxD[5]	I	1	FIFO1_RxD[5]	I	1
TSEC1_RxD[6]	I	1	FIFO1_RxD[6]	I	1
TSEC1_RxD[7]	I	1	FIFO1_RxD[7]	I	1
TSEC1_RX_DV	I	1	FIFO1_RXC[0]	I	1
TSEC1_RX_ER	I	1	FIFO1_RXC[1]	I	1
TSEC1_COL	I	1	FIFO1_TX_FC	I	1
TSEC1_CRS	I/O	1	FIFO1_RX_FC	O	1
MDIO	I/O	1	leave unconnected		
MDC	O	1	leave unconnected		

Table 15-169. 16-Bit FIFO Interface Mode Signal Configuration (eTSECs 1 and 2) (continued)

eTSEC Signals			16-Bit FIFO Interface		
			Frequency [MHz] 155		
			Voltage [V] 2.5		
TSEC2_GTX_CLK	O	1	leave unconnected		
TSEC2_TX_CLK	I	1	not used		
TSEC2_TxD[0]	O	1	FIFO1_TxD[8]	O	1
TSEC2_TxD[1]	O	1	FIFO1_TxD[9]	O	1
TSEC2_TxD[2]	O	1	FIFO1_TxD[10]	O	1
TSEC2_TxD[3]	O	1	FIFO1_TxD[11]	O	1
TSEC2_TxD[4]	O	1	FIFO1_TxD[12]	O	1
TSEC2_TxD[5]	O	1	FIFO1_TxD[13]	O	1
TSEC2_TxD[6]	O	1	FIFO1_TxD[14]	O	1
TSEC2_TxD[7]	O	1	FIFO1_TxD[15]	O	1
TSEC2_TX_EN	O	1	FIFO1_TXC[2]	O	1
TSEC2_TX_ER	O	1	leave unconnected		
TSEC2_RX_CLK	I	1	not used		
TSEC2_RxD[0]	I	1	FIFO1_RxD[8]	I	1
TSEC2_RxD[1]	I	1	FIFO1_RxD[9]	I	1
TSEC2_RxD[2]	I	1	FIFO1_RxD[10]	I	1
TSEC2_RxD[3]	I	1	FIFO1_RxD[11]	I	1
TSEC2_RxD[4]	I	1	FIFO1_RxD[12]	I	1
TSEC2_RxD[5]	I	1	FIFO1_RxD[13]	I	1
TSEC2_RxD[6]	I	1	FIFO1_RxD[14]	I	1
TSEC2_RxD[7]	I	1	FIFO1_RxD[15]	I	1
TSEC2_RX_DV	I	1	FIFO1_RXC[2]	I	1
TSEC2_RX_ER	I	1	not used		
TSEC2_COL	I	1	not used		
TSEC2_CRS	I	1	not used		
Sum		52	**Sum**		43

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16.4.1.1.4, 16-31	Revise first sentence of step 1 to say, “Set MR*n*[CDSM/SWSM] and MR*n*[XFE] and clear MR*n*[CTM] to indicate extended chaining and single-write start mode.“
18.6.5.2, 18-44	In Figure 18-41, “Error/Port-Write Interrupt Status Register (EPWISR),” add the following sentence to the PINT (bit 0) field description: “This bit is also set for outbound doorbell packet response time-out (PRT) errors.”
18.6.5.7, 18-47	Change the sentence, “The value of this register should always be larger than the link time-out value (PLTOCCSR),” to the following: “The value of this register should always be larger than the link time-out value (PLTOCCSR). By default, this time-out value is disabled (all zeros).”
18.6.7.7, 18-59	Add the following sentence to the end of the first paragraph: “Note that the LCSBA1CSR register (See Section 18.6.1.11, “Local Configuration Space Base Address 1 Command and Status Register (LCSBA1CSR)”) has priority over all ATMU windows if both are configured for the same address space.”
18.7.4.3, 18-86	In Table 18-92, “IDQDPAR Field Descriptions,” and Table 18-91, “EIDQDPAR Field Descriptions,” add the following note to the field descriptions of DQEPA and DQDPA: “Note that this base address must be queue-size aligned.”
18.10.2.1, 18-170	Modify the subsections of Section 18.10.2.1, “Outbound Doorbell Controller,” as follows:

18.10.2.1.1 Interrupts

The “SRIO outbound doorbell” controller interrupt is generated after the completion of a doorbell (done, error, packet response time-out or retry limit exceeded) if this interrupt event is enabled (ODDATR[EODIE] is a 1). The event that caused this interrupt is indicated by ODSR[EODI]. The interrupt is held until the ODSR[EODI] bit has been cleared by writing a 1.

The “SRIO error/port-write” interrupt can be generated for the following reasons:

- RapidIO error response. An interrupt is generated after a RapidIO error response is received and this interrupt event is enabled (LTLEECSR[MER])
- Packet response time-out. An interrupt is generated after a packet response time-out occurs and this interrupt event is enabled (LTLEECSR[PRT])
- Retry error threshold exceeded. An interrupt is generated after a retry threshold exceeded error occurs and this interrupt event is enabled (LTLEECSR[RETE])

18.10.2.1.2 Error Response Errors

When a RapidIO error response is received by the doorbell controller the following occurs:

- The doorbell controller sets the message error response status bits (ODSR[MER]and LTLEDCSR[MER])
- If LTLEECSR[MER] is set, the interrupt “SRIO error/port-write” is generated.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

18.10.2.1.3 Packet Response Time-Out Errors

When a packet response time-out occurs for a doorbell the following occurs:

- The doorbell controller sets the packet response time-out status bits (ODSR[PRT]and LTLEDCSR[PRT])
- If LTLEECSR[PRT] is set, the interrupt “SRIO error/port-write” is generated and EPWISR[PINT] is set.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

18.10.2.1.4 Retry Error Threshold Exceeded Errors

When a retry error threshold exceeded error occurs for a doorbell the following occurs:

- The doorbell controller sets the retry threshold exceed status bits (ODSR[RETE] and LTLEDCSR[RETE])
- If LTLEECSR[RETE] is set, the interrupt “SRIO error/port-write” is generated.
- After the doorbell operation completes (indicated by ODSR[DUB]) the doorbell controller stops.

18.10.2.1.5 Error Handling

When an error occurs and the “SRIO error/port-write” interrupt is generated, the following occurs:

- Software determines the cause of the interrupt and processes the error
  - LTLEDCSR and ODSR capture the error condition for outbound doorbells
  - EPWISR[PINT] is set for PRT error since it is detected by the SRIO controller
  - Note that LTLEDCSR is a capture once register, so ODSR should be examined to make sure an outbound doorbell error did not occur immediately after another captured error
- Software verifies the doorbell controller has stopped operation by polling ODSR[DUB]
- Software disables the doorbell controller by clearing ODMR[DUS]
- Software clears the error by writing a 1 to the corresponding outbound doorbell status bits (ODSR[PRT], ODSR[PRT], and/or ODSR[RETE] as well as LTLEDCSR)

When an error occurs and the “SRIO error/port-write” interrupt is not enabled, the following occurs:

- Software determines that an error has occurred by polling the status bits (ODSR[MER], ODSR[PRT], and/or ODSR[RETE])
- Software verifies the doorbell controller has stopped operation by polling ODSR[DUB]
- Software disables the doorbell controller by clearing ODMR[DUS]
- Software clears the error by writing a 1 to the corresponding status bits (ODSR[MER], ODSR[PRT], and/or ODSR[RETE])

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18.8.12.1, 18-104	Modify third paragraph, as follows: “The RapidIO controller detects two fatal errors: exceeded failed threshold and exceeded consecutive retry threshold. In these cases, the port has failed because its recoverable error rate has exceeded a predefined failed threshold or because it has received too many packet retries in a row. In the first case, the controller sets the output failed-encountered bit in the error and status CSR; the RapidIO output hardware may or may not stop (based on stop-on-port-failed-encounter-enable and drop-packet-enable bits). In the second case, the controller sets the retry counter threshold trigger exceeded bit in the implementation error CSR; the RapidIO hardware continues to operate. In both cases, an interrupt is generated, and while the port continues operating at least partially, a system-level fix (such as reset) is recommended to clean up the controller’s internal queues and resume normal operation. Fatal errors are detected in the physical layer only.”
19.2, 19-5	Replace sentence beginning with “For the MPC8568 the link may be either x4 or x8, depending on...” with “The PCI Express controller can be configured for a maximum link width of either ×4 or ×8 depending on the cfg_io_ports[0:2] sampled at reset.”
19.3.7.1.1, 19-43	In last bullet, add the statement that, “In this case [no bus number matches], PEX_ERR_DR[ICCA] is set.”
19.3.7.2, 19-44	Add statement that the PCI Express Controller Internal CSR registers are not accessible by inbound PCI Express configuration transactions.
19.3.10.5, 19-85	In Figure 19-106, “PCI Express Correctable Error Status Register,” change the Access from “Read/Write” to “w1c.”
19.4.1.8, 19-102	Revise first paragraph by removing, “originating from the PCI Express outbound ATMUs,” from the first sentence. In addition, remove the following sentence: “Note that configuration writes originating from the PCI Express configuration access registers (PEX_CONFIG_ADDR/PEX_CONFIG_DATA) are not serialized.”
20.4.6.9.1, 20-77	Modify the bullets, as follows: • IV1 holds the *most* significant bytes of the initialization vector (bytes 1–8). • IV2 holds the *least* significant bytes of the initialization vector (bytes 9–16).
20.4.6.9.2, 20-77	In last sentence, change “register 3” to “register 7.”

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21.4, 21-6 In Table 21-3, “Global Utilities Block Register Summary,” add SRDSCR0 and SRDSCR1 after CLKOCR, as follows:

Table 21-3. Global Utilities Block Register Summary

Offset	Register	Access	Reset	Section/Page
Debug Control				
0xE_0E00	CLKOCR—Clock out control register	R/W	All zeros	21.4.1.28/21-31
0xE_0F04	SRDSCR0—SerDes control register 0	R/W	*nn*00_*nn*00	21.4.1.29/21-32
0xE_0F08	SRDSCR1—SerDes control register 1	R/W	All zeros	21.4.1.30/21-33

21.4, 21-6 In Table 21-3, “Global Utilities Block Register Summary,” add the CEIMXCR*n* registers, as follows:

Table 21-3. Global Utilities Block Register Summary

Offset	Register	Access	Reset	Section/Page
QUICC Engine Block Interrupt Muxing Registers				
0xE_0200	CEIMXCR0—CE Interrupt multiplexing control register 0	R/W	All zeros	21.4.1.24/21-29
0xE_0204	CEIMXCR1—CE Interrupt multiplexing control register 1	R/W	All zeros	21.4.1.25/21-30
0xE_0208	CEIMXCR2—CE Interrupt multiplexing control register 2	R/W	All zeros	21.4.1.26/21-30
0xE_020C	CEIMXCR3—CE Interrupt multiplexing control register 3	R/W	All zeros	21.4.1.27/21-31

21.4.1.24, 21-29 Add Section 21.4.1.24, “CE Interrupt Mux Control Register 0–3 (CEIMXCR0–CEIMXCR3),” as follows:

21.4.1.24 CE Interrupt Mux Control Register 0–3 (CEIMXCR0–CEIMXCR3)

This register programs the routing of the interrupt signals from hardware accelerators in the MPC8569E to the QUICC Engine EXT[1..4] SNUMs. Refer to External Hardware Request section of the RISC Control chapter in the *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Interrupt signal connections can be routed either to the programmable interrupt controller (PIC) or to the QUICC Engine. By routing to the QUICC Engine, this allows it to handle the interrupts, and thus freeing up the CPU. Please contact Freescale for the availability of microcode packages taking advantage of this feature. Please note that the interrupt to the host CPU should be masked consistently with the programming of this register.

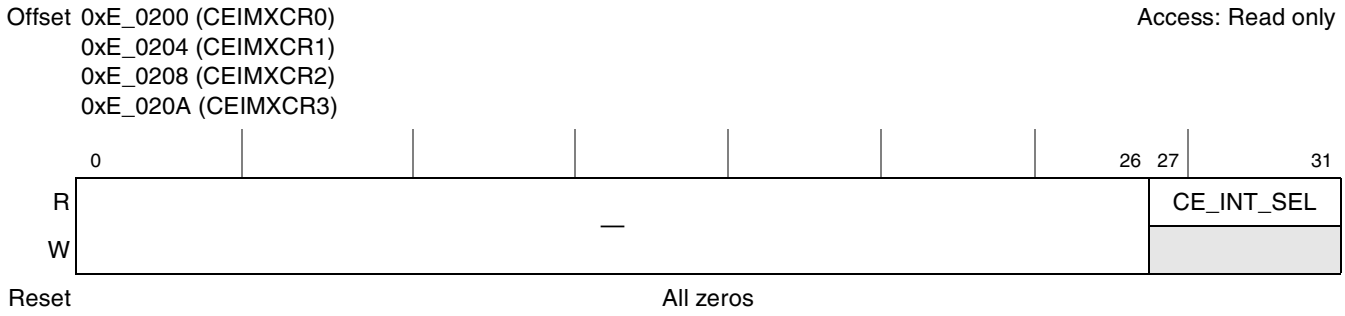

Figure 21-26. CE Interrupt Mux Control Register 0–3 (CEIMXCR0–CEIMXCR3)

Table 21-27. CEIMXCR0–CEIMXCR3 Field Descriptions

Bits	Name	Description
0–26	—	Reserved
27–31	CE_INT_SEL[0–3]	QUICC Engine interrupt selection. 00000 EXTx 00001 Security_2 00010 SRIO 1 & 2 E/PW 00011 SRIO inb message 1 00100 SRIO outb message 1 00101 Reserved 00110 Security_1 00111 Reserved 01000 Reserved 01001 Reserved 01010 SRIO inbound doorbell 01011 SRIO outbound doorbell 01100 SRIO inb message 0 01101 SRIO outb message 0 01110 Reserved 01111 Reserved 10000 Reserved

21.4.1.25 DDR Calibration Status Register (DDRCSR)

Shown in Figure 21-27, the DDRCSR contains debug status bits from the DDR SDRAM controller.

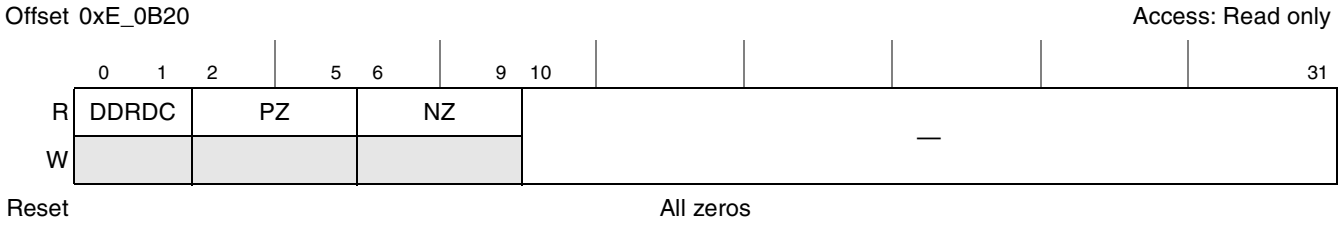

Figure 21-27. DDR Calibration Status Register (DDRCSR)

Table 21-28 describes the bit settings of DDRCSR.

Table 21-28. DDRCSR Field Descriptions

Bits	Name	Description
0–1	DDRDC	DDR driver compensation input value. This field reflects the current state of the MDIC[0:1] driver impedance calibration signals.
2–5	PZ	Current setting of PFET driver impedance (Field values not defined below are reserved.) 0000 Highest impedance; half strength 1000 Higher impedance 1100 Nominal impedance 1110 Lower impedance 1111 Lowest impedance; double strength
6–9	NZ	Current setting of NFET driver impedance (Field values not defined below are reserved.) 0000 Highest impedance; half strength 1000 Higher impedance 1100 Nominal impedance 1110 Lower impedance 1111 Lowest impedance; double strength
10–31	—	Reserved

21.4.1.26 DDR Control Driver Register (DDRCDR)

Shown in Figure 21-28, the DDRCDR contains bits that allow control over the I/O drivers of the DDR SDRAM controller.

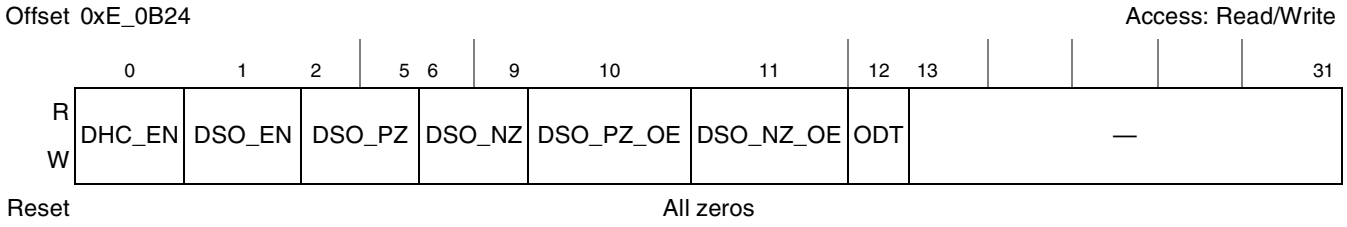

Figure 21-28. DDR Control Driver Register (DDRCDR)

Table 21-29 describes the bit settings of DDRCDR.

Table 21-29. DDRCDR Field Descriptions

Bits	Name	Description
0	DHC_EN	DDR driver hardware compensation enable
1	DSO_EN	DDR driver software override enable
2–5	DSO_PZ	DDR driver software p-impedance override
6–9	DSO_NZ	DDR driver software n-impedance override
10	DSO_PZ_OE	DDR driver software p-impedance OE
11	DSO_NZ_OE	DDR driver software n-impedance OE
12	ODT	ODT termination value for IOs 0 ODT termination of 75 ohms 1 ODT termination of 150 ohms
13–31	—	Reserved

21.4.1.27 DDR Clock Disable Register (DDRCLKDR)

Shown in Figure 21-29, the DDRCLKDR contains bits that allow disabling the clocks of the DDR SDRAM controller.

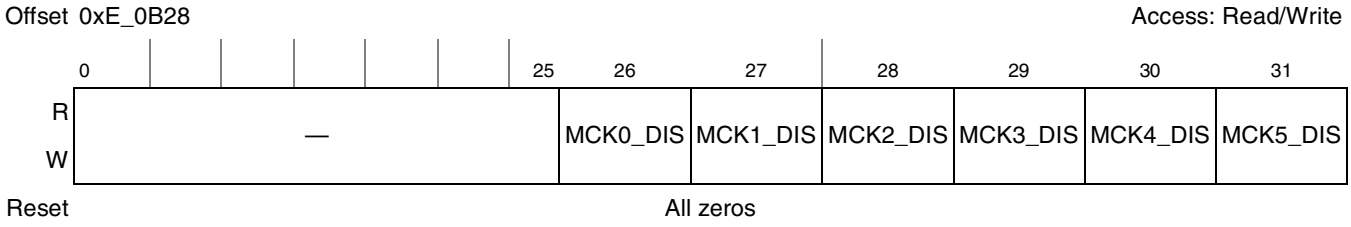

Figure 21-29. DDR Clock Disable Register (DDRCLKDR)

Table 21-30 describes the bit settings of DDRCLKDR.

Table 21-30. DDRCLKDR Field Descriptions

Bits	Name	Description
0–25	—	Reserved
26	MCK0_DIS	DDR clock 0 disable 0 MCK0 is enabled. 1 MCK0 is disabled.
27	MCK1_DIS	DDR clock 1 disable 0 MCK1 is enabled. 1 MCK1 is disabled.
28	MCK2_DIS	DDR clock 2 disable 0 MCK2 is enabled. 1 MCK2 is disabled.

Table 21-30. DDRCLKDR Field Descriptions (continued)

Bits	Name	Description
29	MCK3_DIS	DDR clock 3 disable 0 MCK3 is enabled. 1 MCK3 is disabled.
30	MCK4_DIS	DDR clock 4 disable 0 MCK4 is enabled. 1 MCK4 is disabled.
31	MCK5_DIS	DDR clock 5 disable 0 MCK5 is enabled. 1 MCK5 is disabled.

21.4.1.28 Clock Out Control Register (CLKOCR)

Shown in Figure 21-30, the CLKOCR contains control bits that select the clock sources to be placed on the clock out (CLK_OUT) signal.

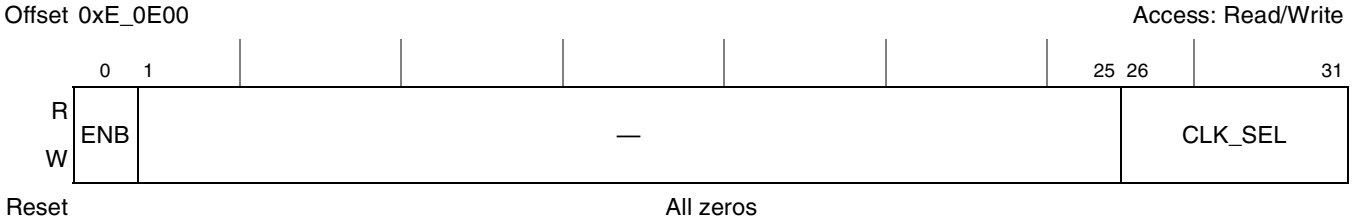

Figure 21-30. Clock Out Control Register (CLKOCR)

Table 21-31 describes the bit settings of CLKOCR.

Table 21-31. CLKOCR Field Descriptions

Bits	Name	Description
0	ENB	Clock out enable 0 CLK_OUT signal is three-stated 1 CLK_OUT signal is driven according to CLKOCR[CLK_SEL]
1–25	—	Reserved

Table 21-31. CLKOCR Field Descriptions (continued)

Bits	Name	Description
26–31	CLK_SEL	Clock out select 000000 CCB (platform) clock 000001 CCB (platform) clock divided by 2 000010 SYSCLK (echoes SYSCLK input) 000011 SYSCLK divided by 2 (demonstrates platform PLL lock) 000100 Reserved 000101 Reserved 000110 Reserved 000111 Reserved 001000 Reserved 001001 Reserved 001010 Reserved 001011 Reserved 001100 Reserved 001101 Reserved 001110 Reserved 001111 Reserved 01xx0x Reserved 01xx1x QUICC Engine Block clock 10x000 Reserved 10x001 Reserved 10x010 PCI bus clock 10x011 PCI bus clock divided by 2 10x100 Reserved 10x101 Reserved 10x110 Reserved 10x111 Reserved 11x000 Reserved 11x001 Reserved 11x010 Reserved 11x011 Reserved 11x100 Reserved 11x101 Reserved 11x110 Reserved 11x111 Reserved

21.4.1.27, 21-32 In Table 21-30, “CLKOCR Field Descriptions,” remove “Logic 0,” and “Logic 1,” from the CLK_SEL (bits 26–31) field description.

21.4.1, 21-32 Add Section 21.4.29, “SerDes Control Register 0 (SRDSCR0),” as follows:

21.4.1.29 SerDes Control Register 0 (SRDSCR0)

Shown in Figure 21-31, the SRDSCR0 contains control bits for the SerDes high-speed interface port.

Offset 0xE_0F04 Access: Read/Write

	0															15	16			19	20			23	24							31
R W	—																XMITEQ03				XMITEQ47				—							
Reset	*n*	*n*	*n*	*n*	*n*	*n*	*n*	*n*	0	0	0	0	0	0	0	0	*n*	*n*	*n*	*n*	*n*	*n*	*n*	*n*	0	0	0	0	0	0	0	0

Figure 21-31. SerDes Control Register 0 (SRDSCR0)

Table 21-32 describes the fields of SRDSCR0.

Table 21-32. SRDSCR0 Field Descriptions

Bits	Name	Description
0–15	—	Reserved
16–19	XMITEQ03	Transmit equalization selection bus for lanes 0-3 Default value: 1100 PCI Express Bit 16 is amplitude select: 0 5/6 Vdd-diff-pk=pk 1 Vdd-diff-pk=pk Bits 17–19 are equalization amplitude: 000 No equalization 001 1.09x relative amplitude 010 1.2x relative amplitude 011 1.33x relative amplitude 100 1.5x relative amplitude 101 1.71x relative amplitude 110 2.0x relative amplitude
20–23	XMITEQ47	Transmit equalization selection bus for lanes 4-7 Default value: 1100 PCI Express 1011 Serial RapidIO Bit 20 is amplitude select: 0 5/6 Vdd-diff-pk=pk 1 Vdd-diff-pk=pk Bits 21–23 are equalization amplitude: 000 No equalization 001 1.09x relative amplitude 010 1.2x relative amplitude 011 1.33x relative amplitude 100 1.5x relative amplitude 101 1.71x relative amplitude 110 2.0x relative amplitude
24–31	—	Reserved

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21.4.1, 21-33 Add Section 21.4.30, “SerDes Control Register 1 (SRDSCR1),” as follows:

21.4.1.30 SerDes Control Register 1 (SRDSCR1)

Shown in Figure 21-32, the SRDSCR1 contains the control bits for SerDes high-speed interface port.

Offset 0xE_0F08 Access: Read/Write

	0	1	2	3	4	5	6	7	8	20	21	24	25	31
R W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	—		LBSELTYPE		—	
Reset	All zeros													

Figure 21-32. SerDes Control Register 1 (SRDSCR1)

Table 21-33 describes the fields of SRDSCR1.

Table 21-33. SRDSCR1 Field Descriptions

Bits	Name	Description
0	PD0	Lane A power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
1	PD1	Lane B power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
2	PD2	Lane C power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
3	PD3	Lane Dpower down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
4	PD4	Lane E power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states
5	PD5	Lane F power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
6	PD6	Lane G power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.

Table 21-33. SRDSCR1 Field Descriptions (continued)

Bits	Name	Description
7	PD7	Lane H power down 0 Normal 1 The serial links are disabled (turn off) and power usage is minimized in all internal cells. Can be used for PEX L1/L1s states.
8–20	—	Reserved
21–24	LBSELTYPE	Select type loop-back 0000 Aplication mode 0001 Digital loopback mode 0010–1111 Reserved
25–31	—	Reserved

24.1, 24-1 Change SPI description in bulleted list to read: “Two serial peripheral controllers (SPI1 and SPI2). SPI2 can also be used for Ethernet PHY management.”

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