Freescale Semiconductor
Addendum

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Errata to the MPC8280 PowerQUICC II Family Reference Manual, Rev. 1

This errata document describes corrections to the *MPC8280 PowerQUICC II Family Reference Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items with section and page numbers in bold are new since the last revision of this document.

To locate any published updates for this document, refer to the website listed on the back cover of this document.

Section, Page No.	Changes
Throughout	Change all references to VCC power supply signal to VDDH.
2.4.2.3, 2-23	Replace information regarding AN1767 with AN2129, as follows: "*Instruction and Data Cache Locking on the e300 Processor Core* application note (order number: AN2129)."
4.3.1.4, 4-21	In Figure 4-14, change the lower bits at address 0x10C10 to be 0x10C0A.
4.3.2.1, 4-26	In Table 4-9, "BCR Field Descriptions," update the description for DAM so that the values read: 0 The memory controller asserts $\overline{CS}$ on the cycle following the assertion of $\overline{TS}$ when accessing an address space controlled by the memory controller. 1 The memory controller inserts one wait state between the assertion of $\overline{TS}$ and the assertion of $\overline{CS}$ when accessing an address space controlled by the memory controller.
4.3.1.1, 4-18	In Table 4-4, "SICR Field Descriptions," add the following sentence to the field description of HP (bits 2–7): "Port C interrupts have a fixed priority level and cannot be advanced to the highest priority level."
4.3.2.13, 4-43	In Figure 4-34, "Local Bus Transfer Error Status and Control Register 2 (L_TESCR2)," and Table 4-18, "L_TESCR2 Field Descriptions," change L_TESCR2[PB] bits to 8–11, instead of 12–15. Change bits 12–15 to "Reserved, should be cleared."
5.4, 5-8	Added the following sentence before the last sentence in the last paragraph: "Note that rstconf# should be asserted no later than 1007 CLKIN cycles after hreset# assertion."
5.4.1, 5-10	In Table 5-7, "Hard Reset Configuration Word Field Descriptions," for MODCK_H description, clarify that PCI_MODCK_H[0–3] pins are used.
9.6, 9-4	Changed the referenced default value of ALRH to 0x0126_7893.
9.11.1.6, 9-33	In Table 9-7, "PTCR Field Descriptions," for PTCR[PTV], clarify that the clock referred to is the CPM clock.
9.11.2.6, 9-50	In Table 9-25, "PCI Bus Programming Interface Register Description," change bit description to say, "0x00 When the PCI bridge is configured as a host; or, when the PCI bridge is configured as a peripheral device to indicate the programming model supports the I_2O interface."
9.11.2.8, 9-51	In Table 9-27, "PCI Bus Base Class Code Register Description," change bit description to say, "0x06 When the PCI bridge is configured as a host; or, when the PCI bridge is configured as a peripheral device to indicate the programming model supports the I_2O interface." In the note on I_2O compliancy, change the values of the interface, subclass code, and base class code registers to 0x00, 0x80, and 0x06 respectively.
10.4, 10-6	In Table 10-2, modify the description for bit 29, SCCR[CLPD], to read: 1 CPM and SIU enter low power mode when the core does.

Section, Page No.	Changes
11.1, 11-3	Remove the words “for single accesses” from the end of the bulleted item which reads “Read-modify-write (RMW) odd/even parity...”
11.2.4, 11-8	Add the following first paragraph: RMW parity mode is used when there is a special memory byte lane for parity with its own byte enable, and actual RMW transaction would occur only for sub-port size write transaction. Normal parity mode is used when each data byte lane is appended with a parity bit, using the same byte enable.
11.4.6.4, 11-41	Replaced the last sentence of the section with the following: The most efficient programming will be CL – 1, but in some cases this setting can violate t_{RAS} (activate to precharge) for a single beat read. If this happens, LDOTOPRE should be set to the minimum that meets t_{RAS}.
14.5, 14-19	In Figure 14-8, “Internal Data RAM Memory Map,” 0xs00 is not a valid offset value; change to 0x2000.
19.8.5, 19-25	In Table 20-6, “IDMA BD Field Descriptions,” revise the description for bit 15, DDTB, as follows: 01 The destination address lies within the local or PCI buses.
20.3.2, 20-15	In Table 20-6, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 Reserved. 01 PowerPC™ little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most-significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.
24.8, 24-7	In Table 24-5, change the third sentence in the Transmitter Underrun description to read as follows: Underrun in transparent mode occurs when the CPM or SDMA is experiencing a latency issue and cannot keep up with the transmission rate.
27.5.6, 27-16	In Table 27-8, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame.

00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

28.2.3.1, 28-8 In Table 28-3, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows:

Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame.

00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

29.9.2, 29-44 In Table 29-22, “TxBD Field Descriptions,” for bit 4, “L,” add the following note to the field description:

Note: In Transparent Mode operation, setting Last puts the channel to Idle state after sending the last byte of the buffer (or the CRC, if enabled). To resume transmit, set the POL bit in the CHAMR. For continuous transmission—for example, with no concept of a frame boundary—Last should NOT be set in Transparent Mode.31.10.2.3.2, 31-54In Table 31-23, change the second sentence of the field description for TCT[SN] to read “Used to generate the sequence number in the AAL1 PDU header.”

30.10.1.1, 30-17 Revise Section 30.10.1.1, “Re-Initialization Procedure,” as follows:

1. Disable the FCC transmission by clearing GFMR[ENT].
2. Remember the TxBD pointer range for data recovery (Every TxBD marked Ready contains data that has not been transmitted). Clear the Ready bit of the entire TxBD ring.

3. Issue an “INIT TX PARAMS” command using the CPCR.
4. Enable FCC transmission by setting GFMR[ENT] and poll TSTATE[8:31] until it is equal to 0x040000.
5. Issue a “Graceful Tx Stop” command using CPCR
6. Restore the Ready bit for all TxBDs marked for data recovery.
7. Modify TBPTR in PRAM to point to the TxBD to be transmitted next.
8. Issue a “Restart Tx” command using the CPCR.

30.10.1.3, 30-17	Remove section, “Adjusting Transmitter BD Handling.”
31.10.2.3, 31-54	In Table 31-23, Transmit Connection Table (TCT) bit 8 for AVCF Added the following sentence to the note on AVCF. "The AVCF bit m ust not be set for VBR.”
36.7, 36-8	Remove paragraph with references to FPSMR[ECM].
36.8, 36-12	In Table 36-2, “Ethernet-Specific Parameter RAM,” change the description for location 0xFC to read, “**Reserved and must be cleared**,” in bold font. For offset 0xFF, add “**POLL_DELAY**” as the offset name; the name should be in bold to indicate that the user needs to initialize.
36.19, 36-24	In Figure 36-9, “Fast Ethernet Receive Buffer (RxBD),” and Table 36-10, “RxBD Field Descriptions,” remove references to RxBD[CMR]. Bit 6 should be reserved.
38.3.1, 38-3	Modify the last paragraph, as follows: “The receiver synchronizes on the synchronization pattern located in the FDSR. For instance, if an 8-bit SYNC is selected, reception begins as soon as these eight bits are received, beginning with the first bit following the 8-bit SYNC. The value for FDSR should be 0x00*nn* if 8-bit SYNC is selected. This effectively links the transmitter synchronization to the receiver synchronization.”
39.5.1, 39-12	In Table 39-6, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory. 01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the

most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

40.5, 40-11 In Table 40-11, “RFCR/TFCR Field Descriptions,” modify the second encoding in GBL (bit 2) field description to be for “1,” not “0.”

40.5, 40-11 In Table 40-11, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows:

Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame.

00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

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