Freescale Semiconductor
Addendum

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Errata to the MPC8272 PowerQUICC II Family Reference Manual, Rev. 2

This errata document describes corrections to the *MPC8272 PowerQUICC II Family Reference Manual*, Revision 2. For convenience, the section number and page number of the errata item in the reference manual are provided. Items with section and page numbers in bold are new since the last revision of this document.

To locate any published updates for this document, see the website listed on the back cover of this document.

2.3.1.2.1, 2-13 — In Table 2-1, modify the description for bit 10, HID0[STOP], to read as follows:

1 Stop mode enabled. Sleep mode is invoked by setting MSR[POW] while this bit is set. The main MPC8272's PLL remains active and all the internal clocks–including the core's clock–stop.

2.3.1.2.4, 2-15 — Update section to "Software can identify the MPC8272's processor core by reading the processor version register (PVR). For the processor version number, refer to the PowerQUICC II Masks and Versions chart on the MPC8272 product summary page at the Freescale website."

2.4.2.3, 2-21 — Replace information regarding AN1767 with AN2129, as follows: "*Instruction and Data Cache Locking on the e300 Processor Core* application note (order number: AN2129)."

4.3.1.1, 4-18 — In Table 4-4, "SICR Field Descriptions," add the following sentence to the field description of HP (bits 2–7):

"Port C interrupts have a fixed priority level and cannot be advanced to the highest priority level."

4.3.1.4, 4-21 — In Figure 4-14, change the lower bits at address 0x10C10 to be 0x10C0A.6.1, 6-1 Add the following second paragraph to the note:

The OE control signal of the BADDR[27]/~IRQ1, BADDR[28]/ ~IRQ2, ~CI/BADDR29/~IRQ2, ~WT/BADDR30/~IRQ3, BADDR31/ ~IRQ5/~CINT, and ALE/~IRQ4 pins is at an unknown state for 16K clocks during HRESET. This will happen only during HRESET and will not effect the functional state of these pins or cause false interrupts.

5.4, 5-7 — Added the following sentence before the last sentence in the last paragraph: "Note that rstconf# should be asserted no later than 1007 CLKIN cycles after hreset# assertion."

5.4, 5-7 — In Table 5-6, updated "address" to "offset" as follows:

Table 5-6. Configuration EEPROM Offsets

Configured Device	Byte 0 Offset	Byte 1 Offset	Byte 2 Offset	Byte 3 Offset
Configuration master	0x00	0x08	0x10	0x18
First configuration slave	0x20	0x28	0x30	0x38
Second configuration slave	0x40	0x48	0x50	0x58
Third configuration slave	0x60	0x68	0x70	0x78
Fourth configuration slave	0x80	0x88	0x90	0x98
Fifth configuration slave	0xA0	0xA8	0xB0	0xB8
Sixth configuration slave	0xC0	0xC8	0xD0	0xD8
Seventh configuration slave	0xE0	0xE8	0xF0	0xF8

6.1, 6-1 — Add the following second paragraph to the note:

The OE control signal of the BADDR[27]/~IRQ1, BADDR[28]/ ~IRQ2, ~CI/BADDR29/~IRQ2, ~WT/BADDR30/~IRQ3, BADDR31/ ~IRQ5/~CINT, and ALE/~IRQ4 pins is at an unknown state for 16K clocks during HRESET. This will happen only during HRESET and will not effect the functional state of these pins or cause false interrupts.

Chapter 9, 9-2 Updated Figure 9-1, “PCI Bridge in the MPC8272,” as follows:

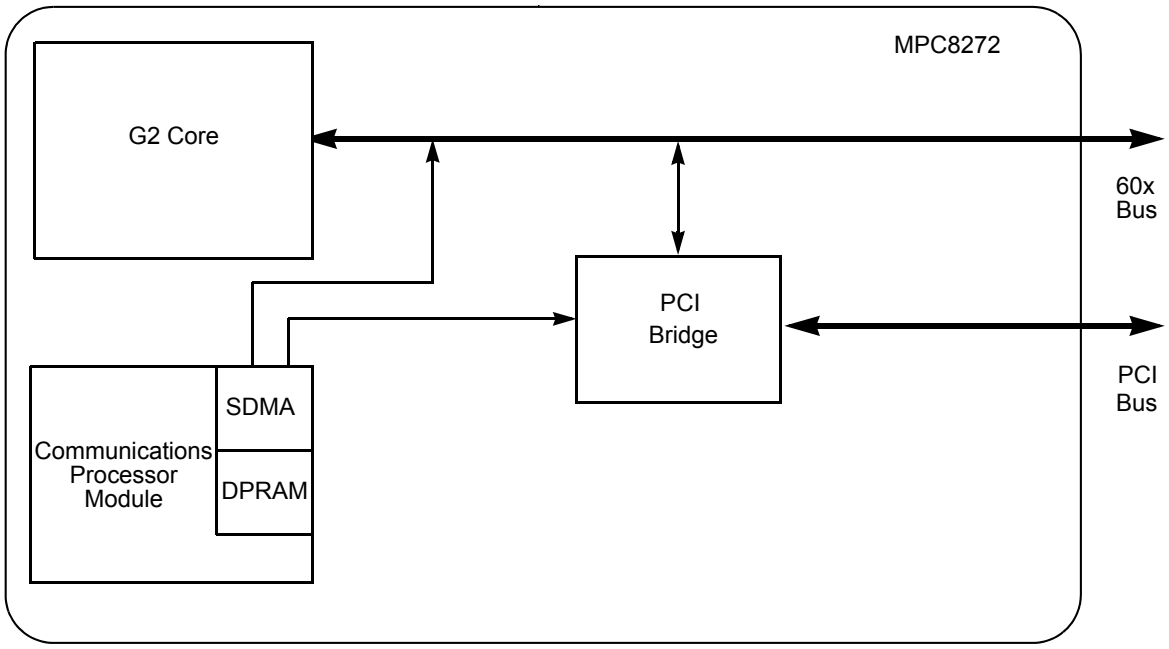

Figure 9-1. PCI Bridge in the MPC8272

9.6, 9-5 Changed the referenced default value of ALRH to 0x0126_7893.

9.11.1.6, 9-34 In Table 9-7, modify the second and third sentences of the description for bits 23–0, PTCR[Preload timer values], to clarify that the clock being referred to is the CPM clock:

Delayed PCI read transactions to a non-prefetchable address space remain valid within the PCI bridge a minimum of (2^{24} – Preload Timer Value) internal CPM clock cycles. The discard timer is used to discard delayed reads from non-prefetchable address space if the master has not repeated the transaction in *n* internal CPM clock cycles, where $n = (2^{24}$ – Preload Timer Value).

9.11.2.6, 9-51 In Table 9-25, “PCI Bus Programming Interface Register Description,” change bit description to say, “0x00 When the PCI bridge is configured as a host; or, when the PCI bridge is configured as a peripheral device to indicate the programming model supports the I_2O interface.”

9.11.2.8, 9-52 In Table 9-27, “PCI Bus Base Class Code Register Description,” change bit description to say, “0x06 When the PCI bridge is configured as a host; or, when the PCI bridge is configured as a peripheral device to indicate the programming model supports the I_2O interface."

In the note on I_2O compliancy, change the values of the interface, subclass code, and base class code registers to 0x00, 0x80, and 0x06 respectively.

10.4, 10-7 — In Table 10-2, modify the description for bit 29, SCCR[CLPD], to read:

1 CPM and SIU enter low power mode when the core does.

11.4.6.4, 11-34 — Replace the last sentence of the section with the following:
The most efficient programming will be CL – 1, but in some cases this setting can violate t_{RAS} (activate to precharge) for a single beat read. If this happens, LDOTOPRE should be set to the minimum that meets t_{RAS}.

11.4.12.1, 11-44 — Update Table 11-22, "Register Settings (Page-Based Interleaving)," as follows:

Table 11-22. Register Settings (Page-Based Interleaving)

Register	Settings	
BR*x*	[BA] = Base address [PS00] = 64-bit port size [WP] = 0 [MS010] = SDRAM-60x bus	[EMEMC] =0 [ATOM] = 00 [DR] = 0 [V] = 1
OR*x*	[AM] =1111_1100_0000 [LSDAM] =00000 [BPD] = 01 [ROWST] = 0110	[NUMR] =011 [PMSEL] =0 [IBID] = 0
PSDMR	[PBI] =1 [RFEN] =1 [OP] = 000 [SDAM] =011 [BSMA] =010 [SDA10] =011 [RFRC] = From device data sheet [PRETOACT] =From device data sheet	[ACTTOROW] = From device data sheet [BL] =0 [LDOTOPRE] = From device data sheet [WRC] = From device data sheet [EAMUX] =0 [BUFCMD] =0 [CL] = From device data sheet

11.4.13, 11-45 — Update Table 11-26, "Register Settings (Bank-Based Interleaving)," as follows:

Table 11-26. Register Settings (Bank-Based Interleaving)

Register	Settings	
BR*x*	[BA] = Base address [PS] = 00 (64-bit port size0 [WP] = 0 [MS]010 = SDRAM-60x bus	[EMEMC] =0 [ATOM] = 00 [DR] = 0 [V] = 1
OR*x*	[SDAM] = 111_1100_0000 [LSDAM] = 00000 [BPD] = 01 [ROWST] = 010	[NUMR] = 011 [PMSEL] =0 [IBID] =0

Table 11-26. Register Settings (Bank-Based Interleaving) (continued)

Register	Settings	
PSDMR	[PBI] = 0 [RFEN] =1 [OP] = 000 [SDAM] = 001 [BSMA] = 010 [SDA] = 10011 [RFRC] From device data sheet [PRETOACT] From device data sheet	[ACTTOROW]From device data sheet [BL] = 0 [LDOTOPRE]From device data sheet [WRC] From device data sheet [EAMUX] =0 [BUFCMD] =0 [CL] From device data sheet

11.5.3, 11-55 Update Table 11-30, "Boot Bank Field Values after Reset," as follows:

Table 11-30. Boot Bank Field Values after Reset

Register	Setting
BR0	BA From hard reset configuration word. See Section 5.4.1, "Hard Reset Configuration Word." PS From hard reset configuration word. See Section 5.4.1, "Hard Reset Configuration Word." WP 0 MS 000 EMEMC From hard reset configuration word. See Section 5.4.1, "Hard Reset Configuration Word." V 1
OR0	AM1111_1110_0000_0000_0 (32 Mbytes) BCTLD0 CSNT1 ACS11 SCY1111 SETA0 TRLX1 EHTR0

11.6.4.2, 11-70 Replace Table 11-35, "UPM Address Multiplexing" with the following tables:

This table shows UPM address multiplexing for A0:A15.

Table 11-35. UPM Address Multiplexing (A0:A15)

SDAM	External Bus Address Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15
000	Signal driven on external pins when address multiplexing is enabled	—	—	—	—	—	—	—	—	—	—	—	—	—	A5	A6	A7
001		—	—	—	—	—	—	—	—	—	—	—	—	—	—	A5	A6
010		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A5
011		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
100		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
101		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

This table shows UPM address multiplexing for A16:A31.

Table 11-36. UPM Address Multiplexing (A16:A31)

SDAM	External Bus Address Pins	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
000	Signal driven on external pins when address multiplexing is enabled	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23
001		A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22
010		A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21
011		A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
100		A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19
101		—	—	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18

11.6.5, 11-73 Update Table 11-38, “Register Settings,” as follows:

Table 11-38. Register Settings

Register	Settings	
BRx	BA msb of base address PS 00 = 64-bit port size WP0 MS 100 = UPMA	EMEMC 0 ATOM 00 DR 0 V 1
ORx	AM 1111_1111_0000_0000_0 = 16 Mbyte BI 0	EHTR 0
MxMR	BSEL 0 = 60x bus RFEN 1 OP 00 AM 001 DSA As needed G0CLA N/A	GPL_A4DIS 0 RLFA As needed WLFA As needed TLFA As needed MAD N/A

13.5.1, 13-17 Remove the following sentence from the NOTE: “Therefore, a system design should not plan to access the 60x bus simultaneously with DPRAM BD fetches.”

18.8.5, 18-24 In Table 18-10, “IDMA BD Field Descriptions,” revise the description for bit 15, DDTB, as follows:

01 The destination address lies within the PCI bus.

19.1.1, 19-9 In Table 19-2, “GMSR_L Field Descriptions,” revise the description for bits 28-31, MODE, as follows:

0011 Reserved
0101 Reserved

19.1.4, 19-10 In Table 19-3, “TODR Field Descriptions,” in TOD field description, change “TOD is cleared automatically after one serial clock...” to “TOD is cleared

	automatically after one system clock cycle, but transmitting on demand continues until an unprepared (R = 0) BD is reached.”
19.3.2, 19-15	In Table 19-6, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 Reserved. 01 PowerPC™ little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most-significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.
23.8, 23-7	In Table 23-5, change the third sentence in the Transmitter Underrun description to read as follows: Underrun in transparent mode occurs when the CPM or SDMA is experiencing a latency issue and cannot keep up with the transmission rate.
26.3.2.5, 26-5	Change all “16,384” to “8,192.” Change “4-byte pointers” to “8-byte pointers.” Change all “256” to “128.”
26.3.2.8, 26-9	In Table 26-1, mark the RX_FRM_Base and TX_FRM_Base parameters in boldface to show that they must be initialized by the user.
26.3.4.1, 26-16	In Table 26-4, mark the RPACK parameter in boldface to show that it must be initialized by the user.
26.3.4.2, 26-20	In Table 26-8, mark the RPACK parameter in boldface to show that it must be initialized by the user.
26.6.2, 26-38	In Table 26-15, “Transmit Buffer Descriptor (TxBD) Field Descriptions,” add the following to bit 4 “L” field description: **Note**: In Transparent Mode operation, setting Last puts the channel to Idle state after sending the last byte of the buffer (or the CRC, if enabled). To resume transmit, set the POL bit in the CHAMR. For continuous transmission—for example, with no concept of a frame boundary—Last should NOT be set in Transparent Mode.
27.5.6, 27-17	In Table 27-8, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a

buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

28.2.3.1, 28-8

In Table 28-3, "RFCR*x*/TFCR*x* Field Descriptions," revise the description for bits 3–4, RFCR/TFCR[BO], as follows:

Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame.

00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory.

01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

28.3.12, 28-19

Change step 1 to read, "Configure the port C pins to enable SMTXD1 and SMRXD1. Set PPARC[4,5] and PDIRC[5]. Clear PDIRC[4] and PSORC[4,5]."

29.10.1.1, 29-17

Revise Section 29.10.1.1, "Re-Initialization Procedure," as follows:

1. Disable the FCC transmission by clearing GFMR[ENT].
2. Remember the TxBD pointer range for data recovery (Every TxBD marked Ready contains data that has not been transmitted). Clear the Ready bit of the entire TxBD ring.
3. Issue an "INIT TX PARAMS" command using the CPCR.
4. Enable FCC transmission by setting GFMR[ENT] and poll TSTATE[8:31] until it is cleared.
5. Issue a "Graceful Tx Stop" command using CPCR
6. Restore the Ready bit for all TxBDs marked for data recovery.
7. Modify TBPTR in PRAM to point to the TxBD to be transmitted next.
8. Issue a "Restart Tx" command using the CPCR.

29.10.1.3, 29-17	Remove section, “Adjusting Transmitter BD Handling.”
30.10.2.3.2, 30-51	In Table 30-22, change the second sentence of the field description for TCT[SN] to read “Used to generate the sequence number in the AAL1 PDU header.”
32.7, 32-8	Remove paragraph with references to FPSMR[ECM].
32.8, 32-12	In Table 32-2, “Ethernet-Specific Parameter RAM,” change the description for location 0xFC to read, “**Reserved and must be cleared**,” in bold font. For offset 0xFF, add “**POLL_DELAY**” as the offset name; the name should be in bold to indicate that the user needs to initialize.
32.19, 32-25	In Figure 32-10, “Fast Ethernet Receive Buffer (RxBD),” and Table 32-11, “RxBD Field Descriptions,” remove references to RxBD[CMR]. Bit 6 should be reserved.
35.5.1, 35-12	In Table 35-6, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory. 01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double word contains data to be transmitted earlier than the most significant byte of the same buffer double word. 1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.
36.5, 36-10	In Table 36-7, “RFCR/TFCR Field Descriptions,” modify the second encoding in GBL (bit 2) field description to be for “1,” not “0.”
36.5, 36-11	In Table 36-7, “RFCR*x*/TFCR*x* Field Descriptions,” revise the description for bits 3–4, RFCR/TFCR[BO], as follows: Byte ordering. This bit field should be set by the user to select the required byte ordering for the data buffer. If this bit field is modified on the fly, it will take effect at the beginning of the next frame. 00 DEC (and Intel) convention is used for byte ordering—swapped operation. It is also called little-endian byte ordering. The transmission order of bytes within a buffer word is reversed as compared to the PowerPC mode. This mode is supported only for 32-bit port size memory. 01 PowerPC little-endian, or munged, byte ordering. As data is transmitted onto the serial line from the data buffer, the least significant byte of the buffer double

word contains data to be transmitted earlier than the most significant byte of the same buffer double word.

1X PowerPC byte ordering—normal operation. It is also called big-endian byte ordering. As data is transmitted onto the serial line from the data buffer, the most significant byte of the buffer word contains data to be transmitted earlier than the least significant byte of the same buffer word.

37.5, 37-19 Figure 37-22, “Primary and Secondary Option Programming,” replace with the following:

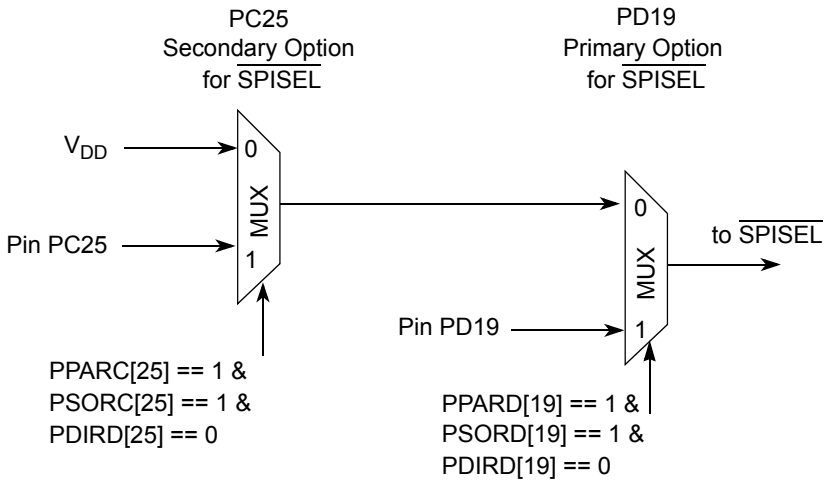

Figure 37-22. Primary and Secondary Programming

38.2, 38-9 Add the following caution note after the last paragraph:

CAUTION

It is important to set the PPC_ALRx registers so that the SEC has a slot in the bus arbitration scheme. Refer to Section 4.3.2.2, “60x Bus Arbiter Configuration Register (PPC_ACR),” and Section 4.3.2.3, “60x Bus Arbitration-Level Registers (PPC_ALRH/PPC_ALRL).”

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