

ALTIVECPEMAD/D  
(Motorola Order Number)

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REV. 0

# ***PowerPC***<sup>TM</sup>

## *Errata*

## **AltiVec<sup>TM</sup> Technology Programming Environments Manual Errata**

This errata describes corrections to the *AltiVec Technology Programming Environments Manual* (order #: ALTIVECPEM/D, rev. 0) referred to as the PEM. For convenience, the section number and page number are provided.

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Section #/Page #

Changes

2.1.2, Page 2-4 Replace Figure 2-4, “Saving/Restoring the AltiVec Context Register (VRSAVE)” with the following:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11	VR12	VR13	VR14	VR15
Reset	0000_0000_0000_0000															
R/W	R/W using <b>mfspr</b> or <b>mtspr</b> instructions															
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	VR16	VR17	VR18	VR19	VR20	VR21	VR22	VR23	VR24	VR25	VR26	VR27	VR28	VR29	VR30	VR31
Reset	0000_0000_0000_0000															
R/W	R/W using <b>mfspr</b> or <b>mtspr</b> instructions															
SPR	SPR256															

2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown.

4.2.2.4, Page 4-20 Change Table 4-9 as follows:

- the mnemonic for Vector Round to Floating-Point Integer Nearest should be **vrfin** not **fvrfin**.
- the mnemonic for Vector Round to Floating-Point Integer toward Zero should be **vrfiz**, not **fvrfiz**.
- the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be **vrfip**, not **fvrrip**.
- the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be **vrfim**, not **fvrifim**.

6.2, Page 6-24 Change the **mfvsr** encoding as shown below (note: bit 31 is not 0):

04	vD	00000	00000	1540
0	5 6	10 11	15 16	20 21
				31

6.2, Page 6-25 Change the **mtvsr** encoding as shown below (note: bit 31 is not 0):

04	00000	00000	vB	1604
0	5 6	10 11	15 16	20 21
				31

A.1, Page A-2 Change the **mfvsr** encoding as shown below (note: bit 31 is not 0):

<b>mfvsr</b>	04	vD	00000	00000	1540
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**Section #/Page #**                      **Changes**

A.1, Page A-2                      Change the **mtvscr** encoding as shown below (note: bit 31 is not 0 and vD should be vB):

<b>mtvscr</b>	04	00000	00000	vB	1604
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A.2, Page A-9                      Change the **mfvscr** encoding as shown below (note: bit 31 is not 0):

<b>mfvscr</b>	000100	vD	00000	00000	110 0000 0100
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A.2, Page A-9                      Change the **mtvscr** encoding as shown below (note: bit 31 is not 0):

<b>mtvscr</b>	000100	00000	00000	vB	110 0100 0100
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A.3, Page A-14                      Change the **mfvscr** encoding as shown below (note: bit 31 is not 0):

<b>mfvscr</b>	04	vD	00000	00000	1540
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A.3, Page A-14                      Change the **mtvscr** encoding as shown below (note: bit 31 is not 0):

<b>mtvscr</b>	04	00000	00000	vB	1604
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