Freescale Semiconductor
Product Brief

QUICC_CODESPB
Rev. 0, 06/2005

QUICC Code Solutions for the PowerQUICC II™ and PowerQUICC III™ Families

For access and edge infrastructure equipment, end manufacturers need to protect their hardware and software investment in already installed equipment while enduring the arduous task of supporting evolving protocol standards. Rising to meet this challenge, Freescale offers a range of QUICC code solutions that reduce the need for hardware design changes and instead provide seamless software upgrades.

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1 Overview

The PowerQUICC II (PQ2) and PowerQUICC III (PQ3) range of communications processors include an integrated communications processor module (CPM) or RISC microcontroller which can support downloadable RAM-based microcodes referred to as QUICC codes.

QUICC codes enhance the wealth of field proven layer 2 protocol (ATM, Ethernet, HDLC and PPP based) software support available today on the CPM. They provide equipment manufacturers with a seamless software upgrade to support evolving protocol standards using existing PQ2 and PQ3 hardware-based designs

Figure 1 shows the layer 2 software protocols supported today on the CPM with configurable device API drivers and initialization software.

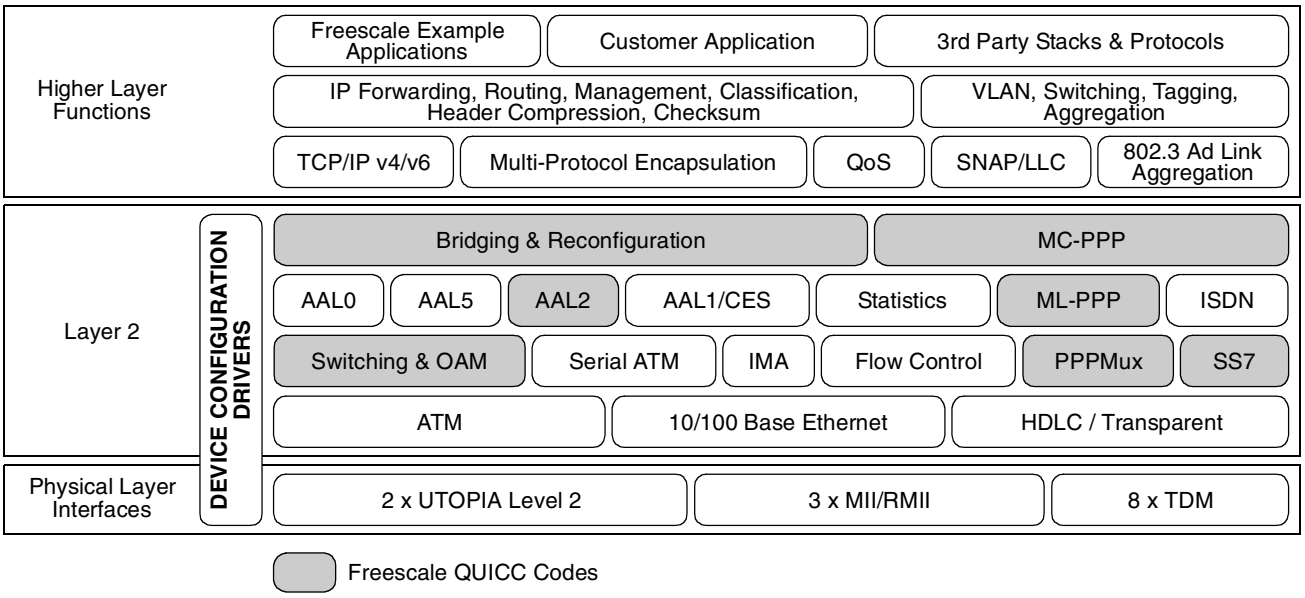

Figure 1. Protocol Support on the CPM

The MSP QUICC code extends the existing functionality available in ROM on the PowerQUICC family to support ATM layer switching and OAM functionality without core software intervention. Similarly, the FDS QUICC code provides automatic data forwarding (bridging) between an Ethernet FCC and an ATM FCC without the need for core software intervention.

The higher layer protocol functions, such as IP forwarding, routing, and classification, utilize third-party protocol stacks or customer software running on the PowerPC™ core.

The following QUICC codes are available today for Freescale's range of PowerQUICC II and PowerQUICC III devices and have been production quality tested both internally and externally by leading networking and telecom infrastructure companies. Freescale also provides a complete set of documentation, drivers and dedicated support for each QUICC code to quicken your time to market.

2 Enhanced SS7 (ESS7)

Signaling system #7 (SS7) is a global telecom standard used to define procedures and protocol by which network elements in PSTN exchange information over a digital signaling network for wireless and wire-line call setup, routing, and control. The PowerQUICC family is designed to support part of the message transfer part (MTP-2) layer functionality as defined in the ITU-T Q.703 (07/96) recommendations to enable applications requiring multichannel SS7 processing.

The ESS7 QUICC code extends the existing SS7 functionality available in ROM on the PowerQUICC family by providing support for high speed SS7 channels at T1/E1 rates, as defined by ITU-T Q703 Annex A recommendation and the Chinese YD/T1125 (2001) standard.

Key features of the ESS7 QUICC code include:

- Fully backward compatible with existing SS7 functionality on the PowerQUICC family
- Support for up to four independent SS7 channels at T1/E1 data rates on MCCs
- Maintenance of errored interval monitor (EIM)
- Discard of short signal units < less than 8 octets

The ESS7 QUICC code provides users with one global solution for all SS7 standards (including ANSI, ITU-T, JT, and YD/T1125) and utilizes the CPM to off-load SS7 MTP-2 tasks, which increases the bandwidth available on the CPU for application software.

SS7 is used in a variety of applications that encompass call-control/call-routing, wireline/wireless messaging, and intelligent networking. Figure 2 illustrates an overview of a universal mobile telephony system (UMTS) network for 3G wireless infrastructure where SS7 is used to convey signaling information.

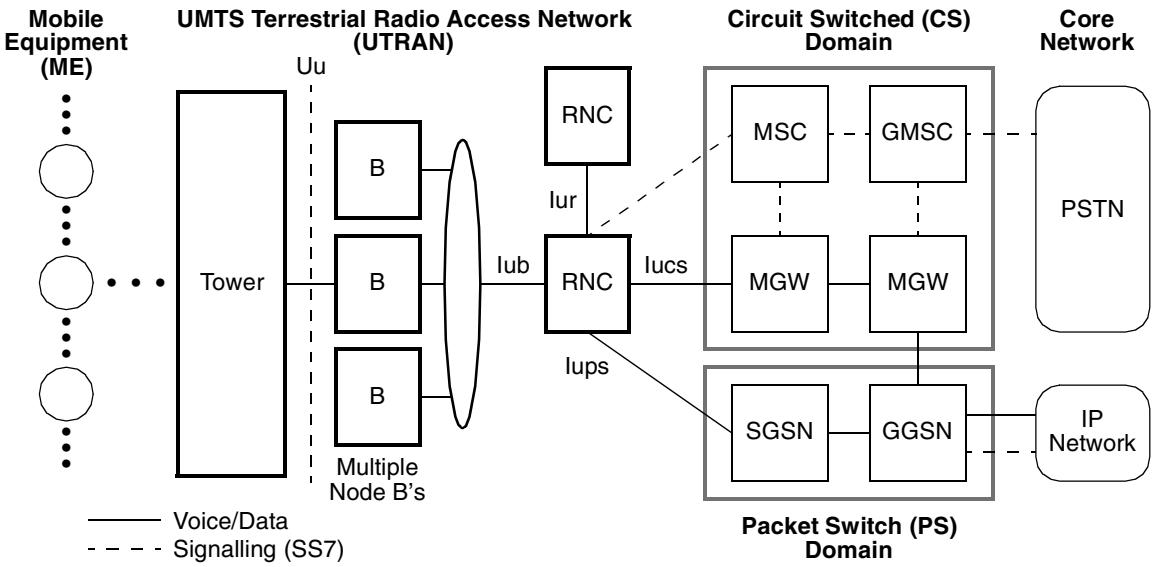

Figure 2. Overview of SS7 in 3G UMTS Network

The UMTS Terrestrial Radio Access Network (UTRAN) includes the radio network controller (RNC), the 3G base stations (node B's), and the air interface (Tower) to the mobile equipment (ME). The RNC is

responsible for controlling and managing the multiple base stations (node B's), including the utilization of radio network services. A node B handles radio channels, including the multiplexing/demultiplexing of user voice and data information.

3 Enhanced AAL2 (EAAL2)

ATM adaptation layer type 2 (AAL2) as defined by the ITU-T recommendations I.363.2 and I.366.1 enables an efficient method of multiplexing voice and data channels over a single ATM VC. The channels consist of packets transported within individual ATM cells. Each packet has a channel identifier (CID) so that each AAL2 user (channel) is uniquely identified by the triplet VP | VC | CID.

The EAAL2 QUICC code extends the existing AAL2 functionality available in ROM on the PowerQUICC family by providing support for up to 64K VC connections, AAL2 statistics gathering, and additional switch mode features.

Key features of the EAAL2 QUICC code include:

- Fully backward compatible with existing AAL2 functionality on the PowerQUICC family
- Support for TxQDs in external memory for up to 64K AAL2 connections
- Maintains statistical counters for the number of transmitted/received packets per CID, for AAL2 CPS and SSSAR modes
- Maintains statistical counters for the number of transmitted/received ATM AAL2 cells per VC, for AAL2 CPS and SSSAR modes

The EAAL2 QUICC code implements tasks such as statistics gathering (normally CPU-intensive and supported through counters managed by the CPM), thus increasing the bandwidth available on the CPU for application software.

Iub is the interface between the node B's and the RNCs and typically consists of multiple T1/E1 links from each node B aggregated to one or several ATM STM-1 (OC-3) links or one STM-4 link. Iur is the interface between the RNCs for soft handover. AAL2 is typically used as the transport mechanism to convey compressed voice and data over the Iur and Iub interfaces in wireless infrastructure equipment including node B's, RNCs and MGWs. Refer to Figure 2.

Additional features also supported with standard AAL2 QUICC code include the following:

- CID masking—enables efficient use of CPM bandwidth and internal memory by masking any unwanted AAL2 CIDs
- Auto-VC-on mode for switch mode—enables efficient use of CPM bandwidth when there are no AAL2 packets to transmit.
- PPRS (packet partial receive storage)—non-blocking queue for partial AAL2 packets in switch mode which reduces delays due to partial AAL2 packets received for transmission.
- Weighted fair queuing (WFQ) prioritization for AAL2 switch mode—support up to four queues per channel, enabling flexibility in scheduling and prioritization on a per-channel basis.

These additional features have been developed to support the increase in AAL2 user traffic rates, due to the introduction of HSPDA (high speed downlink packet access) in 3GPP release 5 for wireless infrastructure equipment.

4 Multi Service Platform (MSP)

The MSP QUICC code extends the existing ATM SAR functionality available in ROM on the PowerQUICC family by providing support for ATM layer switching functionality, QoS, and traffic management on both ingress and egress without CPU host intervention.

Key features of the MSP QUICC code include the following:

- ATM switching capabilities with no host intervention
- Support for policing in accordance with ITU-T I.371 and ATM Forum TM4.1 including GFR
- Support for billing, CLP0 and CLP1 cell count per VCC/VPC
- Statistics support for non-conforming cells and dropped cells
- Support for ATM scheduling per VCC, per VPC or arbitrary VCCs group bundle using prioritized FIFO, weighted round robin or mixed mode scheduling
- Support for multicast through WFQ algorithm or per VCC/VPC queuing mechanism.
- Support for ATM header translation based on VPI or VCI only or both.
- Simultaneous early packet discard and partial packet discard
- Enhanced APC scheduling modes (APC flux compensation and scalable APC) to support ATM PHYs with variable bit rate.
- Dynamic change-of-address compression tables to support mapping of ATM receive channels on more dynamic and more complex VP/VC ranges
- Support for dynamically adding or deleting ATM channels
- Transparent VP switching support in CAM address lookup
- Enhanced OAM support

The MSP QUICC code utilizes the CPM for ATM switching, policing, billing, and scheduling tasks, thus increasing the bandwidth available on the CPU for application software.

Typical applications for MSP include: DSLAM subscriber line cards, ATM multiplexers and concentrators, and cable modem controllers. Figure 3 illustrates how the MSP QUICC code could be used in a DSLAM access line card.

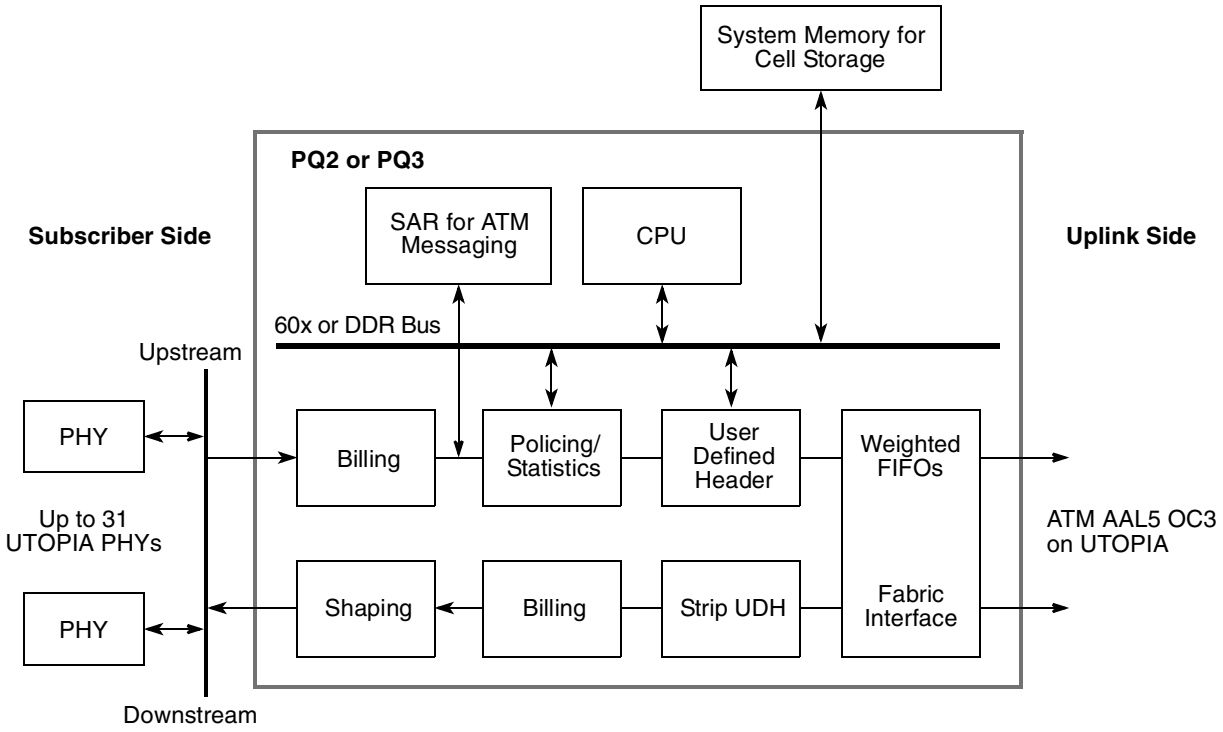

Figure 3. DSLAM Access Line Card Using the MSP QUICC Code on PQ2 or PQ3

The ATM controller on the CPM of the PQ2/PQ3 devices can be used to implement up to 31 PHYs for the subscriber side. Traffic from upstream link could be processed initially by the MSP QUICC code running on the CPM to offload billing, policing, and statistics tasks from the CPU.

User-defined headers could be added on the upstream link to provide additional routing information to the cell for the uplink multiplexing. At this point the cell can be transmitted over the multiplexed uplink. Depending on the system implementation the ATM cell traffic to be multiplexed onto the uplink may be prioritized (weighted round robin or fixed priority) or equal bandwidth allocated. All of these features are implemented by the MSP QUICC code.

On the downstream path, ATM cells are transported from the physical layer over the single UTOPIA interface via the PHY. The ATM cell traffic can be switched by stripping the channel code straight from the user-defined header or from the standard ATM cell header VP/VC combination. Billing and shaping functionality is once again carried out via the MSP QUICC code with minimal CPU intervention, and traffic is switched automatically to the required downstream virtual connection.

The aggregate bandwidth supported by the MSP QUICC code depends on the functions enabled in any given configuration. Under certain conditions the device will function as a 155Mbps switch.

5 Fast Data Switching (FDS)

The FDS QUICC code extends the existing functionality of the PowerQUICC family by allowing automatic data forwarding between fast communication controllers (FCCs). With the FDS QUICC code,

data can be forwarded between Ethernet-mode FCCs or between an Ethernet FCC and an ATM FCC without the need for core software intervention.

Key features of the FDS QUICC code include the following:

- Automatic data forwarding between Ethernet FCCs or between an Ethernet FCC and an ATM (AAL5) FCC
- Ethernet frame differentiation for Ethernet, 802.x, and VLAN frames
- Ethernet frame recognition using an external (hardware) CAM, or via CAM emulation with the SoftCAM feature, which supports up to 255 connections
- CAM search based on user-selected Ethernet frame header octets
- Re-direction of unrecognized Ethernet frames to a global queue
- Forwarding of multiple Ethernet channels to a single AAL5 virtual connection (VPI/VCI)
- Encapsulation feature allows programmable insertion, replacement, and removal of Ethernet frame octets
- Management of free buffer pools for received Ethernet data
- Programmable number of Ethernet transmit priority queues, up to a maximum of eight, to manage outbound Ethernet traffic priorities
- Time stamp to support aging of connections via CPU host software

Typical applications for FDS include: DSLAM line card, central office switches, Ethernet gateways and network edge equipment. Figure 4 illustrates how the FDS QUICC code could be used in a DSLAM access line card.

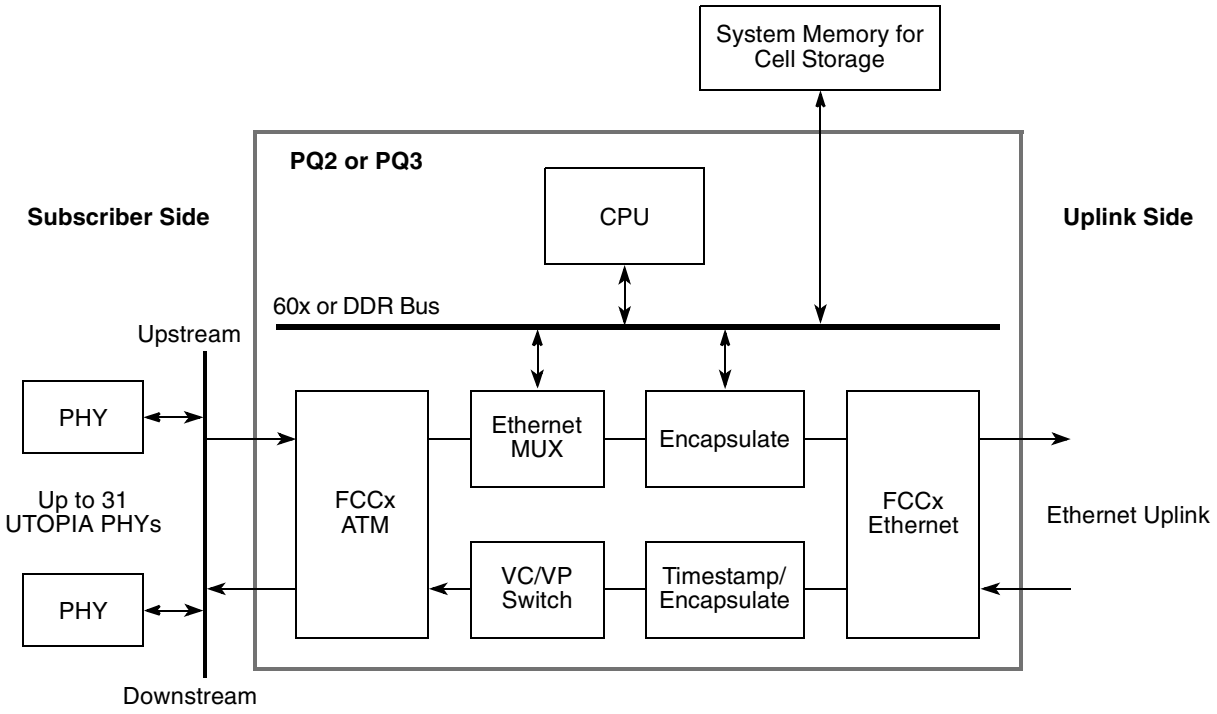

Figure 4. DSLAM ATM Access Line Card to Ethernet Uplink Using the FDS QUICC Code

The CPM's ATM controller can interface up to 31 ATM PHYs on the UTOPIA bus. In a DSLAM application, these ATM PHYs would connect to subscriber lines, and the FDS QUICC code would be used to forward the subscriber data from these lines to the Ethernet uplink (backhaul). Likewise, the CPM would forward Ethernet frames received from the backhaul to specific virtual connections on the desired ATM PHYs.

In the DSLAM's downstream direction, the CPM will build a CAM search string from user-selectable octets in the received Ethernet frame header. The search string will be sought in either an external CAM or in the SoftCAM located in dual-port RAM. The result of the CAM search will be a channel identifier (CID) that the CPM will use to determine how to handle the incoming frame. Frame-handling options allow the frame to be forwarded to a specified ATM PHY on the specified ATM FCC, and provide a means for modifying the frame header in ways such as deleting the Ethernet header or inserting an LLC encapsulation header if desired.

In the DSLAM's upstream direction, the CPM will derive a CID from the AAL5 frame header using the existing external CAM or address compression mechanism. The CPM will use the resulting CID to determine how to handle the incoming AAL5 frame. Frame-handling options allow the frame to be forwarded to a specified Ethernet FCC and with a specified transmission priority. If desired, the CPM can modify the AAL5 frame payload before it is transmitted on the uplink, as might be needed to remove an LLC encapsulation header, for example.

An additional feature provided by the FDS QUICC code allows Ethernet frames to be identified according to whether they are formatted as 802.3, Ethernet, or VLAN-tagged. By recognizing these different frame types, the CPM can be instructed to build CAM search strings differently for each frame type.

The FDS QUICC code's encapsulation feature can be used to implement the tag insertion, removal, and replacement needs of bridging and routing applications, and the Ethernet transmitter's priority queues can be used to support network quality-of-service (QoS) requirements. The FDS QUICC code uses the CPM to perform these low-level data-switching and encapsulation tasks, which increases the bandwidth available on the CPU for application software, thus enabling developers to maximize the value delivered to their customers.

6 Point-to-Point (PPP) Microcode

In recognition of the increasing popularity of IP technology and IP networks, the 3GPP specification in release 5 adds a secondary option to the transport network layer (TNL) using IP. The TNL links different pieces of network equipment in the UTRAN (see Figure 2). Now user data can be conveyed over UDP/IP in the Iur and Iub interfaces, in addition to the initially defined option AAL2/ATM. Therefore, next-generation node B implementations must be IP-ready, which means the data-plane processing must be configurable to support ATM as well as IP. IP is a layer-3 technology and generally utilizes much larger frame lengths. Unlike ATM, it has no built-in traffic-shaping techniques, and to utilize IP in the TNL requires additional fragmentation and segmentation techniques such as multilink PPP (ML-PPP), which allows delay-sensitive traffic to pre-empt non-delay-sensitive traffic. In addition, the use of PPP MUX reduces the PPP header overhead.

The PPP QUICC code extends the existing functionality available in ROM on the PowerQUICC family by providing support for termination of packet-oriented link layer protocols including PPP, multilink/multiclass (ML-PPP MC-PPP), and PPP Mux.

Key features of the PPP QUICC code include the following:

- Fully backward compatible with existing MCC HDLC functionality on the PowerQUICC family
- Support for point-to-point protocol (PPP) in accordance with RFC 1661
- Support PPP in HDLC like framing in accordance with RFC 1662
- Support for multilink PPP (ML-PPP) in accordance with RFC 1990, including user-defined sequence number format, either 12-bit or 24-bit, fragment loss detection and programmable MRRU
- Support multiclass (MC-PPP) extensions in accordance with RFC 2686 for up to eight classes with 2- or 4-bit user-defined class field
- Support for PPP Mux encapsulation in accordance with RFC 3153, for up to 256 sub-frames per fragment
- Support for dynamic addition and removal of link in a bundle
- Support for LCP frame handling
- Support for WFQ algorithm for class and queue selection on up to eight queues per link

The PPP QUICC code utilizes the CPM for tasks such as encapsulation and fragmentation of PPP packets, termination of ML/MC packets, and handling PPP Mux frames, thus increasing the bandwidth on the CPU for application software.

Figure 5 illustrates a generic 3G node B network interface card using the PPP QUICC code and PowerQUICC II or PowerQUICC III silicon.

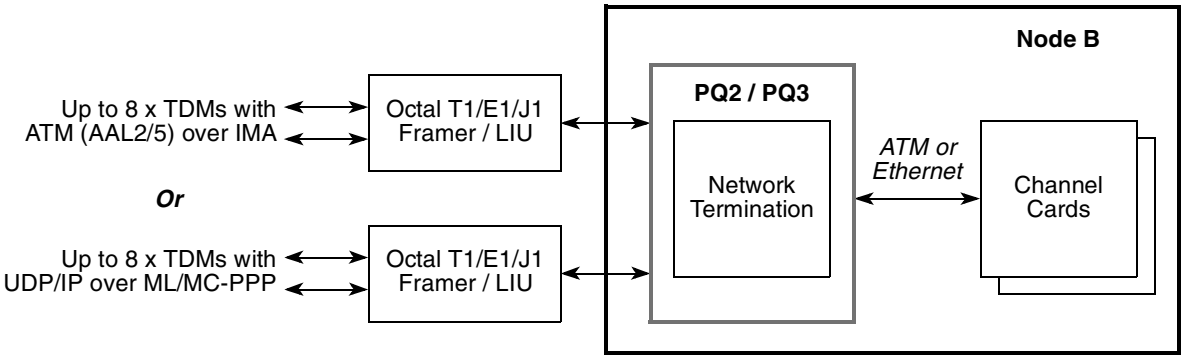

Figure 5. Generic Node B Network Interface Card Using the PPP QUICC Code

The PPP QUICC code enables a flexible transition from an ATM-based to an IP-based transport network layer, with minimal hardware design changes and a seamless software upgrade. This provides a shorter time-to-market as the transport network evolves and protects the user's investment by minimizing hardware and software development cost.

7 Summary

Freescale's range of QUICC codes offer modular, standard-compliant and field-proven software, compatible with the existing PowerQUICC architecture. In addition, these QUICC codes enhance the wealth of field-proven layer-2 protocol software support available today on the CPM.

QUICC codes provide support for the convergence of ATM and IP packet networks, for example, by adapting to different protocols, including ATM (AAL2, AAL5) and PPP, ML/MC-PPP, PPP Mux, with minimal hardware design changes and a seamless software upgrade.

Finally the PowerQUICC architecture continues to provide the most cost-effective solution with higher levels of system integration, performance and protocol support.

8 Revision History

Table 1 provides a revision history for this product brief.

Table 1. Document Revision History

Revision Number	Date	Substantive Change(s)
0	06/08/2005	Initial public release

Appendix A Supported QUICC Code Packages

Table 2 illustrates what QUICC code packages are supported on different silicon revisions and derivatives of the PowerQUICC II and PowerQUICC III families:

Table 2. Summary for QUICC Packages

Part Number / Description	MPC82xx [1] HiP3			MPC82xx [2] HiP4			MPC82xx [3] HiP7		MPC8560
Revision	**A.1**	**B.3**	**C.2**	**A.0**	**B.1**	**C.0**	**0.1**	**A**	**2.02**
MPC8260SW-ESS7 Enhanced SS7 microcode package	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MPC8260SW-EAAL2 Enhanced AAL2 microcode package	N/A	N/A	N/A	Yes	Yes	Yes	Yes	Yes	Yes
MPC8260SW-MSP Multi-service platform microcode package	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MPC8260SW-FDS Fast data switching microcode package	N/A	N/A	N/A	Yes	Yes	Yes	Yes	Yes	Yes
MPC8260SW-PPP PPP microcode package	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes	Yes

1 Devices: MPC8260 and MPC8255

2 Devices: MPC8260A, MPC8264A, MPC8265A, MPC8266A, MPC8255A, and MPC8250A

3 Devices: MPC8280, MPC8270, MPC8275

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